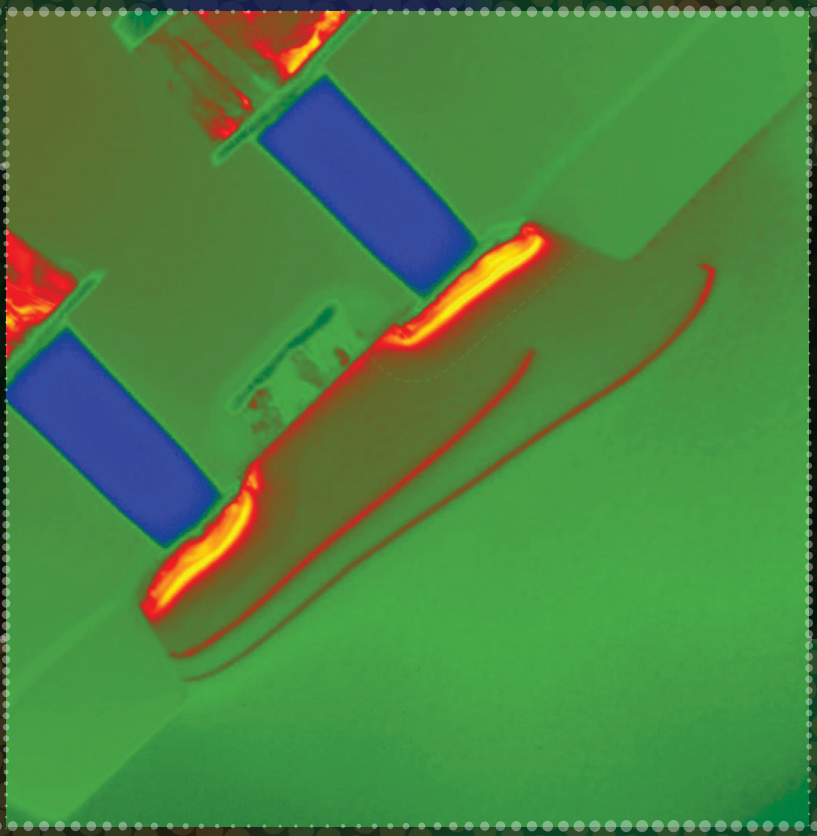
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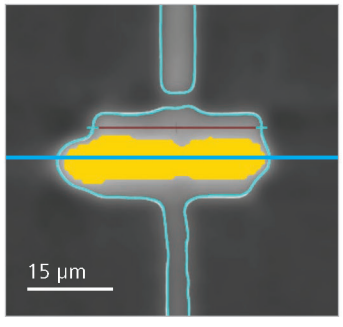
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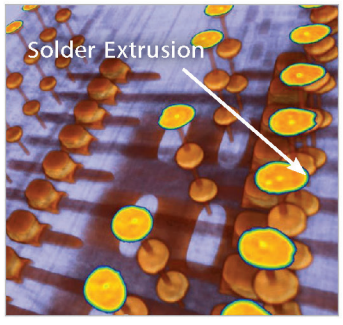
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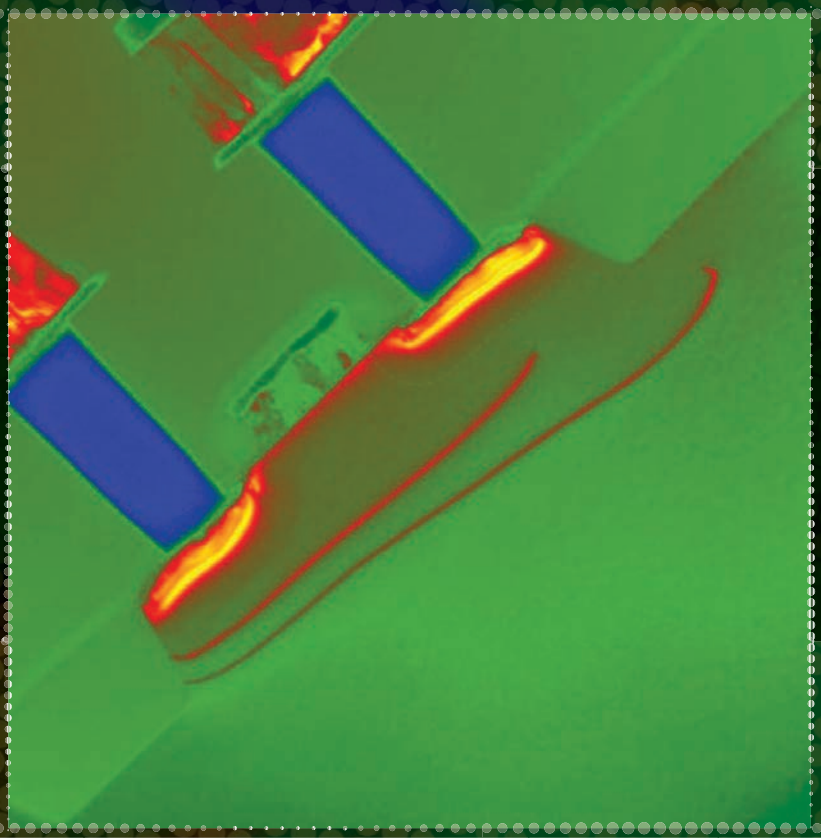
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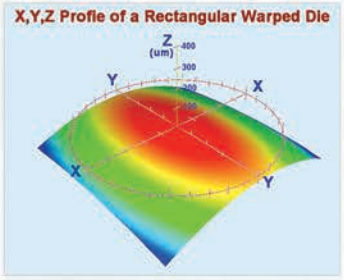
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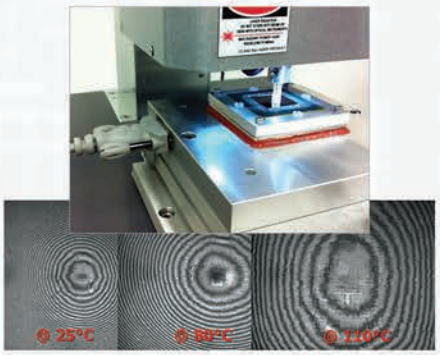
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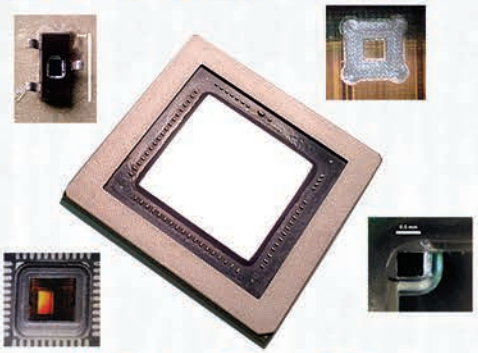
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4 Semiconductor Yield Modeling: A Primer

John Hopkins

This article provides an overview of models used to predict electrical wafer final test yield and how those projections may be used when deciding how to direct valuable failure analysis resources.

10 Recent Trends in Counterfeit Electronic Parts

Fred Schipp

Counterfeiting continues to be reported at a high volume in the electronics industry. This article outlines the extent of the problem, identifies the most susceptible parts and temperature ranges, and proposes a plan forward.

18 Ultrasonic Beam Induced Resistance Change

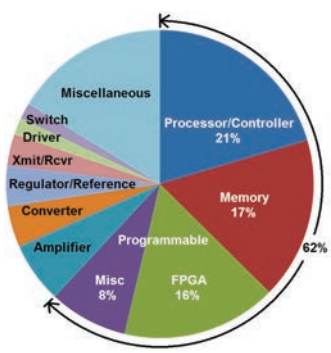
Toru Matsumoto

Conventional photo emission microscopy and infrared optical beam induced resistance change do not detect signals within a package because both methods rely on the detection of light. This article proposes ultrasonic beam induced resistance change as a superior alternative and outlines experiments showing its effectiveness.

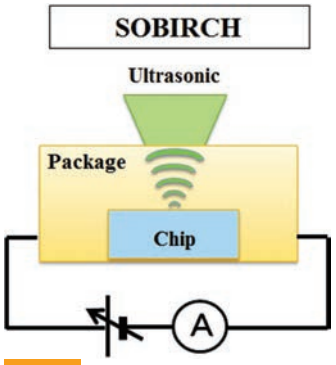
24 Locating Failures in Current Device Nodes: EBIC/EBAC, Current Imaging and Nanoprobing

Stephan Kleindiek, Rosalinda Ring, Klaus Schock, Andreas Rummel, Michael Zschornack, Pascal Limbecker, Andreas Meyer, Randy Newkirk, Kevin Davidson, and Matthias Kemmler

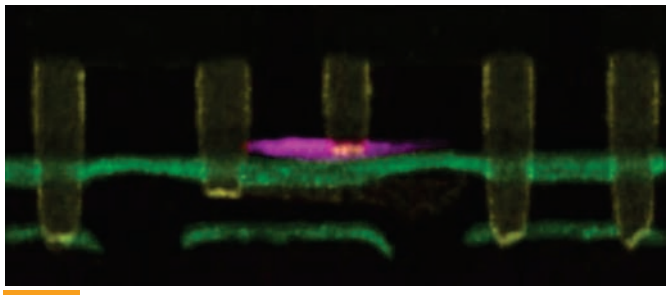
Advances in integrated circuit technology have made failure site localization extremely challenging. Using case studies, the authors show how to employ EBIC/EBAC, current imaging, and nanoprobing as valuable electrical fault isolation techniques.



10



18



24

ABOUT THE COVER

Dislocations Ablaze. This weak-beam dark-field TEM image shows two Si dislocations extending below the p-n junction (marked under the drain) of an nMOSFET. Only when voltage distribution was raised above a critical value did leakage emerge due to a depletion region expanding to include part of the dislocations, with electric field lines concentrating on the dislocations. *Photo by Wentao Qin, ON Semiconductor, First Place Winner in False Color Images, 2017 EDFAS Photo Contest.*

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AUGUST 2018 | VOLUME 20 | ISSUE 3

PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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Electronic Device Failure Analysis™ (ISSN 1537-0755) is published quarterly by ASM International®, 9639 Kinsman Road, Materials Park, OH 44073; tel: 800.336.5152; website: edfas.org. Copyright © 2018 by ASM International. Receive *Electronic Device Failure Analysis* as part of your EDFAS membership. Non-member subscription rate is $135 U.S. per year.

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GUEST EDITORIAL

CHALLENGES FOR BEYOND 14 NM SEMICONDUCTOR FAILURE ANALYSIS

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As semiconductor device scaling continues to shrink, not only is the cost of development skyrocketing, but competition regarding time to market is becoming fiercer among IC manufacturers. This scenario requires the development team to embrace both speedy learning cycles and reliable failure analysis (FA) methods. FA not only provides a rapid turnaround time and high success rate for root cause analysis of yield detractors, but also helps to explore new and more efficient learning opportunities.

In the very early stage of technology development, inline parametric structures are used to monitor device performance and ensure structural dimensions are on target. Parametric structures also help gauge process control robustness. After the parametric structures yield, large parametric and functional (logic and SRAM) structures are used to measure defects at the end of processing. Fault isolation/defect localization from inline parametric structures and functional structures becomes critical. Static and dynamic fault isolation techniques often are used to capture a spot signal from the sample. With the same technique and toolset, a similarly sized signal spot now covers a greater number of devices. Therefore, additional isolation or alternative techniques are required to pinpoint the exact defective device in the spot region.

One example is conductive atomic force microscopy (CAFM), which is performed to acquire electrical characteristics to localize the defective device. Compared to conventional passive voltage contrast (PVC), CAFM is more sensitive and captures the quantitative local conduction behavior of devices in the scanned region. Other examples include nanoprobing/atomic force probing (AFP), electrical probing on a microscopic scale, and electron beam absorbed current (EBAC), a high resolution, static technique. EBAC is often used to isolate defects and improve failure analysis success rates on both logic and SRAM devices.

The smaller critical dimension (CD) has pushed the limits of physical analysis tools and techniques. Scanning electron microscopy (SEM) resolution has become inadequate in clearly visualizing the defects, which in turn increases demand for transmission electron microscopy (TEM) analysis. Due to shrinking device dimensions and differences in device architectures and materials, TEM analysis is also facing new challenges. In the area of sample preparation, not only does the lamella need to be prepared thinner due to a smaller device CD, innovation in workflow is also required to accommodate changes resulting from new materials and architectures. Due to the

(continued on page 7)

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SEMICONDUCTOR YIELD MODELING: A PRIMER

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INTRODUCTION

A semiconductor fab typically produces a variety of semiconductor designs that exhibit a wide range of electrical wafer final test yields depending on the process technology maturity and product design complexity. At any given time, the average percentage of electrically good die on each finished production wafer can range from <10% to well over 90%. It is important to accurately predict the expected yield of each product to determine whether the yield is meeting expectations, and if not, to identify the characteristics of the shortfall. This article provides an overview of models used to predict electrical wafer final test yield and how those projections may be used when deciding how to direct valuable failure analysis resources.

ELECTRICAL TEST YIELD MODELS

Several different models are used in the industry to predict electrical wafer final test yield.[1,2] Although the math differs, all of the models account for process fault density and product design complexity. For the purposes of modelling electrical test yield, a fault is defined as a physical defect that causes the device not to meet the electrical test specification. Design complexity can be described in terms of either a physical or normalized die area. For example, one simple model is the Poisson model that can be written as:

$Y = e^{-AD_0}$ where A = die area and D_0 = fault density

A shortcoming of this model is that for two chips of the same area, there is no distinction between a densely populated logic design (very susceptible to defects) and a more forgiving design (for example, one with redundant SRAM). For a given fabricator fault density, this model would predict the same yield for each die.

The model can be improved by breaking out the total die area into sub-areas of different circuit categories and applying a factor to each area to account for the differing circuit complexity. For example, A1 might be the area of the die populated with dense logic, A2 the area of the die populated by SRAM with redundancy, and A3 the area of the die populated by SRAM without redundancy, etc. The total A would be A1F1 + A2F2 + A3F3 +…where F(n) is between 0 and 1 and accounts for the differing susceptibility to failure of the different circuit categories.

Another commonly used yield model is the Bose-Einstein model, which takes the form:

$Y = 1/(1 + AD)^N$ where A = die area, D = fault density/layer, N = complexity factor

The N factor in the Bose-Einstein model accounts for process complexity and is based on the number of critical mask levels. Figure 1 illustrates the effect of the N factor on the predicted yield for a particular fault density.

Although these models can account for differing design and process com-

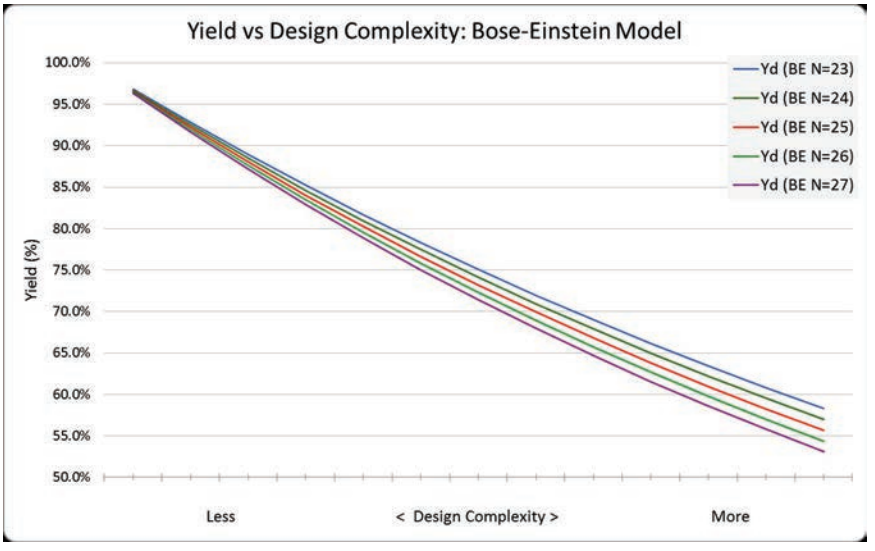


Fig. 1 Yield vs. design complexity for different process complexity factors N (Bose-Einstein model). Higher N corresponds to higher complexity and lower yield.

plexities, they do not account for the phenomena of defect clustering. One way to illustrate how defect clustering affects yield is to consider two cases involving a wafer with 100 die that is subject to exactly 100 chip killing defects. In Case 1, the 100 defects are distributed evenly across the wafer such that one defect falls on each die. The yield will be 0% (all 100 die are killed by one of the 100 defects). In Case 2, the 100 defects are highly clustered and hit only one of the die on the wafer. Although the fault density is exactly the same in both scenarios, the Case 2 yield will be 99%. If clustering is not accounted for, it can result in an underestimation of the yield of large die.

A model that takes into account both circuit complexity and clustering is the negative binomial model:[3,4]

$Y = 1/(1 + A_C D/\alpha)^{\alpha}$ where A_C = critical area, D = defect density and α = cluster factor

A_C is the portion of the die area that is susceptible to defects of a certain size that cause electrical failures. The A_C can be algorithmically determined using various commercial DFM tools.[5] The lower the cluster factor α, the more clustered the defects. The technology α for a fab can be extracted by plotting yield vs. area for various groupings of die yield and typically ranges between 1 and 10.[2] Note that as α approaches infinity, the negative binomial model approaches the Poisson model, as shown in Fig. 2.

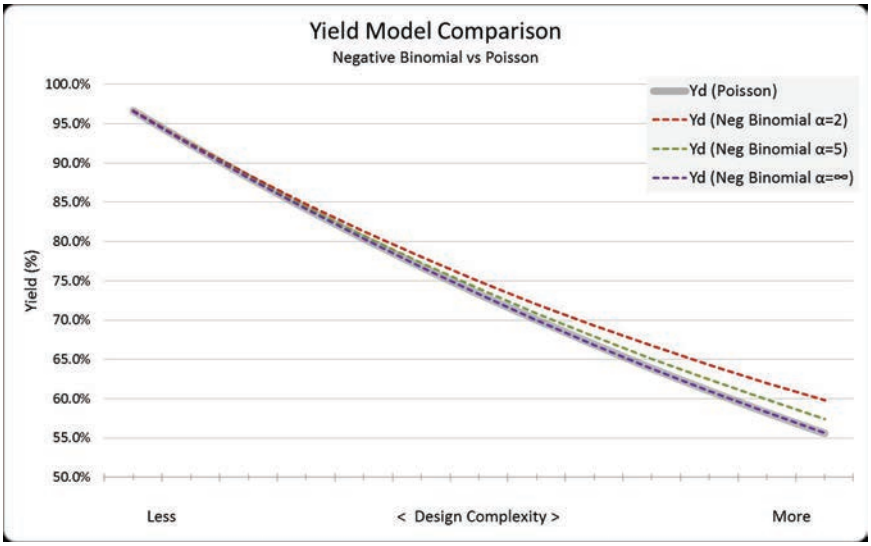


Fig. 2 Yield vs. design complexity for different cluster factors α (negative binomial model). Lower α corresponds to a higher degree of clustering, which results in better yield for larger, more complex designs.

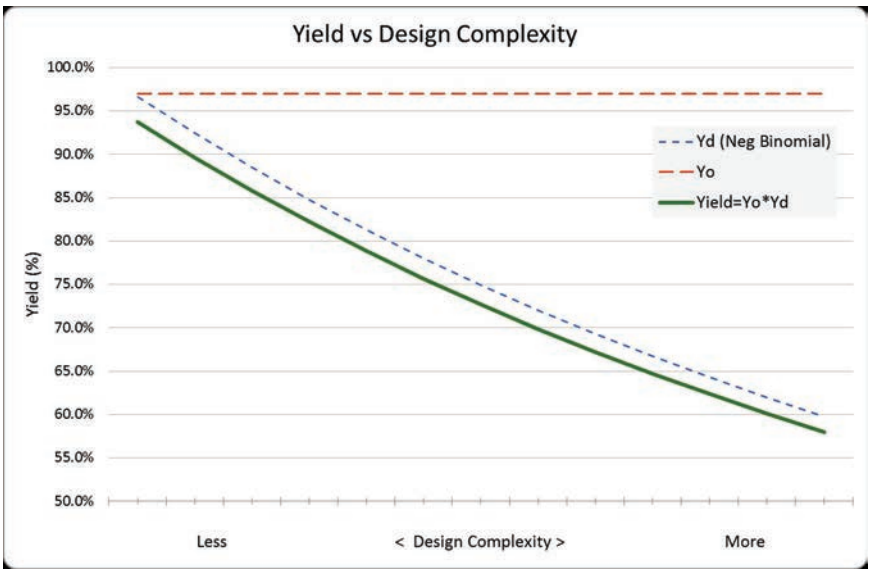


Fig. 3 Yield vs. design complexity. Negative binomial-based model that accounts for both systematic (Y_0) and random defect (Y_D) effects.

SYSTEMATIC VS. RANDOM DEFECT YIELD LOSS

In the yield model equations discussed so far, it is assumed that the yield loss is driven entirely by randomly distributed defects. In reality, a portion of the yield loss can often be attributed to nonrandom systematic mechanisms. Examples include non-centered device parameters, misaligned lithography levels, under- or over-polished insulator layers, etc.[4] These types of mechanisms tend to kill die independent of their layout complexity. To account for this nonrandom defect loss, a systematic yield component (Y_0) must be added to the model:

$Yield = Y_0 * Y_D = Y_0 * 1/(1 + A_C D/\alpha)^{\alpha}$

This negative binomial model takes into account design complexity, clustering, and systematic yield loss mechanisms, as shown in Fig. 3.

Being able to categorize the type of yield loss as random or systematic is important for estimating the yield impact on other products. The random yield (Y_D) impact scales with circuit complexity, while the systematic yield (Y_0) impact is independent of circuit complexity.

The random defect yield can be scaled as follows. A Poisson model is used for simplicity:

Product 1: $Y_{D1} = e^{-A_1 D}$; $D = -\ln(Y_{D1})/A_1$

Product 2: $Y_{D2} = e^{-A_2 D} = e^{-(-\ln(Y_{D1})/A1)A_2} = Y_{D1}^{A2/A1}$

where Y_D = random defect yield, A = die area, D = defect density

As an example, if an increase in the fab's defect density causes a 3.5 point Y_D loss to Product 1, we can calculate the impact to Product 2, which has twice the circuit content as Product 1.

For this example, assume:

Prior to yield drop: Product 1 Y_{01} = 97%, Y_{D1} = 70%.
Assume $Y_{01} = Y_{02} = Y_0$

Using the Poisson model for the random yield component:

- Product 1 yield pre Y_D drop = $Y_0 * Y_{D1}$ = 0.97 * 0.7 = 67.9%
- Product 1 yield post Y_D drop = 0.97 * (0.7-0.035) = 64.5%
- Product 2 yield pre Y_D drop = $Y_0 * Y_{D1}^n$ = 0.97 * 0.7^2 = 47.5%
- Product 2 yield post Y_D drop = 0.97 * $(0.7-0.035)^2$ = 42.9%

So the overall yield impact to Product 1 is a 3.4 point degrade and a 4.6 point degrade to Product 2.

Notice in this example, the systematic yield component did not change. As a second example, instead of a 3.5 point Y_D loss, consider the impact of a 3.5 point systematic (Y_S) yield drop:

- Product 1 pre Y_S drop = $Y_0 * Y_{D1}$ = 0.97 * 0.7 = 67.9%
- Product 1 yield post Y_S drop = (0.97-0.035) * 0.7 = 65.5%
- Product 2 yield pre Y_D drop = $Y_0 * Y_{D1}^n$ = 0.97 * 0.7^2 = 47.5%
- Product 2 yield post Y_D drop = (0.97-0.035) * 0.7^2 = 45.8%

In this case, Product 1 experiences a 2.4 point degrade and Product 2 experiences a 1.7 point degrade. Because systematic yield does not scale with circuit content, the impact is proportionally larger on the better yielding (typically smaller) die.

YIELD ACCOUNTING BY CIRCUIT TYPE

A common question that arises as part of yield analysis activities is whether an observed yield loss for a particular die subcomponent is as expected or not.

As an example, consider the hypothetical 1cm² die illustrated in Fig. 4. Assume that the area of each individual block of logic and memory is known and that the electrical test allows the yield of each individual block to be broken out. A large number of die are tested and the average yield of each block is compiled.

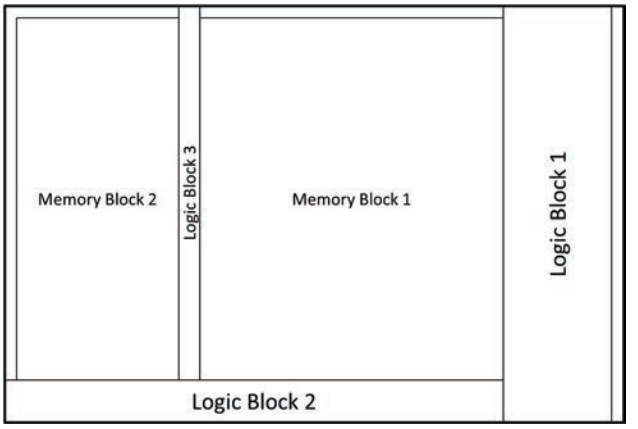


Fig. 4 **Hypothetical chip floor plan with die area broken out by circuit type.**

Table 1 Expected yield by block for hypothetical die using a Poisson yield model

	A (cm²)	Y_D (%) Expected *	Y_D (%) Actual
Logic Block 1	0.4	89.4	
Logic Block 2	0.2	94.6	
Logic Block 3	0.1	97.2	90%
Memory Block 1	0.2	94.6	
Memory Block 2	0.1	97.2	
Total Die	1.0	75.6	

* Poisson D_0 = 0.28/cm²

Table 1 contains the area of each block. Using the Poisson model, the expected yield of each block can be calculated. If the observed test yield of Logic Block 3 is 90% and the other blocks are yielding close to expectations, that might suggest there is a systematic layout or test issue with that block.

CONCLUSION

In summary, this discussion provides a general overview of yield model approaches. Ideally, the yield model takes into account relative circuit complexity and defect clustering. The difference between systematic and random defect yield loss was discussed. Random defect yield scales with circuit complexity, while systematic yield loss generally does not. Both systematic and random defect components of yield loss must be accounted for in a complete model. As the examples in this article demonstrate, with a basic understanding of common yield models, the reader can estimate expected yield losses, understand yield differences between designs, and even identify abnormal yield results within a particular design. Yield

modeling can be used to quantify expected yield loss and direct valuable failure analysis resources where the most yield benefit may be realized.

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ABOUT THE AUTHOR



John Hopkins received a B.S. degree in electrical engineering from the University of Colorado, Boulder in 1979 and an M.S. degree in electrical engineering from the University of Vermont, Burlington in 1985. From 1980 to 2014, he worked for IBM in Essex Junction, Vt. He has been an integration and yield engineer with GlobalFoundries in Malta, N.Y., since 2014.

GUEST EDITORIAL

CONTINUED FROM PAGE 2

3D structure of FinFETs, advanced techniques such as scanning transmission electron microscopy (STEM) and energy-dispersive x-ray spectroscopy (EDS) tomography are often needed to understand the root cause.

As the process becomes ever more sophisticated, defect mechanisms are also becoming more complex. For example, as the smaller CD strains the limit of fabrication tools, the process window for each module becomes tighter and therefore the root cause of a defect may depend on multiple process steps. As device geometries have shrunk beyond double digits nm, the time and effort required to find non-obvious defects has increased.

To be successful, FA analysts will need to have an in-depth understanding of FA techniques and tool limitations in order to rapidly identify and apply the most appropriate techniques. They will also need to develop close collaborations with cross-functional teams in order to speed up yield learning. Early identification of systematic process issues provides key information to the various technology teams for working model validation. Understanding the root cause of failures through precise localization, electrical characterization, and defect imaging is crucial for accelerating advanced technology development.

NOTEWORTHY NEWS

ESREF 2018

The 29th European Symposium on Reliability of Electron Devices (ESREF 2018) will take place **October 1-5** in Aalborg, Denmark. The international symposium continues to focus on recent developments and future directions in failure analysis, quality and reliability of materials, devices and circuits for micro-, opto-, power, and space electronics. It provides the leading European forum for developing all aspects of reliability, including management and advanced analysis techniques for present and emerging semiconductor applications. All aspects related to specification, technology and manufacturing, testing, control, and analysis are addressed. In 2018, ESREF celebrates its return to Denmark after exactly 20 years. The host city is known for the efficiency and reliability of its renewable energy plants, including photovoltaic and wind turbine technologies.

For more information, visit esref2018conf.org.

NOTEWORTHY NEWS

MICROSCOPY & MICROANALYSIS 2018 MEETING

The Microscopy & Microanalysis (M&M) 2018 meeting will be held **August 5-9** in Baltimore. The scientific program features the latest advances in biological, physical, and analytical sciences as well as techniques and instrumentation. Complementing the program is one of the largest exhibitions of microscopy and microanalysis instrumentation and resources in the world. Educational opportunities include a variety of Sunday short courses, tutorials, workshops, and pre-meeting congresses for early-career scientists. The opening reception offers a networking venue for meeting new people in the field and renewing old acquaintances, while the Monday morning plenary session showcases talks from outstanding researchers and recognizes major Society and meeting award winners. In addition, daily poster awards will highlight the best student posters in instrumentation and techniques as well as biological and physical applications of microscopy and microanalysis.

M&M is sponsored by the Microscopy Society of America, the Microanalysis Society, and the Microscopical Society of Canada. For more information, visit microscopy.org/MandM/2018.

NANOTS 2018

The 38th annual NANO Testing Symposium (NANOTS 2018) will be held **November 19-20** at the KFC Hall, Kokusai Fashion Center, in Tokyo. NANOTS is one of the leading technical symposiums for discussing solutions that improve the testing process of nanoscale devices and materials. The two-day event will consist of a symposium with a special invited talk, a special session, technical sessions, a commercial session, an equipment exhibition, and an evening session.

Presentations on original, noncommercial, and nonpublished works are being solicited. Papers for the special session and technical sessions are peer-reviewed and selected based on a clear outline of problem, analysis, solution/results, and conclusion. **Abstracts are due July 27,** with abstract submission beginning in June.

NANOTS is sponsored by the Institute of NANO Testing in cooperation with the Institute of Electronics, Information, and Communication Engineers, the Japan Society of Applied Physics, the Reliability Engineering Association of Japan, and the Union of Japanese Scientists and Engineers.

For more information, visit the NANOTS website at www-nanots.ist.osaka-u.ac.jp/en.

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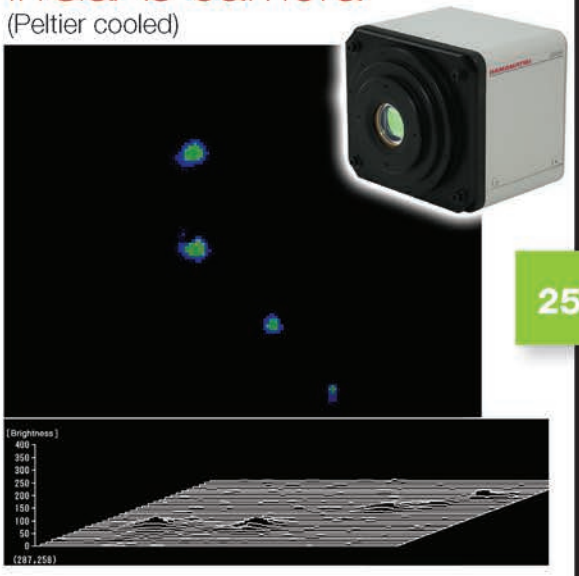
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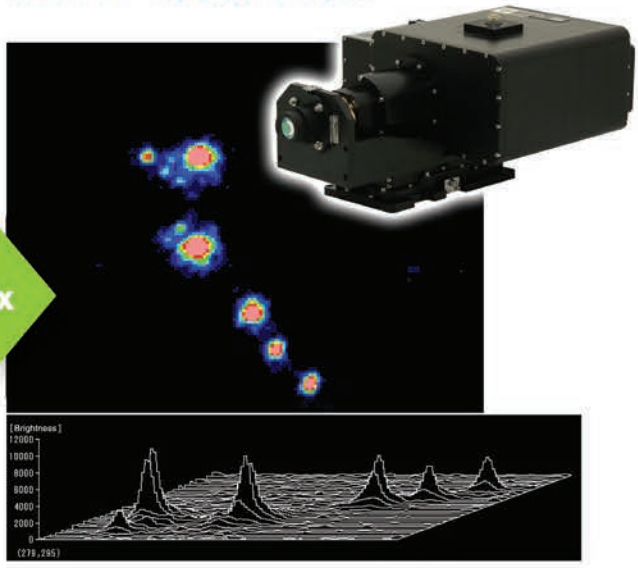
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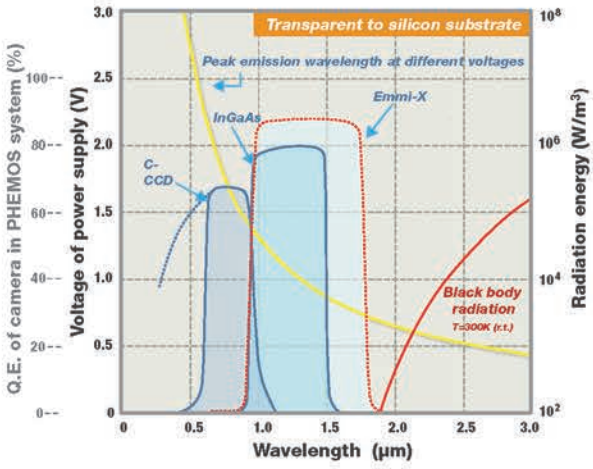
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RECENT TRENDS IN COUNTERFEIT ELECTRONIC PARTS

Fred Schipp
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Counterfeit electronic parts have been the scourge of the electronics industry for more than a decade. In fact, reports of suspect counterfeit parts can be found in Government-Industry Data Exchange Program (GIDEP) database reports as early as the 1970s. Since the turn of this century, counterfeiting of electronic parts seems to have reached epidemic proportions. ERAI,[1] a member-based organization that tracks reports for suspect counterfeit parts, has averaged nearly 100 reports per month for more than five years, although that trend appears to be decreasing. This count, although high, is assumed to be just a fraction of the true counterfeiting total.

It is difficult to assess the true impact of counterfeit electronic parts. The most common counterfeit part actually has the correct internal die, so it functions correctly in the circuit. The problem is that the part may have been tested to a slower specification or to a smaller temperature range (e.g., commercial instead of industrial). Another major concern is that the part has likely seen prior use, followed by removal and refurbishment under undesirable circumstances. This handling and refurbishment creates a significant risk of mechanical (cracks and breaks), electrical (electrostatic discharge), chemical (corrosion), or thermal (delamination and die voids) damage.

These examples all contribute to yielding a part that, despite passing initial testing, may be a ticking time bomb—partially damaged or unsuitable for the application, and perhaps likely to fail at a critical time.

This article does not seek to determine the system impact of counterfeit electronic parts nor does it address intentionally modified, malicious counterfeits, or even cloned devices. Instead, it provides data in order to estimate the actual extent of counterfeiting, analyzes data to identify recent trends in counterfeiting certain part types, and assesses the current value of authentication methods. Most of this information applies to standard "vanilla" counterfeits. These are parts assumed to have been modified to allow the counterfeiter to profit.

EXTENT OF THE PROBLEM

The best place to assess the extent of the problem is through analysis of ERAI data. ERAI is a paid membership organization that has been logging suspect counterfeit and high-risk parts at least since 2005. The parts reported in ERAI are not all suspect counterfeit, but most are thought to be so. This data suggests a continuous increase in monthly reports, plateauing at approximately 95 monthly reports for a nearly five-year span from 2011 through 2015. However, the same data indicates a steady reduction in monthly reports for the past two years or more (see Fig. 1).

Why the downward trend? The optimist might conclude this is due to several reasons, while the pessimist may have completely different theories regarding the downward trend. Below are a few optimistic explanations for the reduction since 2015:

- Fewer parts are being counterfeited because it is too tough to make a profit.
- More counterfeit parts are being caught at the U.S. border and are not making their way to reporting companies.
- Fewer counterfeit parts are being purchased due to increased awareness and obsolescence management.

[1]ERAI Inc. is a global information services organization that monitors, investigates, and reports issues affecting the global electronics supply chain. Members include aerospace, defense, medical, nuclear, and commercial OEMs, CMs, OCMs, distributors, government agencies, industry associations, and other organizations serving the industry.

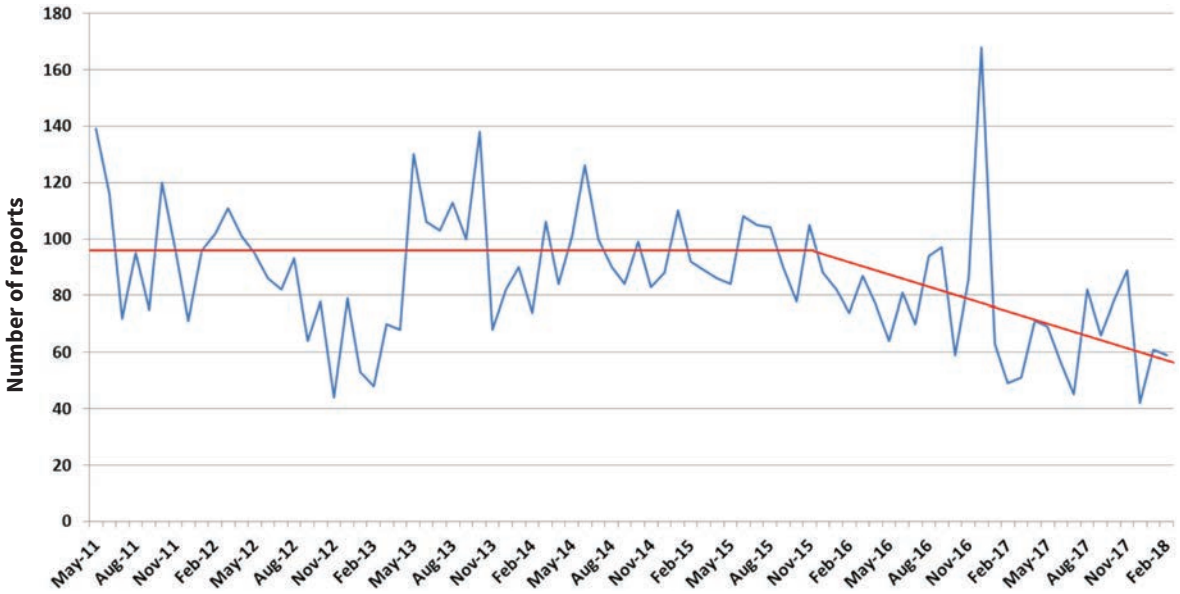


Fig. 1 **ERAI monthly reports, counterfeit and high-risk parts.**

Corresponding pessimistic arguments are as follows:

- Fewer counterfeit parts are being detected because quality is outpacing detection methods.
- Fewer counterfeit parts are being reported.

The recent downward trend is likely due to a combination of these reasons. No doubt, distributors, contractors, and government organizations are more aware of the counterfeit risk in recent years and many organizations have enacted new, robust processes aimed at keeping counterfeit parts from being purchased. Supplier audits and assessments, proactive obsolescence management, and decreased reliance on the unauthorized supply chain (or gray market) have certainly reduced the opportunity for an organization to buy a counterfeit electronic part. In addition, law enforcement personnel are continuing their efforts to seize counterfeit parts at border entry points.

Conversely, it is also assumed that counterfeiters are finding betters ways to remove markings, apply coatings, remark parts, replate leads, and disguise other part variations that would be red flags for personnel performing authentication work. While the trend since 2015 is encouraging, it should be taken with a grain of salt. Counterfeit electronic parts should be presumed to be an ongoing challenge for the foreseeable future. Note, recent data through May 2018 shows the trend leveling off or rising again.

POPULAR COUNTERFEIT PARTS

Integrated circuits, or ICs, have been the most commonly counterfeited electronic part as far back as data exists. In fact, ICs have comprised 85 percent of all counterfeit electronic parts every year from 2012 through 2016. The remaining most-counterfeited electronic part types include transistors, diodes, and capacitors, in this order.

The data shows that all types of integrated circuits are susceptible to counterfeiting, from complex parts such as microprocessors and field programmable gate arrays (FPGAs) to basic building blocks such as digital gates and operational amplifiers. However, it appears that the more complex IC types are more attractive to counterfeiters. For 2017, as in previous years, over 60 percent of suspect counterfeit ICs fall into three categories—microprocessors/microcontrollers, memory, and complex programmable logic devices (including FPGAs).

Figure 2 shows the breakout by IC part type, with these three categories comprising 62 percent of the reported ICs. This should not be particularly surprising, as these are the

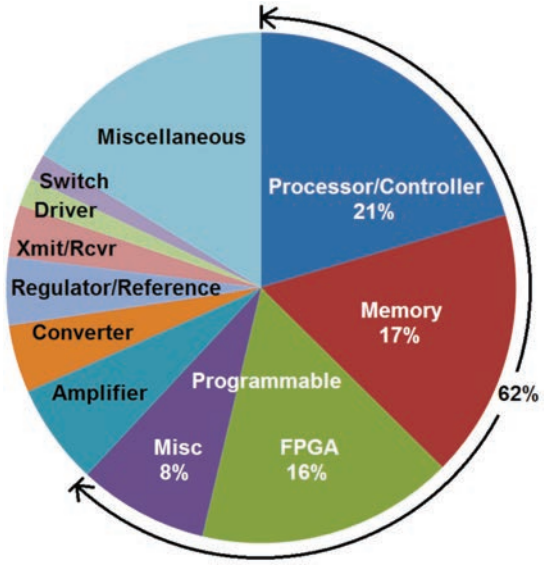


Fig. 2 **Suspect counterfeit percentage by integrated circuit type, 2017.**

most complex part types and are more likely to be prime targets, due to the following reasons:

- Less likely to have multiple manufacturers making pin-compatible parts
- More likely to undergo frequent upgrades or revisions for faster, better parts
- More likely to be considered critical components of a system

The result is that the three most highly counterfeited IC part types are also more likely to cease production earlier—thus becoming obsolete—and be replaced by better versions. Once obsolete, in-production replacements are less likely to be found from competitors, leaving the system designer facing the challenge of either finding out-of-production parts or redesigning the system to accept a new design. This is the perfect storm that forces a search of the gray market where the counterfeit part risk soars. These parts often list for many times the standard price, maximizing profit.

Analysis of recent data shows a decreasing trend in IC percentage, accompanied by an increasing trend in transistors and capacitors. Figure 3 shows the part-type breakdown for 2017, confirming this trend. Data for 2018 is updated through March 17. Because the 2018 snapshot reflects less than a quarter of the year, it is not conclusive. However, it should be noted that both rising trends (transistors and capacitors) have been present since the fourth quarter of 2017. For example, there have been more suspect capacitor reports (45) in the six months from September 2017 through March 2018 than in the two years prior (43).

It appears from the data presented that counterfeiters may be delving into more counterfeiting of lower complexity parts, including discrete semiconductors and passive components.

A DEEPER LOOK AT CAPACITORS

The trending counterfeit capacitor phenomenon can be broken down further into capacitor types (e.g., ceramic, tantalum, aluminum electrolytic, film, etc.). Figure 4 shows this trend from 2012 through mid-March 2018.

As indicated here, the increase in capacitor reporting is almost exclusively due to ceramic capacitors. On the surface, this is counterintuitive, because ceramic capacitors are typically among the cheapest electronic parts, often selling for pennies. On the other hand, tantalum and aluminum electrolytic capacitors sell for 10 times this price or more. While these parts, along with film, porcelain, and other specialty capacitors are also counterfeited, their percentages are much lower. Why? A review of the part numbers, reports, and a little analysis of ceramic capacitor design reveals the reason why counterfeiting of these parts is profitable.

First, ceramic capacitors are small. With length and width typically down to a tenth of an inch or less, there is seldom room for marking the parts. Therefore, a counterfeiter need not worry about removing markings, recoating parts, and adding new markings.

Second, there is great variation in capacitance value, voltage, and tolerance within the same size package. Low value, low voltage, or high tolerance parts can be packaged and labeled as if they are high value, high voltage, or low tolerance parts, thus increasing their value. There is virtually no difference in the physical size of these parts, except perhaps a slight variation in thickness.

(continued on page 14)

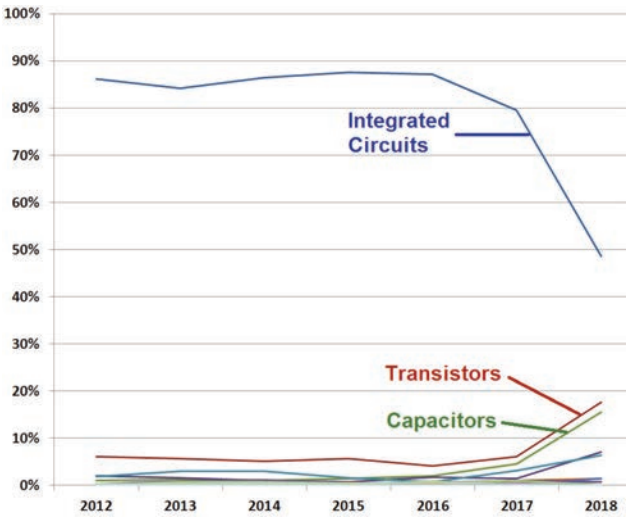


Fig. 3 **Suspect counterfeit percentage by part type.**

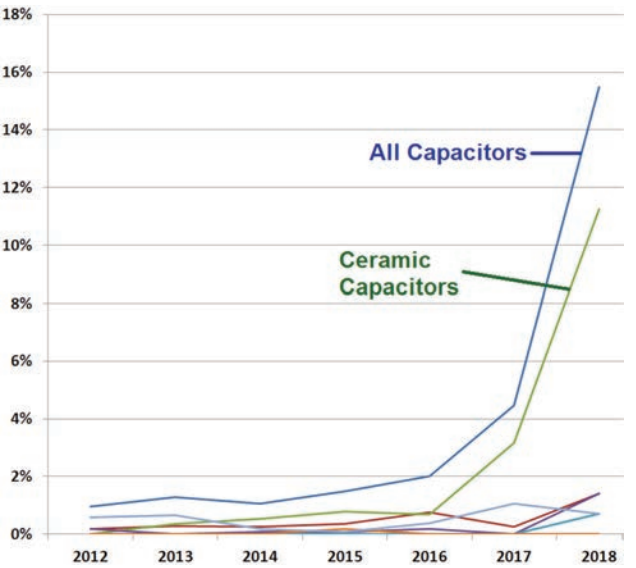


Fig. 4 **Suspect counterfeit percentage by capacitor type.**

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RECENT TRENDS IN COUNTERFEIT ELECTRONIC PARTS *(continued from page 12)*

Third, temperature response of ceramic capacitors can vary widely. The ceramic dielectric within the part determines whether the capacitance value will be stable over a wide temperature range. While the C0G dielectric formulation maintains a stable value within 1 percent from –55° to 125°C, the Y5V formulation loses over 80 percent of its 25°C value when the temperature reaches 100°C. A counterfeiter can realize a profit be selling a Y5V dielectric as a C0G part. A few of the reported suspect counterfeit ceramic capacitors were noted as having failing capacitance value over temperature, which suggests those parts were the wrong dielectric.

Fourth, capacitor characteristics such as voltage and dielectric are not easily detected during receiving inspection. While value and dissipation factor are commonly measured, voltage is not an easy characteristic to verify. Determining whether a 10V capacitor has been illegally substituted for a 50V part might not be possible without submitting a sample to an overvoltage test to note whether any parts fail. Checking for the wrong dielectric might require testing the parts at elevated temperature. Neither test is commonly performed at receipt.

Finally, system failures due to counterfeit ceramic capacitors may be particularly hard to detect. Because many ceramic capacitors serve to filter out noise or unwanted voltage spikes, the failure mode for a counterfeit capacitor is likely to be an intermittent glitch or reset of an IC. These failure modes are notoriously difficult to troubleshoot and may be more likely to result in changing the integrated circuit rather than identifying the faulty capacitor.

COMMON TEMPERATURE RANGES FOR COUNTERFEITING

Counterfeit electronic parts are of particular concern when the application is mission or safety critical. In general, parts intended for higher temperature range applications tend towards higher criticality. There are exceptions, but most would agree that electronic parts tested and used in military or automotive applications are more likely to be critical than parts for commercial and to some extent industrial applications. In addition, parts in these applications are usually more expensive than their commercial counterparts, always an important factor in the counterfeiter's business model. Finally, it makes sense for a counterfeiter to falsify a lower temperature range (i.e., commercial) marking in order to reap the higher cost of the high temperature range part. So can we identify any trends in counterfeiting for these temperature ranges?

ERAI's reporting data on integrated circuits since 2012 was sampled for temperature range, and those parts classified as commercial (0° to 70°C), industrial (–40° to 85°C), automotive (–40° to 125°C), and military (–55° to 125°C). Many part temperature listings did not fit these ranges perfectly, so they were categorized into the closest applicable range. The results are as follows: Data in Table 1 was compared with IC usage estimates taken from Statista and IC Insights, which estimate military temperature range usage of only 1 percent, and commercial temperature range applications using over 70 percent of ICs. Based on this information, it appears that even though they comprise only a small portion of suspect counterfeit integrated circuits, a military temperature range part is much more likely to be counterfeit than a commercial or automotive part—perhaps as much as 15 times likelier. Industrial temperature range parts are also more likely to be counterfeited.

COMMONLY COUNTERFEITED MANUFACTURERS

The data can also be analyzed to determine which original component manufacturers' (OCM) parts are most commonly counterfeited. It must be noted that the manufacturers are not a party to counterfeiting. Therefore, the presence of an electronic part manufacturer on this list should in no way be construed negatively for the manufacturer.

The data presented in Fig. 5 for 2012 through 2017 is stunning, in that one manufacturer's parts are reported much more frequently than the rest. The chart captures

Table 1 Reported integrated circuits by temperature range, 2012 – 2017

Temperature range type	Range	Percent of reported ICs, 2012–2017
Commercial	0° to 70°C	41%
Industrial	–40° to 85°C	45%
Automotive	–40° to 125°C	3.7%
Military	–55° to 125°C	11%

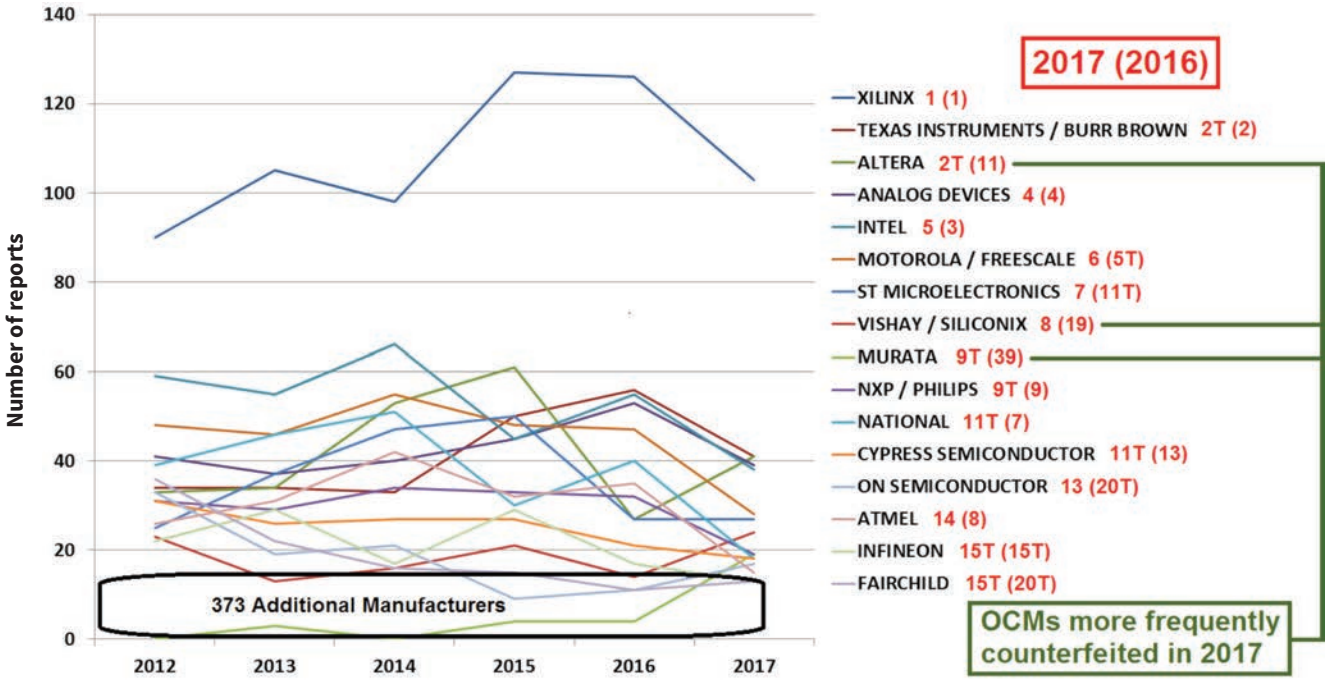


Fig. 5 **Suspect counterfeit reports by manufacturer.**

the number of yearly ERAI reports for the 16 most-counterfeited manufacturer parts (in 2017), and notes there are 373 additional manufacturers with suspect counterfeit parts reported in this six-year span. It is unclear why Xilinx's parts are so popular with counterfeiters, but it's likely a combination of high price, high design turnover (increased obsolescence), and the fact that Xilinx FPGAs and other programmable parts are extremely popular in complex, critical systems.

The data to the right of the figure, in red, shows the rankings (from most counterfeited to least) for 2017 vs. 2016. Note that the three biggest movers up the ladder (an undesirable trend) are Altera, Vishay/Siliconix, and Murata. Altera trails only Xilinx in the manufacture of complex programmable parts. Vishay/Siliconix manufactures a wide range of electronic parts, but most of the reported suspect parts are not ICs but simpler parts such as diodes, optoelectronics, resistors, and inductors. Murata is rising on this list primarily due to increased reporting of ceramic capacitors.

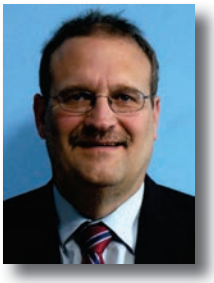
SUMMARY AND PATH FORWARD

Counterfeit electronic parts continue to be reported at a high volume, although this trend may be decreasing somewhat. Counterfeiters continue to fake complex parts such as microprocessors and memory, and in particular, Xilinx parts. Industrial and military temperature range parts are the most popular. In addition, counterfeiters appear to be expanding into low complexity discrete parts like capacitors. These small parts are often easier to counterfeit because they may be unmarked and data sheet characteristics may be difficult to verify.

To minimize the risk of counterfeit parts, it is important to purchase all electronic parts from the authorized supply chain whenever possible. It is also critical to perform adequate authentication testing on electronic parts purchased from unauthorized suppliers. SAE standards such as AS5553, AS6081, and AS6171 can provide guidance. Visual inspection is still the most common detection method for counterfeit electronic parts, but no single test is 100 percent effective. Additional inspections and tests that use solvents, x-ray, scanning electron microscopy, electrical test, and other methods should be part of a robust authentication process.

The industry needs to look toward expanding the available suite of inspections and tests. For example, testing of capacitors might need to include temperature testing or voltage verification. We should aggressively pursue novel authentication methods such as "side channel" electrical testing as a means to identify variations within a part lot without having to perform a complete functional test. Only by continuing to search for improved methods can we hope to stay ahead of advancing counterfeiting skills.

ABOUT THE AUTHOR



Fred Schipp received a B.S. degree in electrical engineering from Rose-Hulman Institute of Technology in 1983 and has 35 years of electronics experience in the military and automotive industries. He currently works at Naval Surface Warfare Center (NSWC)—Crane Division, in Crane, Ind. He has focused almost exclusively on counterfeit electronic parts since 2010, helping to generate anti-counterfeit policy, processes, and training for NSWC Crane, Naval Sea Systems Command, and the Missile Defense Agency. He is a frequent presenter at national anti-counterfeiting conferences.

NOTEWORTHY NEWS

ITC 2018 CO-LOCATED WITH ISTFA 2018

The International Test Conference (ITC) will be held **October 30 to November 3** at the Phoenix Convention Center in Arizona. This year's event will be co-located with ISTFA, providing a shared exhibition and networking events for all attendees. ITC is the world's premier conference dedicated to the electronic test of devices, boards, and systems and covers the complete cycle from design verification and validation, test, diagnosis, failure analysis, and back to process, yield, reliability, and design improvement. At ITC, test and design professionals can confront the challenges the industry faces and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

ITC, the cornerstone of TestWeek events, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including formal paper sessions, tutorials, panel sessions, case studies, a lecture series, commercial exhibits and presentations, and a host of ancillary professional meetings.

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ULTRASONIC BEAM INDUCED RESISTANCE CHANGE

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INTRODUCTION

Photon emission microscopy (PEM) is a powerful tool used to locate failures in semiconductor devices by detecting light emissions. However, detection is not possible if the device is embedded inside the package. Therefore, the mold package must be removed before performing detection. Although lock-in thermography (LIT) can detect the signal propagating through the package mold, the signal spreads under the influence of thermal diffusion through the mold resin and makes failure point identification difficult. Infrared optical beam induced resistance change (IR-OBIRCH) detects the resistance change that takes place when the substrate with biased wiring is stimulated by an infrared laser beam. It is used to find leakage current paths and contact area failures in semiconductor devices.[1] However, this technique requires mold decapsulation because the infrared laser does not propagate through a package mold that is optically nontransparent.

Ultrasound, generally defined as sound waves higher than 20 kHz, is widely used in medical and industrial inspections. In the field of semiconductor devices, ultrasound is often used to detect detachments and cracks in semiconductor packages.[2,3]

Researchers have developed a new technique for package failure analysis on wiring defects using ultrasound without mold decapsulation. The wiring in the chip within the package is stimulated by ultrasound. The role of ultrasound is similar to the infrared laser beam in IR-OBIRCH, as they both provide a heating effect. However, the ultrasonic beam induced resistance change (SOBIRCH) method does not require mold decapsulation because ultrasound can propagate through a package mold that is acoustically transparent. The resistance change that occurs as a result of the heating effect is subsequently detected by an amplifier. Figure 1 shows the comparison between IR-OBIRCH and SOBIRCH.

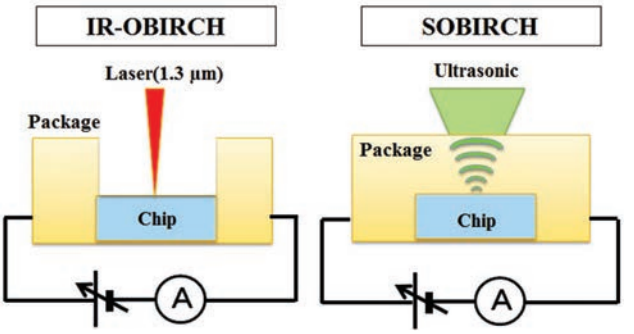


Fig. 1 Comparison of IR-OBIRCH and SOBIRCH.

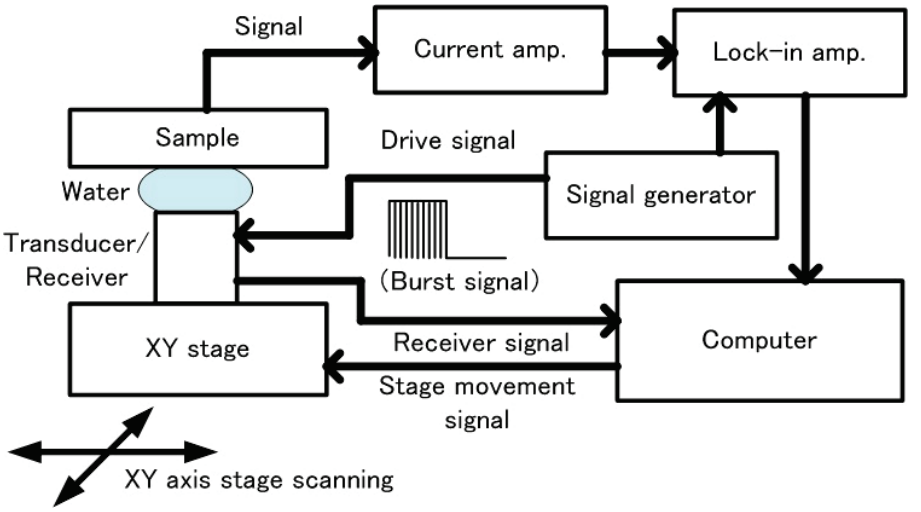
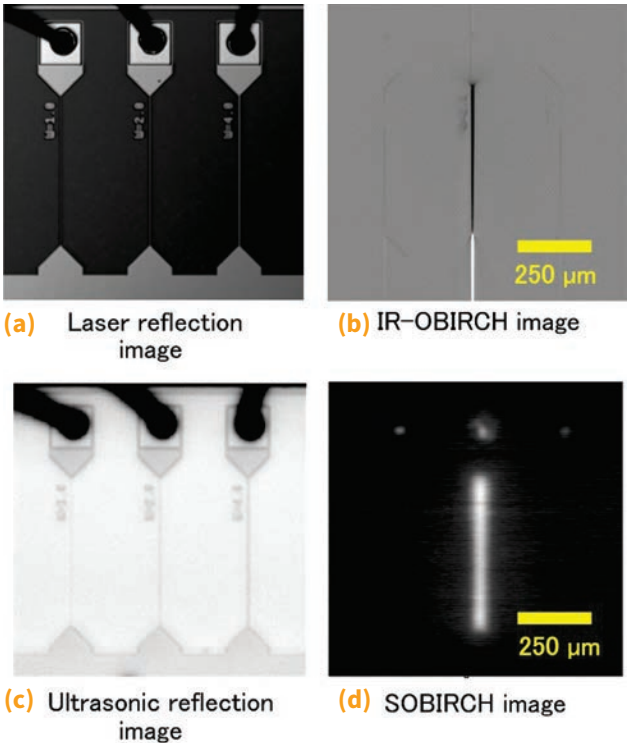


Fig. 2 Schematic diagram of experimental system.

EXPERIMENTAL SYSTEM

Figure 2 shows a schematic diagram of the experimental system. The transducer, driven by a signal generator with a burst signal, generates an ultrasonic wave for stimulation. The signal generator provides the reference signal for the lock-in detection as well. Only 40 and 80 MHz transducers are employed in this research. The transducer and sample are acoustically coupled using water droplets as a medium. A voltage is biased to the sample. The current amplifier measures the current change in the wiring due to the ultrasonic stimulation, and this change is detected by the lock-in amplifier. Because the output of the lock-in amplifier depends on lateral positioning, a 2D profile of the localized failure is created by scanning the transducer along the *x* and *y* axes. An ultrasonic reflection image is acquired prior to this step.



(a) Laser reflection image (b) IR–OBIRCH image

(c) Ultrasonic reflection image (d) SOBIRCH image

Fig. 3 IR-OBIRCH and SOBIRCH images of 2 µm wiring width.

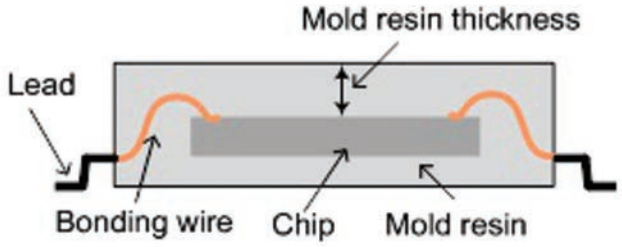


Fig. 4 Structure of wiring sample with mold resin.

BASIC DETECTION METHODOLOGY

EXPERIMENT ON A WIRING SAMPLE WITHOUT MOLD RESIN

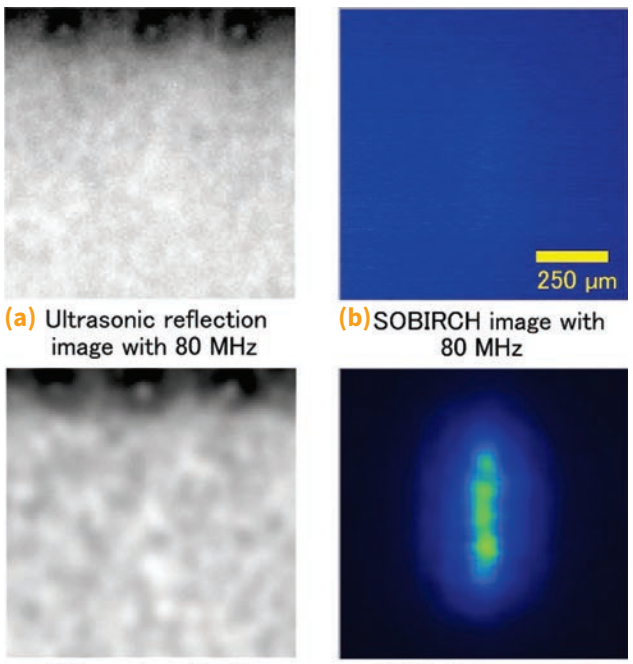
The test sample is a chip with varying aluminum wiring widths of 0.6, 1, 2, 4, and 8 µm. Length is 500 µm. Figures 3a and 3c show the laser and ultrasonic reflection images respectively. IR-OBIRCH was acquired using a 1.3 µm wavelength laser. The transducer frequency and lock-in modulation frequency for SOBIRCH was 80 MHz and 1 kHz, respectively. The bias condition was 500 mV in both experiments.

Figures 3b and 3d show measurement images by IR-OBIRCH and SOBIRCH methods at 2 µm wiring width. It is evident that both methods could detect the signal from the 2 µm wide wiring.

EXPERIMENT ON A WIRING SAMPLE WITH MOLD RESIN

Another wiring sample, sealed with mold resin, was subjected to SOBIRCH inspection. Figure 4 shows a diagram of the sample structure. The sealant is an epoxy resin comprised of a filler with an average particle size of 16 µm in diameter. Multiple samples with varying resin thickness of 305, 320, 420, 620, and 1000 µm directly on top of the chip were studied.

Figure 5 shows images where the wiring width and resin thickness were 2 µm and 305 µm, respectively.



(a) Ultrasonic reflection image with 80 MHz (b) SOBIRCH image with 80 MHz

(c) Ultrasonic reflection image with 40 MHz (d) SOBIRCH image with 40 MHz

Fig. 5 SOBIRCH image with 305 µm mold resin using 40 and 80 MHz transducers.

Ultrasound frequencies of 40 and 80 MHz were explored. The bias voltage was 500 mV and the modulation frequency was 1 kHz. It was discovered that the signal with a 2 µm wiring width could be successfully detected when the carrier frequency was 40 MHz; however, no signal was detected with an 80 MHz carrier frequency. Figure 6 shows images of samples with different resin thicknesses using 40 MHz in carrier frequency. Figure 7 shows the signal-to-noise (S/N) ratio of this measurement. A reduction in S/N ratio occurs with increasing resin thickness; however, it is remarkable that the signal could be detected even with 1000 µm thick resin mold. Figure 8 compares the SOBIRCH and LIT results under the same mold thickness of 320 and 620 µm. The bias voltage was 200 mV and the modulation frequency was 5 Hz in LIT images. Under the influence of the mold's thermal diffusion, the heat point wiring spread to the extent that at 620 µm, localization becomes impossible.

Researchers subsequently confirmed the detection sensitivity on different bias voltages using the 305 µm thick resin sample. The bias voltage was varied from 10 to 250 mV. Figure 9 shows the observed SOBIRCH images.

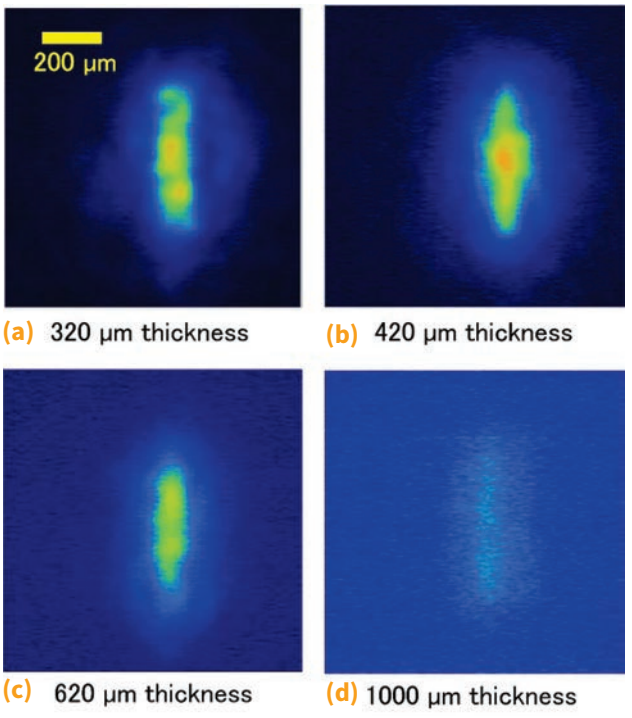


Fig. 6 **SOBIRCH images with different mold resin thickness.**

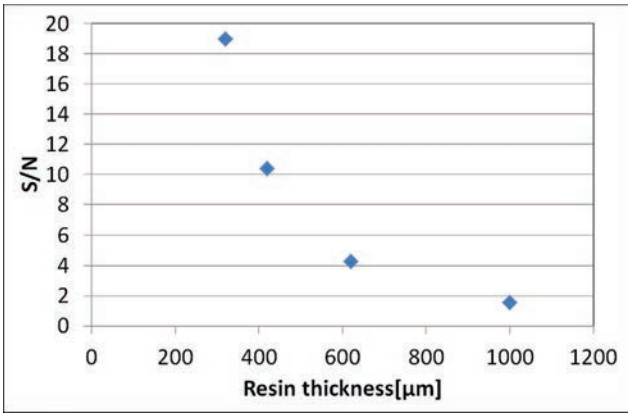


Fig. 7 **S/N for resin thickness.**

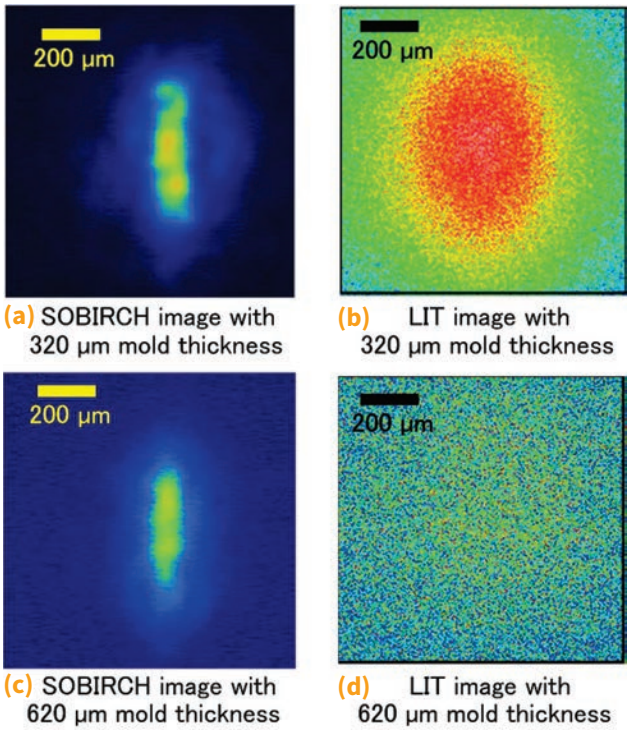


Fig. 8 **SOBIRCH and LIT image of sample with mold resin.**

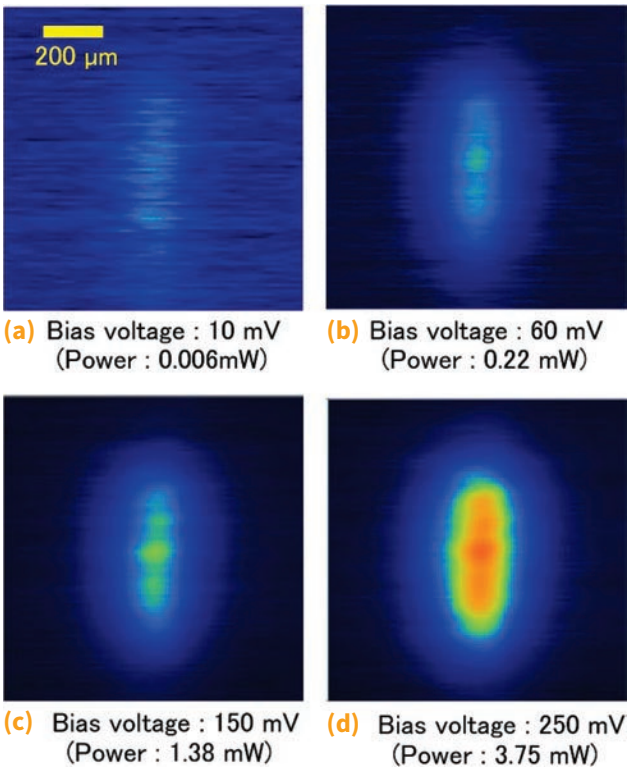


Fig. 9 **SOBIRCH images with different bias voltages.**

Although the signal is weak at 10 mV bias voltage, it is discernable. Figure 10 shows the S/N.

CASE STUDIES OF ACTUAL FAILURES

SAMPLE DESTROYED BY ESD

A case study was conducted on a microcontroller sample destroyed by ESD between VDD and VSS. The sample was a QFP package without mold decapsulation. The mold resin thickness above the top of the chip was about 600 µm. The frequency supplied to the transducer was 40 MHz. The bias voltage was 100 mV for whole chip low magnification imaging and 200 mV for high magnification zoom-in on the localized signal. The modulation frequency was 1 kHz. Figure 11 shows the ultrasound reflection image and SOBIRCH signal of the entire chip. The SOBIRCH image shown in Fig. 11b indicates signs of stimulations on the right edge of the chip. Figure 12 shows the zoom-in images of the localized signal. During physical failure analysis, a defect was found at the exact location of the SOBIRCH signal. Therefore, SOBIRCH successfully localizes without mold decapsulation.

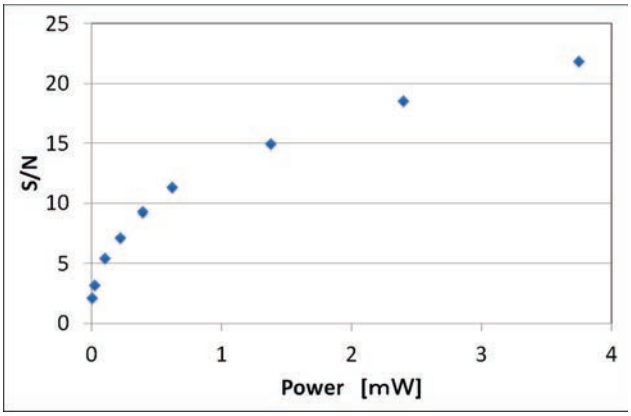


Fig. 10 S/N for power on the sample.

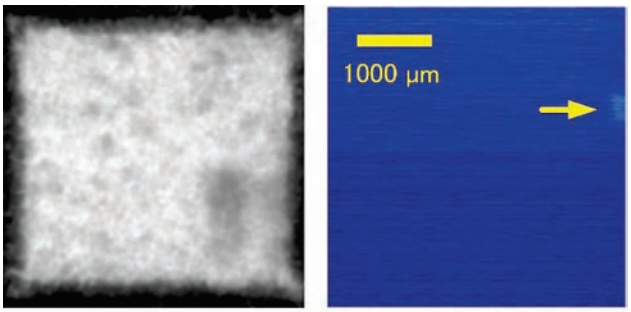


Fig. 11 Images of whole chip.

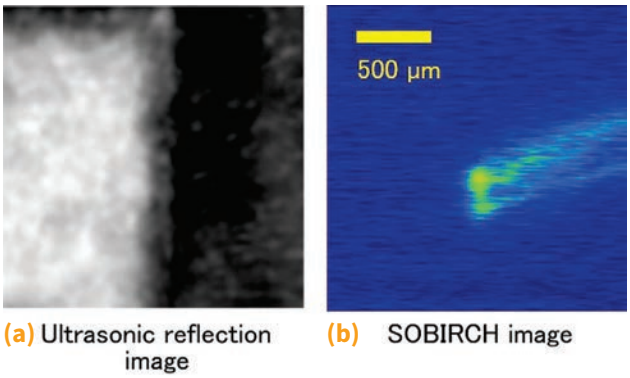


Fig. 12 Zoom-in images of localized region.

ABNORMALITY IN VDD AND VSS

A second case study compares SOBIRCH and IR-OBIRCH. A similar microcontroller sample in a QFP package without mold decapsulation was used. For this sample, a failure in VDD and VSS was observed on a tester. The mold resin thickness was about 500 µm. The carrier frequency was 40 MHz and the bias voltage was 200 mV. Figure 13 shows the ultrasound reflection image and SOBIRCH signal of the entire chip. After SOBIRCH, the sample was subjected to mold decapsulation and was observed by IR-OBIRCH. Figure 14 compares the IR-OBIRCH and SOBIRCH signal images and shows that SOBIRCH successfully acquires the same signal as the IR-OBIRCH image, even without decapsulation. Subsequent physical failure analysis found a short caused by a chip crack, as indicated by the red circle in Fig. 14b. This result further confirms the effectiveness of SOBIRCH.

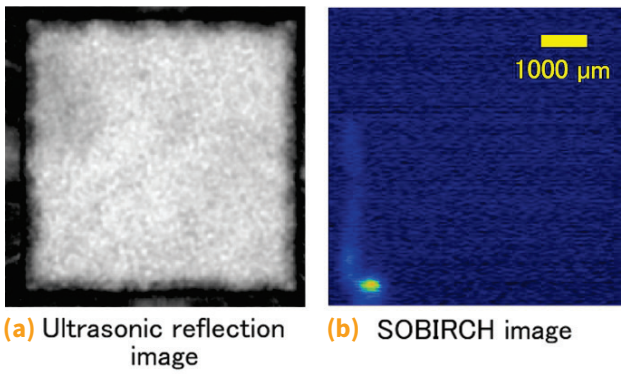


Fig. 13 Images of whole chip.

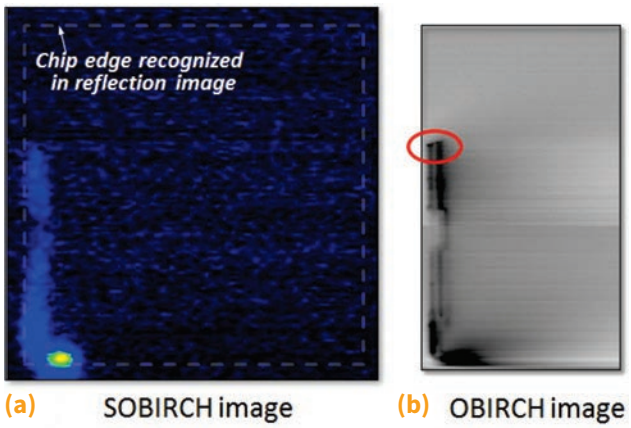


Fig. 14 SOBIRCH and IR-OBIRCH images.

APPLICATION TO A MULTILAYER SAMPLE

As proof of concept, an evaluation was performed on a multilayer test chip using a 40 MHz transducer. Figure 15a shows the sample structure. It consists of a first wiring sample layer followed by a stack layer comprised of die attachment paste (DAP), silicon, and 1 µm thick aluminum. The thickness of silicon is 60 µm and the thickness of DAP is 30 µm. The wiring on the first layer has a length of 500 µm and width of 4 µm. This stack layer repeats to form the multilayer architecture as shown in Figs. 15b and 15c.

SOBIRCH results are shown in Fig. 16. This method is able to detect the wiring resistive signals at the first layer, even with three stacked layers above.

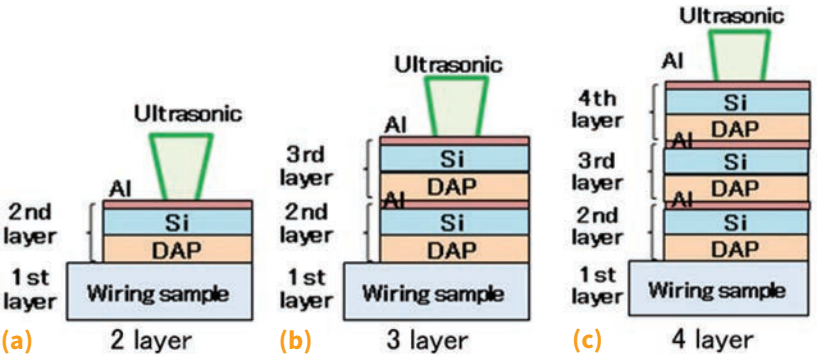


Fig. 15 Structure of multilayer chip sample.

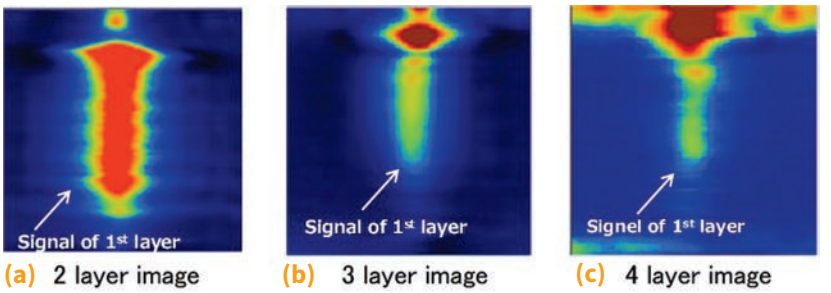


Fig. 16 SOBIRCH images of multilayer chip sample.

CONCLUSION

Instead of using light stimulation based on conventional IR-OBIRCH, ultrasound stimulation is proposed as an alternative. The basic principle of resistance change is similar. Although the lateral spatial resolution is not as defined as IR-OBIRCH, the biggest advantage of SOBIRCH lies in its ability to stimulate internal wiring through the mold resin. The series of studies presented in this article prove its effectiveness to detect a resistance change in metal wiring through the package mold upon ultrasound stimulation. The feasibility for multilayer sample application is further substantiated. Additional enhancements to the approach along with detailed evaluations of actual failed samples are now in progress. The ultimate goal is to improve this novel failure analysis technique.

ACKNOWLEDGMENT

The authors would like to thank Yoshikazu Matsumoto, Renesas Engineering Services, for sample preparation and Dr. Naohiro Hozumi, Toyohashi University of Technology, for support of this article.

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ABOUT THE AUTHOR



Toru Matsumoto received B.E. degrees in image science from Chiba University, Japan, in 1988. He joined Hamamatsu Photonics K.K. in 1988 and worked on the development of the inspection system using image sensors. Since 2004, he has been working on the development of failure analysis systems for semiconductor devices. Matsumoto developed the scanning laser SQUID microscope, laser THz emission microscope (LTEM), and nano electrostatic field probe sensor (NEPS) for failure analysis. He also initiated development of the failure analysis system using ultrasonic stimulation discussed in this article.



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LOCATING FAILURES IN CURRENT DEVICE NODES: EBIC/EBAC, CURRENT IMAGING AND NANOPROBING

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INTRODUCTION

The ever-decreasing line widths in modern semiconductor products, required for delivering higher performance devices that consume less power, can create new challenges for process ramps and yield management. Electrical fault isolation (EFI) is an important tool for locating faults. Once the general region of a fault has been identified, nanoprobing is often used to precisely locate the fault. Next, further analysis of the fault's root cause is performed, e.g., by preparing a site-specific transmission electron microscopy (TEM) section.

As semiconductor nodes get smaller and smaller, there is an increased need to move a large portion of EFI to scanning electron microscopes (SEMs) or combined focused ion beam (SEM/FIB) tools. Prior to moving into SEM or FIB/SEM, samples are typically processed on other test platforms using an array of analysis methods to locate the region of interest (ROI) on the sample—one such method is optical beam induced resistance change (OBIRCH). The scanning electron beam is mainly used to generate images of the sample surface—for device inspection or to assist in landing probe tips for electrical measurements. The FIB can be used to remove or deposit material. This can be useful for preparing TEM slices for further analysis or for modifying circuits in-situ.

EBIC AND EBAC

When imaging the sample, the electron beam will penetrate the sample surface where it can interact with the conducting lines in the device layers. When using probe tips strategically placed on contacts on the sample surface, combined with a highly sensitive amplifier, these induced currents can be recorded and visualized by feeding the recorded current back to the microscope. In this manner, an image is generated of the currents flowing throughout the conducting lines that the probe tip is in contact with.

The electron beam induced current (EBIC) imaging technique[1,2] reveals the location of P-N junctions and the quantitative amount of current flowing to and from them. EBIC imagery is generated by reading a low current signal from the sample—thus a well shielded, low-noise lead is required from the probe tip (that is in contact with the sample) all the way to the EBIC amplifier. Using this type of signal lead, the current induced by the electron beam can be recorded, amplified, converted to a voltage, and fed back into the SEM where it is registered as an auxiliary detector signal. Thus, the EBIC signal is generated within the microscope's control software and can be superimposed on the secondary electron (SE) image for easy identification of the ROI. A schematic of EBIC image generation is shown in Fig. 1.

A similar approach, known as electron beam absorbed current (EBAC) or resistive contrast imaging (RCI),[3] can be used to reveal conductive areas that are buried in the device layers while contacted to the probe tip via a pad on the sample surface. If the current path exhibits an "open" defect, the resulting EBAC image shows an abrupt change in contrast. In the case of a "resistive open" defect, a gradual contrast change is observed. This change in

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contrast represents a shift in current flow through the conductor. Typically, an abrupt contrast change is observed on "hard" open failures and a gradual contrast intensity change is observed on marginal or "soft" open failures.

CURRENT IMAGING

Another complementary method for measuring current flow inside a sample is current imaging (CI). This method employs a probe tip that is brought into contact with the sample. With the tip gently touching the surface, it is scanned over the area of interest in a line-by-line fashion. The tip can be biased to a given voltage and the current flow to bulk is recorded for each scan point. Once the tip is in contact with the sample, the electron beam can be blanked, thus minimizing contamination of the sample surface as well as the probe tips. The obtained data is recorded and used to generate a map of current flow in the scanned area.

As semiconductor samples are flat by nature and the scanned area is comparatively small, the experimental setup can be greatly simplified by foregoing the use of AFM-based methods. The simplicity of this approach allows the operator to choose any of the available probe tips—up to eight using the Prober Shuttle—to act as the scanning tip. Additionally, any of the available probe tips or the sample bulk can be configured either as voltage source or current sink. It is also possible to scan the bulk under a stationary tip. This allows the operator to specifically search for certain artifacts or faults. For example, a leaky gate will produce a current response during the CI sweep if the sample bulk is configured as the current sink, where healthy transistor gates will not show a response on the current map.

A beneficial side effect to the sweeping motion used in the CI technique is that this gentle scrubbing action can be used to remove surface contaminants from the sample, thus providing a clean surface for subsequent probing experiments.

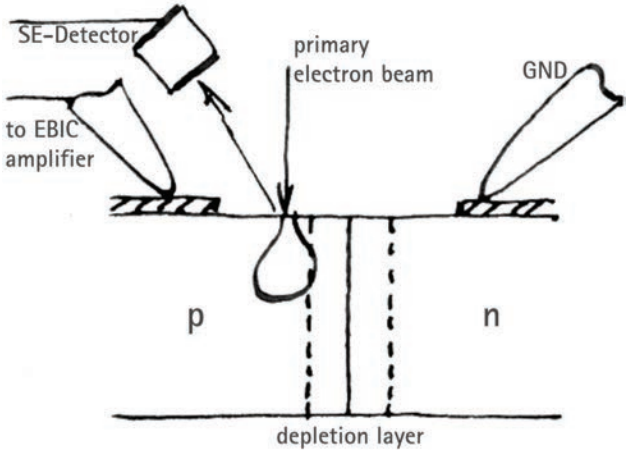


Fig. 1 **EBIC signal generation.**

INSTRUMENTATION

The experiments described in this article were performed using a Kleindiek Nanotechnik Prober Shuttle. This platform is available in two sizes: 100 mm diameter for up to four probes and 140 mm diameter for up to eight probes. Probes are positioned using piezo motors for high stability and positioning accuracy. The Prober Shuttle's low profile allows for inserting the platform via a suitable load lock as well as imaging at very low working distances. The latter is especially important when using low acceleration voltages. The probing system can be enhanced with an array of measurement tools and control software. Notably, the EBIC/RCI amplifier described above was used on the experiments discussed here. Additional modules, such as the CI option, are described below.

FAILURE ANALYSIS CASE STUDIES

CASE #1: LOCATING RESISTOR CHAIN DEFECTS

The device under test (DUT) in this case consisted of a continuous contact chain between silicided N-active islands and the metal 1 layer manufactured in 28 nm technology. In the first case, this chain exhibited a high ohmic link failure that was found during in-fab electrical testing. It exhibited increased resistance of the entire resistor chain. The EBAC technique was employed by placing a probe tip at each end of the resistor chain, while routing one probe tip to ground and the other to the EBAC amplifier. While the electron beam is swept across the sample surface, the resulting EBAC signal is displayed on the microscope screen, revealing the location of a high-ohmic link in the via chain (Fig. 2). A subsequent site-specific

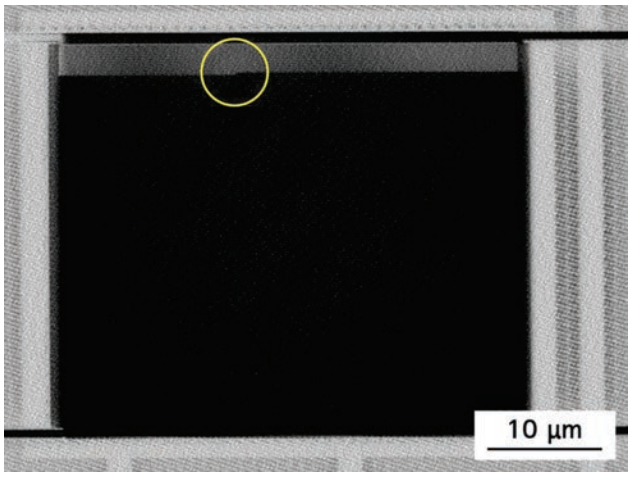


Fig. 2 **EBAC result on resistor chain. The yellow circle indicates the fault's location.**

TEM analysis revealed the root cause: The tungsten plug penetrates the nickel silicide layer due to a hole in this layer (Fig. 3).

CASE #2: INCREASED SUBSTRATE LEAKAGE

Corner experiments of the contact etch process showed that contacts had punched through the SiGe interlayer system (Fig. 3). Current imaging was performed in order to characterize the electrical impact caused by this defect. Additional transistor probing experiments were performed to confirm the CI results.

The test structure consists of a continuous contact chain between silicided P-active island with a SiGe interlayer and metal 1. The vertical contacts are tungsten plugs with a TiN diffusion barrier layer. The SiGe interlayer system belongs to the strain engineering features of PMOS transistors in modern technologies. For the purpose of the experiment, the wafer was taken from production before metal 1 processing in order to have the contacts at the sample surface. The image generated when applying a bias of –1.5 V to the sample while reading the current at the probe tip showed contacts of very similar brightness (Fig. 4).

In contrast, applying a bias of +1.5 V to the sample while scanning the same area reveals notable differences in the brightness of various spots, i.e., their current response (Fig. 5).

Using the detailed scan shown in Fig. 5 (bottom), the probe tip can be positioned on the various contacts without the need to un-blank the electron beam. This helps to reduce the sample's exposure to the electron beam and thus minimize surface contamination.

Using the needle already in contact with the sample, IV measurements were performed on two of the contacts—one showing a strong current response and one showing a weak response. The obtained IV curves show

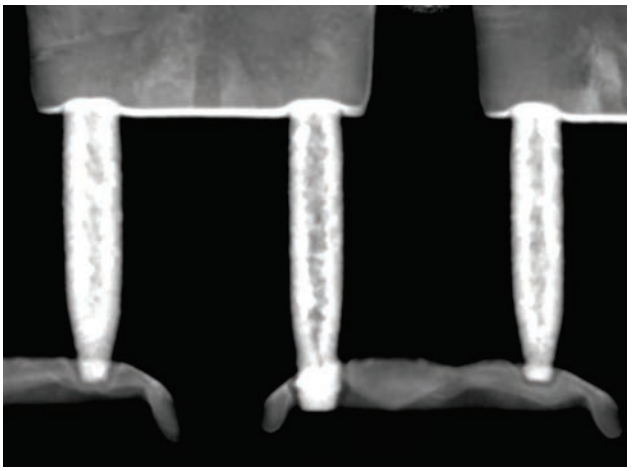


Fig. 3 **TEM analysis of fault in via chain showing a punch through the SiGe interlayer system.**

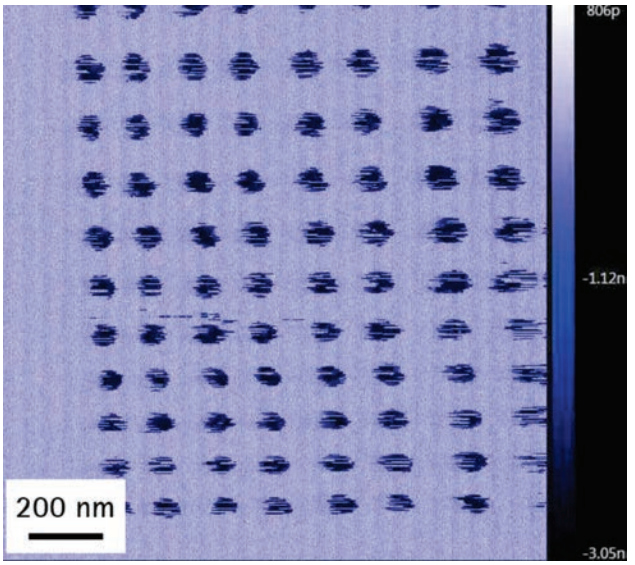


Fig. 4 **Sample bias -1.5 V.**

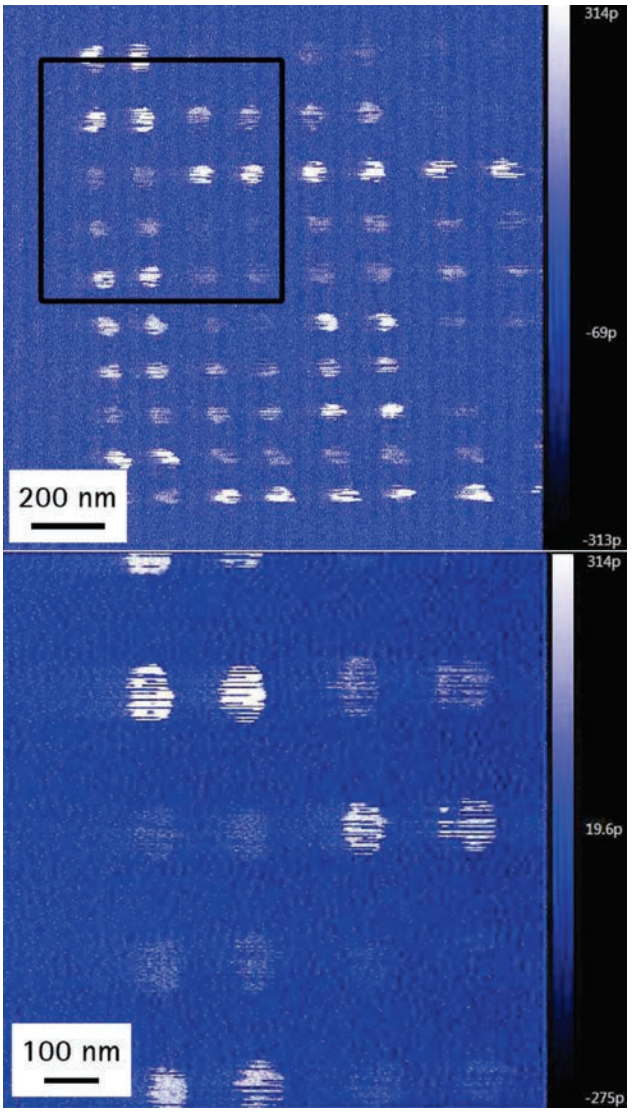


Fig. 5 **Sample bias 1.5 V (top), zoomed area (bottom).**

the same result as the scans: Applying a positive voltage to the tip results in a similar current on both contacts, while applying a negative voltage to the tip shows a strong discrepancy in the resulting current, depending on which contact is being observed.

Further investigations including site-specific TEM analyses and subsequent energy-dispersive x-ray (EDX) investigations were performed to elucidate the root cause for the observed phenomena. Results indicate that the increased leakage is related to the penetration depth of the contacts through the SiGe-interlayer region and corresponding implants (Fig. 6).

CASE #3: BACK END OF LINE (BEOL) OPEN ISSUE ON COPPER PLATING RECIPE DEVELOPMENT WAFER

After an environmental stress test, a metal-7 via chain from a copper plating recipe development wafer failed (open) and was analyzed. The failing via chain process monitor structures did not show passive voltage contrast (PVC) signals during the fab in-line electron beam inspections. The same condition was observed when both PVC and active voltage contrast (AVC) were conducted on the device in the SEM (Fig. 7).

The "high resistance" open failures on the via chain structure at metal 7 was isolated using the SEM in-situ RCI/EBAC technique. The gradual change in resistance (contrast) was observed at the defect site (white arrow) when the sample was scanned with the SEM beam voltage of 2kV, beam current of 6.4 nA, and scan rate of 30 µs (Fig. 8). The same signal was enhanced when the signal polarity was swapped on the macro structure (Fig. 9).

FIB cross sections of the RCI site showed varying

(continued on page 30)

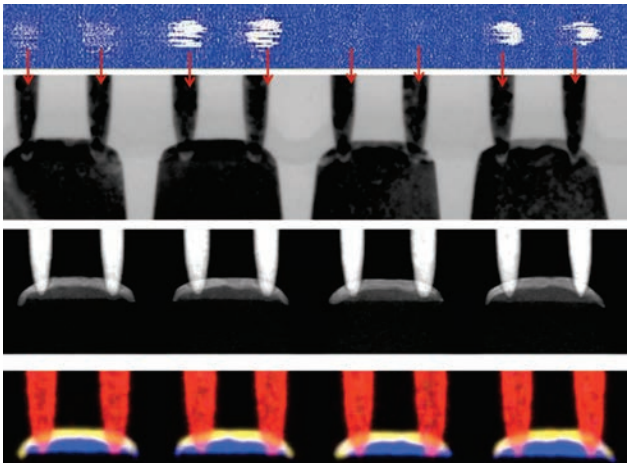


Fig. 6 **TEM and EDX analyses of various contacts exhibiting different current responses (red: W, yellow: Ni, and blue: Ge).**

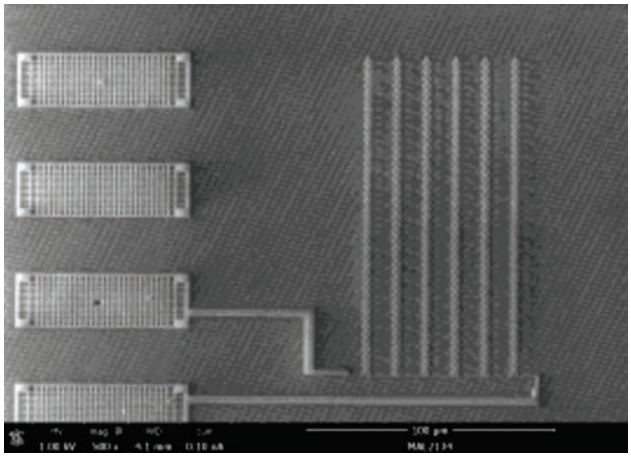


Fig. 7 **No contrast change was observed when in-situ SEM PVC and AVC analyses were done on the via chain structures at metal 7. One of the pads was grounded by milling a 1 × 10 µm hole in the pad.**

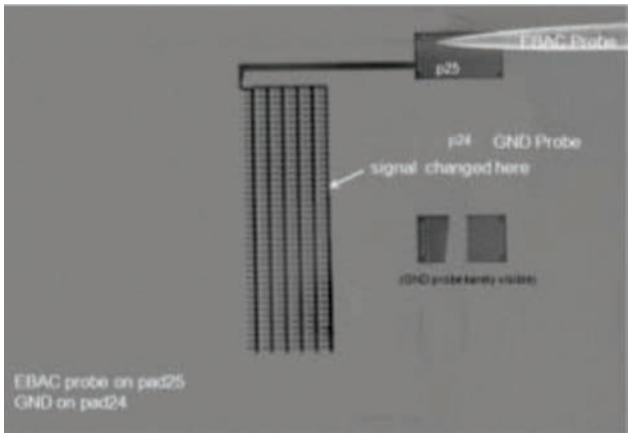


Fig. 8 **The RCI/SEM overlay image of the via chain process monitor test structure at metal 7 with the RCI amplifier probe (visible) on pad 25 and ground probe (not visible) on pad 24. The via chain structure shows a gradual contrast change at the defect site (white arrow) when analyzed.**

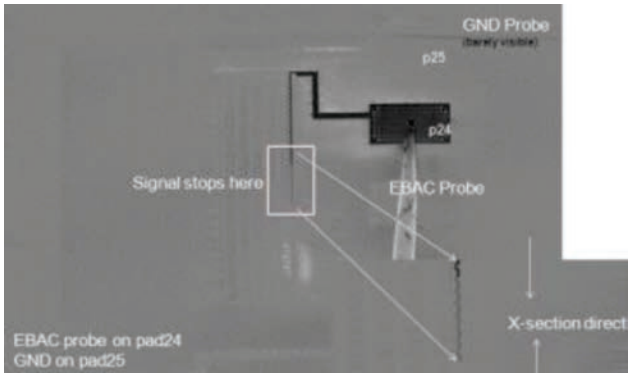
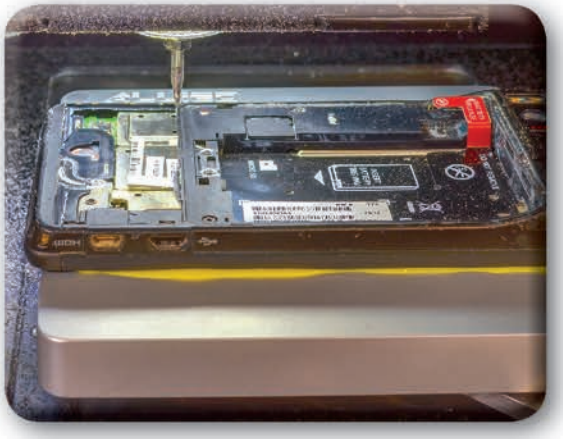


Fig. 9 **RCI/SEM overlay image of test structure with RCI probe (visible) on pad 24 and pad 25 grounded (not visible). Contrast change was more pronounced when the bias polarity was reversed on the structure.**

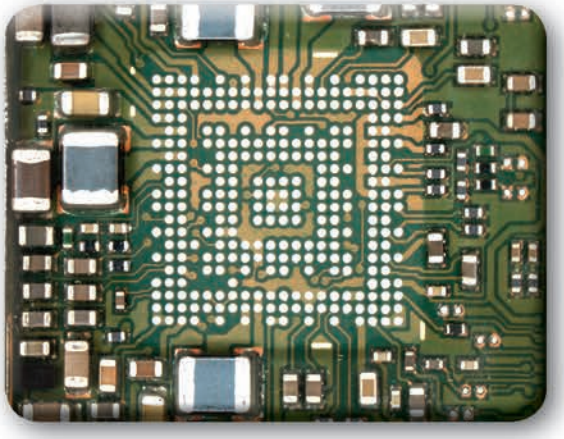
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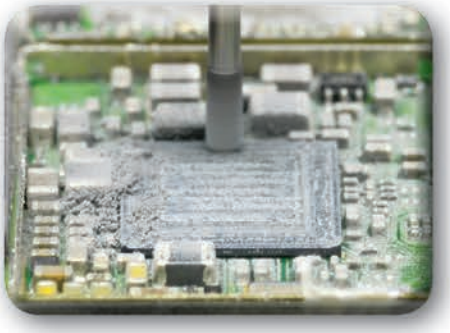
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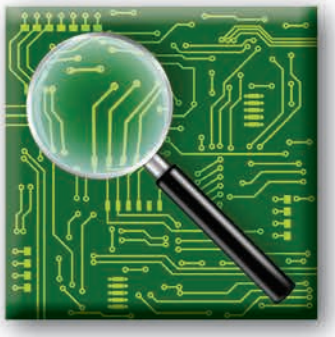
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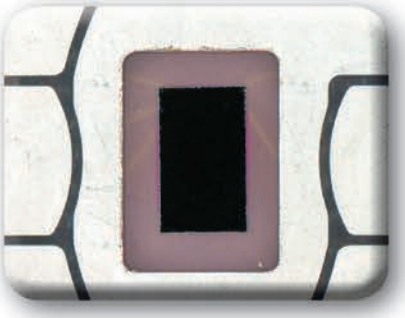




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LOCATING FAILURES IN CURRENT DEVICE NODES *(continued from page 27)*

degrees of metal voids along the high resistance path on the lower level metallization. The vias appeared to be intact and free of voids (Figs. 10, 11).

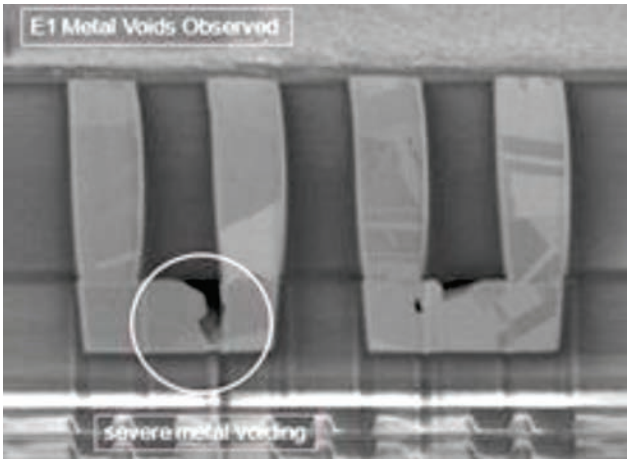


Fig. 10 FIB cross-section SEM image of RCI site where metallization started showing partial metal voids in lower Cu metal line.

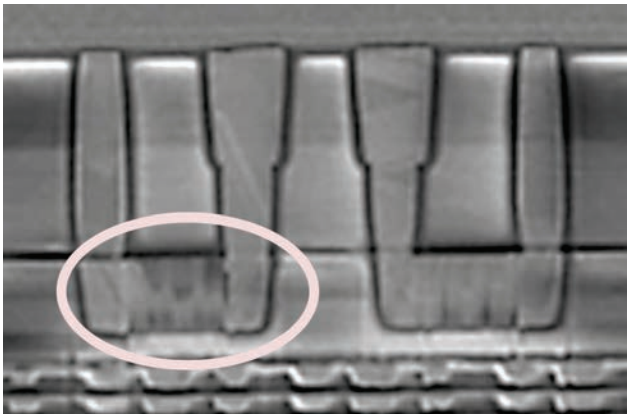


Fig. 11 Further FIB cross-section shows where the metal line was almost completely "open." Throughout the cross-sections, the vias appear to be intact. The issue was isolated to the copper plating process.

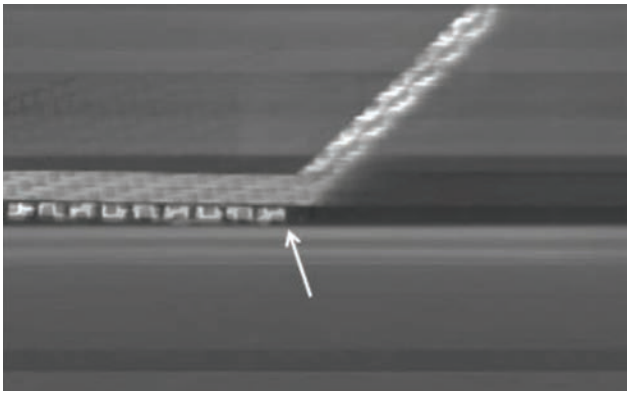


Fig. 12 Health of line metal stack test structures on the guard ring. Initial PVC analysis did not show obvious contrast change in the structure of interest (guard ring), so RCI analysis was done at the top metal layer. RCI signal observed at 2 kV and 26 nA.

CASE #4: BEOL OPEN FAILURES DUE TO MISSING VIA ON HEALTH OF LINE WAFERS

Defect localization using RCI was conducted on a health of line (HOL) wafer at metal 9 with the metal stack (in guard ring) failing for "open." Figures 12 and 13 illustrate the SEM/RCI overlay images obtained when the device at metal 9 was scanned in the SEM with a beam voltage of 2kV and beam current of 26 nA. FIB cross-sections of the EBAC/RCI site at metal 9 showed the "open" failure was due to a missing via 5 in the metal stack. Initial analysis was conducted with PVC, but failed to give observable contrast change when scanned in the SEM. PVC has been known not to be less sensitive or effective in producing clear contrast change on long repeating structures.[4]

CASE # 5: FRONT END OF LINE (FEOL) SUBSTRATE MICROCRACKS

Elevated defectiveness was reported on an M1/CA/PC//RX structure. The failures were reported "open" at wafer



Fig. 13 SEM/RCI overlay image highlighting the abrupt contrast (resistance) change on the guard ring at metal 9 (white arrow). The defect was isolated at metal 6 with the missing via A5. RCI signal observed at 2 kV and 26 nA.

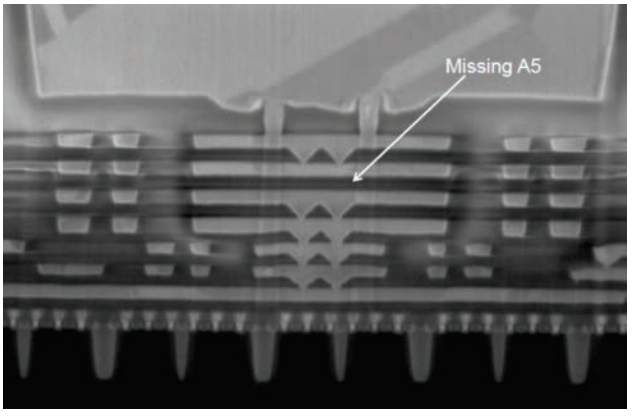


Fig. 14 FIB cross-section SEM image highlighting the missing via 5 in the guard ring at the RCI/EBAC site shown in Figs. 12 and 13.

electrical testing. Figures 15 and 16 show the analysis conducted on a process control monitor structure with long single metal 1 (M1) contact (CA) chain to active (RX) regions with dummy metal 1 lines perpendicular to the chain. The wafer was failing for "high resistive" open. The RCI data recorded at 2 kV/26 nA allowed localization of the defect site to a single M1 site.

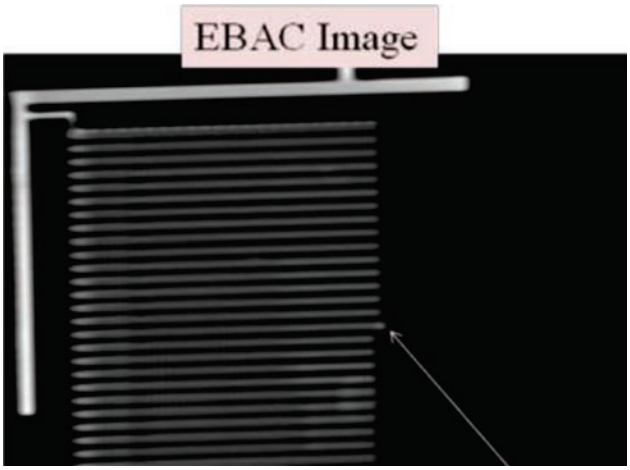


Fig. 15 Test structure composed of metal 1 contact chain to active regions with dummy metal 1 line parallel to the chain. RCI image was scanned at 2 kV and 26 nA of beam current.



Fig. 16 SEM/RCI overlay image highlighting the localized site.

FIB cross-sections of the EBAC/RCI site showed multiple microcracks below metal 1 (Fig. 17). The microcracks severed the PC (PO), RX (AA), and the shallow trench isolation (STI) below metal 1. This resulted in the observed high resistive open.

CASE #6: FEOL MICRO CONTAMINATIONS

A HOL wafer failing for CA/RX high resistive "open" was analyzed. Figures 18 and 19 illustrate the failure analysis performed on a test structure consisting of a single

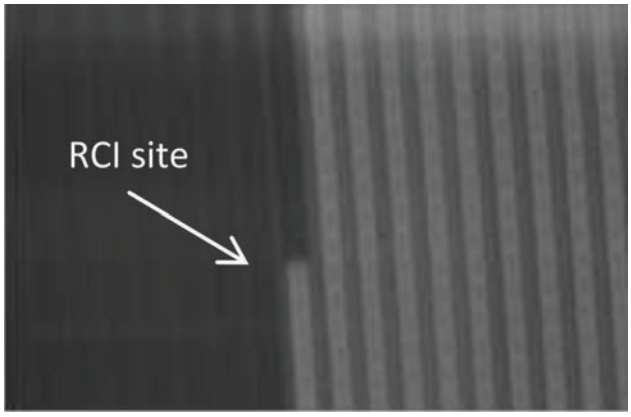


Fig. 18 Contact/active (CA/RX-AA) resistive open failure on health of line (HOL) test structure consisting of a single metal 1/contact (CA) chain to islands of active (RX-AA) regions with parallel polysilicon (PC) lines. The RCI result, recorded at 2 kV/1.6 nA, localizes the defect site on the M1/CA/PC/RX test structure.

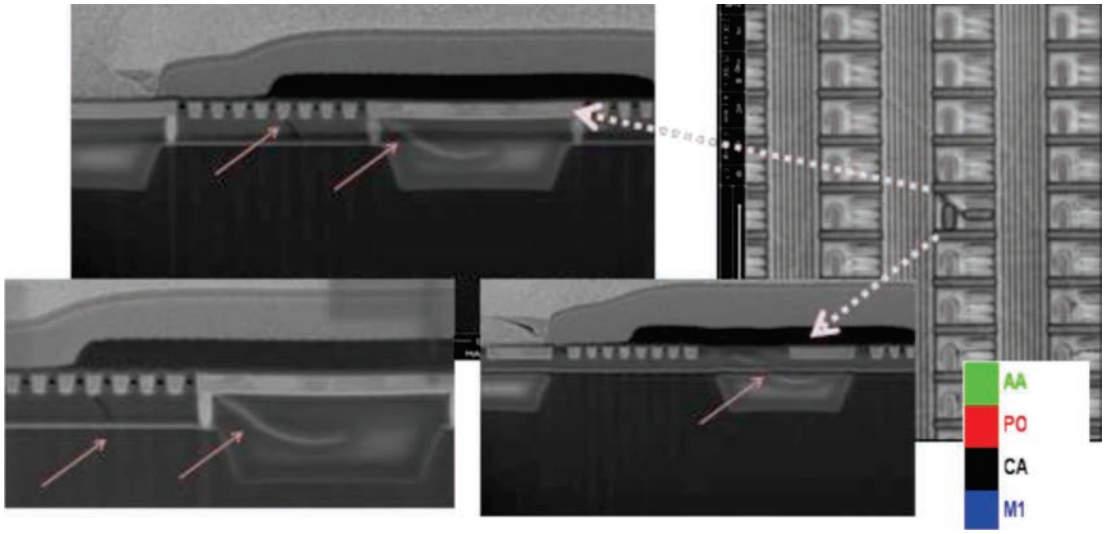


Fig. 17 SEM top-down image (top left) of the process monitor structure and FIB cross-section SEM images of the RCI site from Figs. 15 and 16 illustrating varying degrees of microcracks at the substrate layer below metal 1. Microcracks affect the active (AA), PC gate (PO), interlevel dielectric (ILD), and shallow trench isolation (STI) material.

metal 1 contact (CA) chain to islands of active (RX) regions with dummy parallel PC lines. The split lot wafer showed an elevated number of soft failures at 12 o'clock. RCI analysis at 2 kV/1.6 nA localized the defect to two adjacent contacts. The FIB cross-sections and advanced TEM analysis showed evidence of the presence of a particle between the contact and active (CA/RX) layers (Figs. 19, 20). The particle appeared to have blocked the CA etch resulting in an unlanded CA, which resulted in the observed electrical "open" failure.

SUMMARY

Advances in integrated circuit (IC) technology have made failure site localization extremely challenging. Much work has been done to effectively and rapidly detect defects on ICs during fabrication.

The nanoprober based current imaging system provides a number of advantages for SEM (or FIB/SEM) based failure analysis. Among these are easy navigation to the region of interest (using the SEM), fast and contamination-free imaging of the contacts (using CI), and the possibility of performing nanoscale probing in situ without moving to a separate tool. When combined with EBIC/EBAC/RCI, the nanoprober is equipped with additional capabilities for elucidating the root cause of common failures.

This work demonstrates that RCI is a valuable defect localization technique for "soft" or "marginal" open failures affecting the full range of process modules with defect sizes in the 20 to 50 nm range or on defects buried beneath multiple layers of metals.

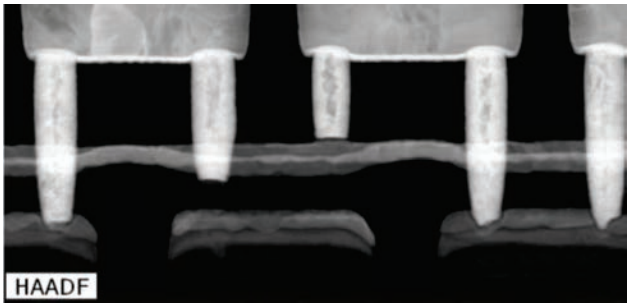


Fig. 19 High-angle annular dark-field scanning transmission electron microscopy (HAADF STEM) image of the defect site highlighting the unlanded contact.

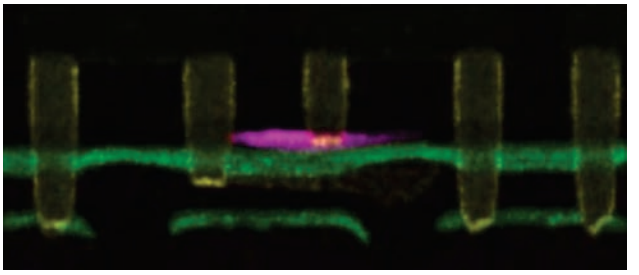


Fig. 20 Energy dispersive x-ray (EDX) map of the area shown in Fig. 19 reveals the presence of a particle between the RX and the CA layers. The particle appears to have blocked the CA etch, resulting in unlanded CAs.

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5. R. Rosenkranz, S. Doering, W. Werner, and L. Bartholomaeus: "Active Voltage Contrast for Failure Localization in Test Structures," *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2006, p. 316-320.

ABOUT THE AUTHORS



Stephan Kleindiek studied physics in Marburg and Tübingen, Germany. After a six-month visit to IBM's T.J. Watson Research Center in Yorktown Heights, N.Y., in 1994, he finished his Ph.D. in 1996 and founded Kleindiek Nanotechnik in 1997, where he now serves as CEO. He invented the Nanomotor and subsequent rotational motors, which are the foundation for his company's products.



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ISTFA/2018 PREVIEW

Efrat Moyal, ISTFA 2018 General Chair
Lattice Gear LLC
efrat.moyal@latticegear.com



"Failures Worth Analyzing" is the theme of this year's ISTFA taking place at the Phoenix Convention Center.

ISTFA HIGHLIGHTS AT A GLANCE

- Keynote 1: Transformation to automated driving
- Keynote 2: Autonomous vehicle security
- Panel Discussion: Which failures are worth analyzing
- First time co-located with the International Test Conference
- NEW interactive user group sessions

What percentage of detected failures do you analyze? If your answer is close to 100%, then come to the 44th International Symposium for Testing and Failure Analysis (ISTFA) to hear some thought-provoking and challenging perspectives from leading industry experts.

ISTFA 2018 will take place October 28 to November 1 in Phoenix. The theme of this year's event is "Failures Worth Analyzing," which aims to complement ongoing discussions on cutting costs and improving throughput by rethinking failure analysis strategies. Should we identify the most efficient workflow and equipment for hard vs. soft failures or systematic vs. random failures? How about designing a workflow that focuses on high return, high value failure analysis to maximize return on FA investments?

As we strive for a 100% success rate, do we need to analyze every failure? Or can we afford to be selective? If not, how do we prioritize and strategize? One young technology being challenged by this very question is the autonomous vehicle (AV) sector. Not only is it continually pressed to cut time and cost in its testing and FA to stay competitive, the products (AVs) also face a vast range of users, use styles, and external conditions that are impossible to predict and test for. These issues will be addressed in the keynote talk.

The ISTFA 2018 keynote will focus on AV technology, starting with "Transformation to Automated Driving" presented by Mark-Tami Hotta, who led many development programs in the automotive industry and was the CEO of the nation's leading independent automotive testing center. He will discuss several aspects of this transformation, such as its potential significance, what some of the challenges are likely to be, what the transition period may look like, and how technologies and vehicles may be tested and validated. Dr. Mark Tehranipoor, an expert in



Hyatt Regency Phoenix, the conference hotel.



A view of downtown Phoenix from 32nd Street and Lincoln. Courtesy of Visit Phoenix.

hardware security, will discuss the challenges AV faces due to today's supply chain complexity, especially in terms of security and quality issues directly impacting integrated circuits and systems. Understanding the failure mechanisms resulting from poorly designed integrated circuits or tampered and insecure systems are "worth analyzing."

This year's panel discussion will challenge FA norms regarding types of failures, including those that call for full analysis, those needing electrical failure mode signature analysis to close, and those requiring minimal time and effort. The discussion will also cover how to avoid dead ends in analysis. Experts from the automotive industry, semiconductor companies, medical device manufacturers, and packaging and assembly service providers have been invited to participate.

For the first time, ISTFA will co-locate with the International Test Conference (ITC). As an IEEE conference, ITC is dedicated to logic and memory testing of electronic devices, diagnosis, and yield analysis, and is one of the leading test conferences worldwide. Complementing ISTFA, ITC 2018 features a related theme, "AI Toward Autonomous Testing." This conference includes a solid mix of industrial contributions and academic research, especially on current topics such as automotive and artificial intelligence. Joint sessions with ISTFA and ITC highlighting topics such as diagnosis and yield will be offered. In addition, a joint expo floor represents the largest ever at ISTFA, with 30% more companies, technologies, and products to visit and explore.

Many opportunities are planned for attendees to interact face-to-face with industry experts, peers from labs around the world, and across industries. Attendees are encouraged to ask questions and share experiences during and after the technical talks. Newly designed Hybrid User Group sessions are where the "rubber hits the road" for new physical tool technologies, innovative techniques, and actual use or test cases. Attendees are encouraged to bring their work challenges to the user groups for discussion.

Take this unique opportunity to expand your knowledge, network, and develop an FA support group to advance your work, career, and professional growth.

ISTFA 2018 TECHNICAL SESSIONS

Symposium sessions will be packed with high quality, innovative, and original unpublished presentations in two tracks:

- Emerging FA Techniques and Concepts
- Future Challenges of FA
- Fault Isolation
- 3D Devices Failure Analysis
- Organic Electronics
- Wireless, Self-Powered, Sensors, MEMS Failure Analysis
- Detecting Counterfeit Microelectronics
- Alternative Energy
- FA Process
- Packaging and Assembly Level FA
- Diagnostic Testing, Scanning and Debug
- Board and System Level FA
- Metrology and In-Line Device Characterization
- Microscopy
- Circuit Edit
- Sample Preparation and Device Processing
- Scanning Probe Analysis
- Yield and Reliability Enhancement
- Nanoprobing, Electrical Characterization
- Competitive Analysis and Reverse Engineering
- FA Use Cases

ISTFA/2018

EXHIBITORS

ISTFA 2018 EXHIBITORS as of 6-26-18

BOOTH #	COMPANY
606	Advanced Spectral Technology, Inc.
407	Allied High Tech Products
130	Angstrom Scientific, Inc.
127	Anton Paar
226	Applied Beams
430	Attolight AG
428	Barnett Technical Services
721	BSET EQ
129	Buehler, An ITW Company
406	Checkpoint Technologies
114	Contech Solutions Inc.
531	Control Laser Corp.
327	DC - Digit Concept
612	EAG Laboratories
209	EDAX Inc.
208	Electron Microscopy Sciences
211	Ephemeron Labs Inc.
112	Gallant Precision Machining Co., Ltd.
314	Gatan
513	Hamamatsu Corporation
214	HDI Solutions - Hitachi
121	Herzan LLC
109	Hi-Rel Laboratories
707	Hitachi High Technologies
608	ibss Group Inc.
431	Imina Technologies SA
111	IR Labs
607	JEOL USA
215	JIACO Instruments
107	Keyence Corporation
128	Kleindiek Nanotechnik
220	LatticeGear
730	Leica Microsystems
120	Mager Scientific, Inc.
708	MASER Engineering B.V.
221	Materials Analysis Technology
415	Mentor, A Siemens Business
528	Mesoscope Technology Co. Ltd.
728	Micromanipulator
629	MicroNet Solutions, Inc.
231	Microsanj LLC

BOOTH #	COMPANY
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213	MSSCORPS Co., Ltd.
228	Nanotronics
413	Neocera LLC
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306	Nisene Technology Group, Inc.
713	Nordson Dage / Nordson Sonoscan
823	OKOS
310	Olympus
320	Oxford Instruments
807	PACE Technologies
631	Park Systems Inc.
113	PrimeNano Inc.
212	PVA TePla America Inc.
507	Quantum Focus Instruments
427	Quartz Imaging
126	Raith America, Inc.
521	RKD Engineering
420	RKD Systems
321	Robson Technologies Inc.
821	Rolink, LLC
210	Sage Analytical Lab
820	Samco Inc.
627	SELA USA Inc.
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108	SmarAct Inc.
620	SPI Supplies, Inc.
614	Synopsys
110	Ted Pella
429	TeraView LTD
307	TESCAN USA
313	Thermo Fisher Scientific (formerly FEI)
206	TMC Ametek
106	Trion Technology
621	ULTRA TEC
330	Varioscale Inc.
706	XEI Scientific
312	Yxlon FeinFocus
512	ZEISS
509	Zurich Instruments AG

ISTFA/2018

FAILURES WORTH ANALYZING

OCTOBER 28

NOVEMBER 1

2018

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Where: Selected entries will be displayed and prizes awarded October 28 - November 1 at the 44th International Symposium for Testing and Failure Analysis (ISTFA) Conference and Exposition in Phoenix.

Categories: No more than one image per person allowed in each category

I. *Color Images Only* (*Optical Microscopy*)

II. *Black & White Images Only* (*Optical Microscopy/SEM/TEM/X-Ray/UV Micrographs/Other*)

III. *False Color Images Only* (*SPM/SAM/Photon Emission/Other*)

Images will be judged on failure analysis relevance (35%), aesthetics (35%), and novelty of the technique or mechanism (30%).

Deadline: Entries must be submitted by September 1.

Entries: Submit by email to **photocontest@edfas.org** (subject line: EDFAS Photo Contest).

Format: Submissions should be made through email only, with one picture attached. Each submission must be in a standard format (PNG, JPEG, TIFF, BMP, etc.). Please provide your highest-resolution image. The preferred submission is a .jpg or .tif, five inches wide at 300 dpi resolution.

Along with the picture, the email should include the name of the submitter, category of submission, mailing address, phone, fax, email address, and a description of the micrograph (not exceeding 50 words). The picture should not have any contact information embedded.

Copyright & Permissions: Entrants are responsible for obtaining any releases or any other permission or license necessary for the submission of their work for this contest and future publication. EDFAS and ASM International will have the right to exhibit, reproduce, and distribute in any manner any or all of the entries. The entries will not be returned to the submitters.

Prizes: **1st place** in each category receives a wall plaque and one-year complimentary ASM/EDFAS membership.

2nd and 3rd places in each category receive award certificates and one-year complimentary ASM/EDFAS memberships.

The top 10 entries in each category will be displayed at ISTFA 2018 in Phoenix.



edfas.org

ISTFA/2018

PHOENIX, AZ
OCT 28 - NOV 1, 2018

FAILURES WORTH ANALYZING

2018 ISTFA FA Video Contest

ARE YOU THE NEXT SCORSESE... OF FAILURE ANALYSIS?

We hope so!

Submit your 3 minute (or less) video about an exciting result or a scintillating artifact – anything goes, as long as it relates to Failure Analysis! Your FA Community will judge them and recognize winners at this year's ISTFA during the Social Event. Show off your filmmaking skills and FA prowess!

WHO SHOULD SUBMIT?

Failure Analysts

Anyone working in the Failure Analysis field.

Students

Students currently studying in fields related to Failure Analysis (Physics, Electrical Engineering, Chemistry, Materials Science, etc.).

DISCOUNTS AND PRIZES

SPREAD THE GIFTS! ALL qualified entries WIN!
All qualified entries win an ASM T-shirt (Failure Analysis)

DISCOUNTS: Main author of qualified entries gets 15% discount during registration (to receive the video discount, please register as a presenter).

PRIZES:

- 1st Prize: 50% conference fee + plaque
- 2nd Prize: 30% conference fee + award
- 3rd prize: 20% conference fee + award

WINNING CRITERIA: Videos will be judged on creativity, originality, message, production quality, and overall presentation.

WINNERS SELECTION: Winners will be selected during the conference.

- Strictly one entry per participant. Official ballots will be available listing the titles of each entries. Name and affiliations of the voters will be required.

WINNERS ANNOUNCEMENTS: Winners will be announced 2 weeks after the conference, winning participants will be informed by emails, and the winning videos will be posted on the ASM and EDFAS websites 2 weeks after the conference.

CELEBRATION: Awards for this year's winners will be handed out during the ISTFA 2019 EDFAS membership meeting.

VIDEO REVIEW: The video entries will be reviewed as they get submitted through the deadline (October 8, 2018).

The video must be 3 minutes or less. It must be an original work and must contain only authorized content—including music, images, film clips, and other intellectual or copyrighted property.

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FIRST TIME CO-LOCATED WITH THE INTERNATIONAL TEST CONFERENCE (ITC)!

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Thermal Microscopy

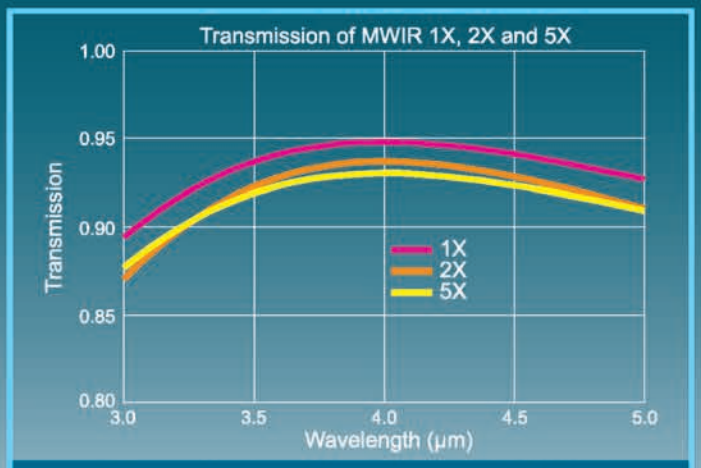
The SEMICAPS Thermal Microscopy is used in semiconductor analysis laboratories for thermal imaging to detect hot-spots. These hot-spots are often caused by electrical shorts and current leakages that are often due to the breakdown of the oxide layer. For use with all SEMICAPS platforms.



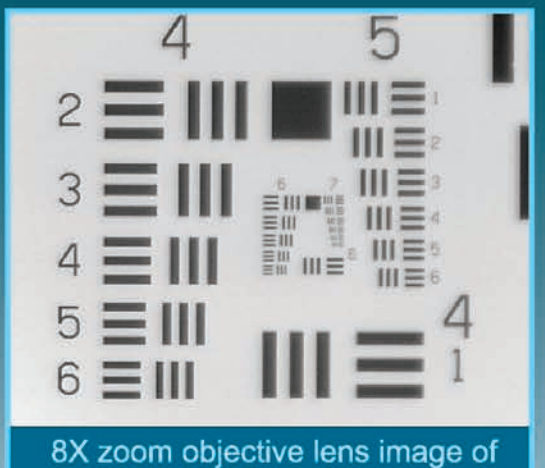
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Transmission of the standard MWIR objective lenses



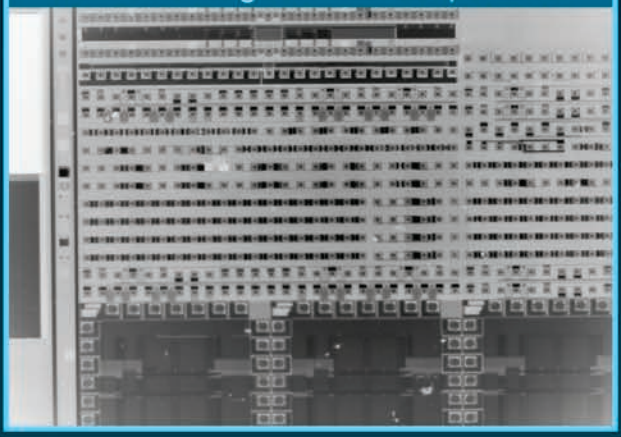
8X zoom objective lens image of USAF target; group 7 element 5 resolved 203 lp/mm

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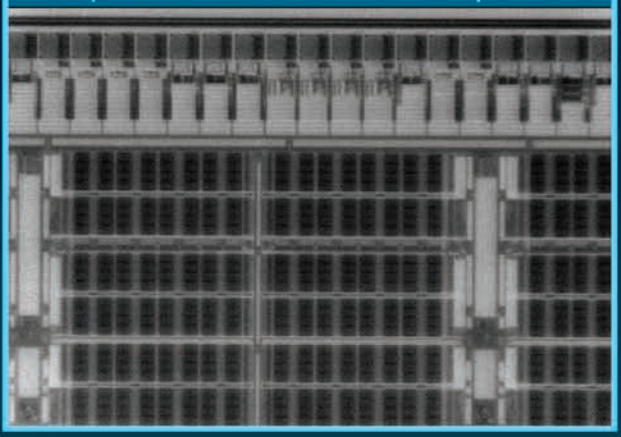
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3X zoom objective lens
front side image at room temperature



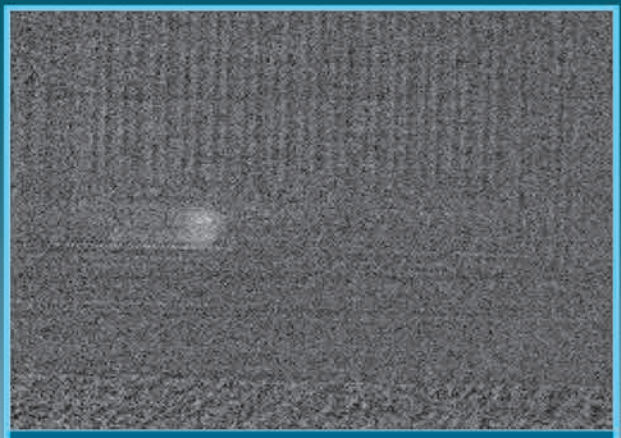
8X zoom objective lens image through
780 µm thick silicon at room temperature



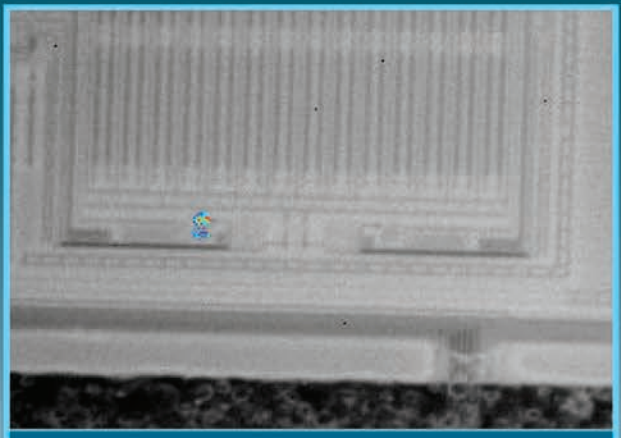
Available Objectives

	Standard			Large Format			Zoom
Magnification	1X	2X	5X	1X	3X	8X	3X to 5X
Objective NA	0.22	0.41	0.63	0.25	0.5	0.62	0.42 to 0.68
Working Distance/mm	16.5	15.7	15.2	26.6	16.7	16.7	15

These hot-spot images are conveniently overlaid onto the actual image of the IC to enable quick localization of the defects. In addition, the THM can also be used to perform thermal mapping and profiling so that engineers can determine potential regions in a working IC that may result in reliability issues.



Lock-in thermal emission image of
a hot-spot dissipating 2µW of power
(biased at 1V, 2µA).



Overlay of thermal emission
(in psedo color and after thresholding)
on the thermal background image.

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PROFILES OF CANDIDATES FOR THE EDFAS BOARD OF DIRECTORS

Cheryl Hartfield, Chair, EDFAS Nominating Committee
cheryl.hartfield@outlook.com

The EDFAS Board of Directors, during its April meeting, unanimously approved three new board members with terms beginning in 2018:

Finance Officer • 2018-2020

- Martin Keim

Members-At-Large • 2018-2021

- Renee Parente
- C.T. (Tom) Schamp

Congratulations to these new board members.



Martin Keim joined the Silicon Test Solutions Group of Mentor Graphics in 2001, now a Siemens Business, where he is currently engineering director of the Memory Built-In Self-Test and Silicon Insight team. He was an editor of the sixth edition of the *Microelectronics Failure Analysis Desk Reference,* responsible for the test and diagnosis chapters. He is currently a member of the EDFA Editorial Board and served on the EDFAS Board of Directors from 2015 to 2017. For several years, Keim volunteered on the International Symposium for Testing and Failure Analysis (ISTFA) organizing committee, serving as General Chair in 2016. He holds several national patents and is author of many technical publications. He received a doctorate in informatics from the Albert-Ludwigs University in Germany.

Vision Statement

"My vision for EDFAS is for it to be globally the number one source of information and education for every stage of a failure analyst's career. The ISTFA event grew steadily over the past years in important metrics, such as the number of attendees and paper submissions, and the size of the exposition. Driven by this premier symposium, EDFAS is doing well. This success does not hide the fact that ISTFA and EDFAS are aging. For the continued relevance of the symposium and the society as a whole, EDFAS must find a way to generate and deliver value to the society's members. EDFAS also must find a way to educate and mentor new engineers and become an important part in their journey as failure analysis leaders. In doing so, EDFAS must fully become an international society.

The majority of young engineers who can benefit from what the society has to offer are no longer confined within the boundaries of the U.S., but are in many international locations. This is especially true for the FA community in Asia. ISTFA has already recognized this need and begun programs to attract younger engineers by reaching out to universities. In order to turn these programs into a successful movement, EDFAS has to support the event in reaching out to this next generation at home and abroad. Only together can we ensure that ISTFA and EDFAS remain the most relevant resources for FA engineers in the world.

During my tenure on the EDFAS Board of Directors, I am looking forward to developing such sustained, global outreach programs for all stages of a failure analyst's career, from the young engineers at the beginning of their careers to the most senior FA leaders."



Renee S. Parente has been affiliated with AMD since 1995. She is currently a business operations manager in the Foundry Technology Organization in Austin, Texas, where she plays a dual role as a business operations leader and organizational development leader. She is responsible for capital asset management, financial forecasts, R&D organization development management, and employee engagement activities.

Parente is a strong believer in building a community through industry involvement and volunteerism. She is returning co-chair for the ISTFA panel discussion this year. In past years, she served on the ISTFA organizing

committee assisting the panel chair, attendee committee, and microscopy review committee. Parente also hosted multiple EDFAS Lonestar Chapter meetings for her organization and held positions on the AMD Technology Showcase organizational committee. She is vice chair of the AMD Austin Community Affairs Council and a member of the organization committee for AMD's Innovation Showcase, Building Leaders Initiative, Lean Six Sigma Steering Committee, and Leadership Experience.

Parente has 20 years of semiconductor process characterization and device analysis laboratory experience. Most recently, she was the AMD Austin Device Analysis lab's site lead and Physical Failure Analysis manager responsible for lab safety, PFA tools, and technique development. Prior to roles in management, she was a member of the technical staff and worked as an individual contributor in various physical analysis labs within AMD and its Motorola Alliance. Parente also was her company's corporate representative on the SEMATECH ICFAC Council (Integrated Circuit Failure Analysis Council) and served on the PIFAC Council (Package and Interconnect Failure Analysis). She received her bachelor's degree in biochemistry from Rutgers University in 1994.

Vision Statement

"I would love to see more failure analysis engineers participate in EDFAS. The FA community is relatively small and we must all take ownership and do our part to improve it. My personal goals are to make EDFAS and the ISTFA event accessible to more individuals and to increase the participation rate in the conference. EDFAS could help our members justify conference attendance by enabling their involvement with our society by volunteering on a review committee, organizational committee, or as a tutorial contributor. I believe we should strive to keep EDFAS in the forefront of the failure analysis world and increase the sessions for emerging talent. EDFAS should continue to be the society people think of first as a source of failure analysis innovation sharing, training, and networking."



Tom Schamp is principle consulting scientist at Materials Analytical Services LLC headquartered in Suwanne, Ga. His failure analysis background grew out of his engineering roles at Cerium Labs and SVTC Technologies. As the lead TEM analyst and materials scientist, he regularly worked on troubleshooting, DOE development, and running TEM experiments.

Later, as senior product specialist at Hitachi High Technologies America, Schamp supported customers through demonstrations. Before joining Cerium, he received a B.S. in math and physics from Lynchburg College and two degrees (M.S. and Ph.D.) in materials science and engineering from the University of Virginia.

Schamp's volunteerism with ISTFA includes serving as a presenter, reviewer, and session co-chair for microscopy. With a home in Grand Prairie, Texas, he stays involved with the ASM Alamo Chapter. Schamp has also been a presenter at a local EDFAS meeting.

Vision Statement

"I see EDFAS as a strong resource not only for the semiconductor FA community, but also for those outside of it. The wide range of techniques and methodologies utilized within the FA community from SPC to microscopy to simulations are useful for general materials analysis. A tremendous strength of the EDFAS community is the openness to share techniques and new technologies.

Where I see the greatest potential is in growing engagement with students and vendors. I would like to see more student involvement at ISTFA, where students get to see real-world applications and solutions, as well as share their own solutions. I can imagine a number of ways to bring in students, such as direct marketing to colleges and universities in the ISTFA host cities, travel grants, and student awards.

My observation is that vendors—having been one myself—self-segregate from the attendees. Some of this is by necessity, such as booth setup, but some is simply human nature to remain within one's crowd. Vendors have the added complexity of being in competition with one another and needing to ensure their own trade secrets are not compromised. I would like to find ways to break down these barriers and encourage social and networking interactions between attendees and vendors. A few ideas include smaller tables in seating areas, continuing to provide wide blocks of time during ISTFA for engagement, and joint vendor-customer presentations.

Ultimately, my vision for EDFAS is to continue to be a strong resource for the community while growing the membership."

EDFAS
Electronic Device Failure Analysis Society
ASM INTERNATIONAL

DIRECTORY OF INDEPENDENT FA PROVIDERS

Rosalinda M. Ring, Lam Research
rose.ring@lamresearch.com

Electronic companies of all types and sizes require failure analysis (FA) services. Our goal is to supply a resource of FA service providers for your reference files. The directory lists independent providers and their contact information, expertise, and types of technical services offered.

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INTERNATIONAL TIN ASSOCIATES (ITA) LABS

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ROODMICROTEC GMBH

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PRODUCT NEWS

PRESS RELEASE SUBMISSIONS:
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Larry Wagner, LWSN Consulting Inc.
lwagner10@verizon.net

NEW SOLUTIONS FOR ACCELERATING, INNOVATING AND ENHANCING PRODUCTIVITY IN THE FAB AND LAB

Thermo Fisher Scientific, Shanghai, announces new products that improve quality control and yield in semiconductor manufacturing.

Verios G4 Extreme High-Resolution SEM. The Thermo Scientific Verios G4 extreme high-resolution (XHR) scanning electron microscope (SEM) delivers the capability and flexibility needed to determine root cause defects, yield losses, and process and product failures.



Thermo Scientific Verios G4.

Hyperion II Fast & Efficient Nanoprober. Nanoprobers make direct electrical measurements of individual transistors. The new Thermo Scientific Hyperion II, a nanoprober based on an atomic force microscope (AFM), eliminates the vacuum requirements and e-beam/sample interactions of SEM-based nanoprobers. The Hyperion II's automated operation and imaging modes are designed for speed and ease of use. In addition, its ability to precisely localize electrical faults may improve the speed and efficiency of subsequent DualBeam or TEM analysis.



Thermo Scientific Hyperion II.

iCAP TQs ICP-MS for Fast and Reliable Chemical Monitoring. The Thermo Scientific iCAP TQs inductively coupled plasma-mass spectrometer (ICP-MS) is a dedicated semiconductor version of the well-established iCAP TQ ICP-MS. It provides the fast, reliable, and reproducible measurement of low-level contaminants in ultra-high purity (UHP) chemicals required to support automated at-line monitoring and statistical process control for advanced semiconductor manufacturing processes. Moving chemical analysis from the lab to the fab is now possible with this new system and allows at-line control of chemical baths, which optimizes response times.

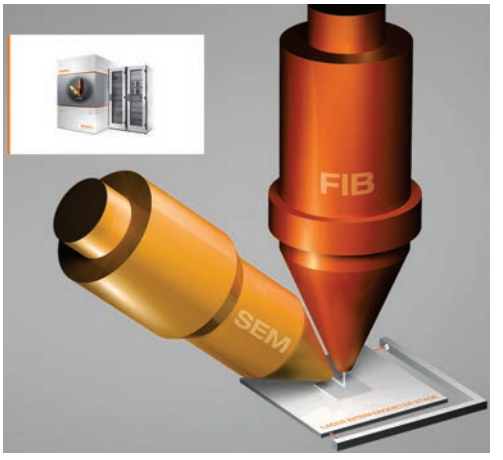


Thermo Scientific iCAP TQs.

For more information, visit thermofisher.com.

FIB-SEM SPECIALIZES IN FIB-CENTRIC NANOFABRICATION

Raith, Dortmund, Germany, introduces a state-of-the-art solution for FIB-SEM nanofabrication with the new VELION FIB-SEM instrument. To meet the most demanding requirements in R&D nano prototyping as well as sample preparation and microscopy, the ion column is installed

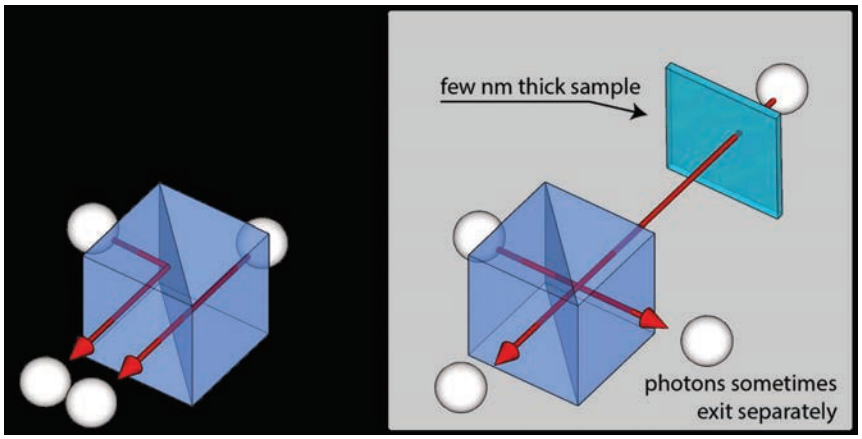


VELION, inset image, supports FIB and SEM nanofabrication.

vertically in the system. Supported by a Raith proprietary fast field emission SEM column and its unique laser interferometer stage, VELION is equipped for various research and development tasks.

"VELION provides versatile FIB nanofabrication across large areas with all direct and 3D patterning techniques. Complementing electron beam lithography, it helps to achieve scientific results faster by easy in-situ optimization and less process steps. At the same time, sample preparation and inspection applications like x-section analysis and TEM lamella are enabled by live high resolution SEM imaging," says Dirk Brüggemann, VP of sales and marketing. "FIB and even multiple non-contaminating ion species beyond gallium and new patterning approaches are now available with lithography class stability and precision."

For more information, visit raith.com/velion.



Artist's impression of photons entering beamsplitter, as per the new research technique.

100× MORE PRECISE NANOSCALE MEASUREMENTS

The precision of measuring nanoscopic structures could be improved in the future based on research into optical sensing by scientists at the University of Warwick and QuantIC researchers at the University of Glasgow and Heriot-Watt University. QuantIC is the UK Quantum Technology Hub in Quantum Enhanced Imaging and is part of the UK National Quantum Technologies Program.

Using pairs of photons, researchers devised a way to measure the thickness of objects that are less than a 100,000th of the width of a human hair. The new technique involves firing two near identical photons onto a beamsplitter and monitoring their subsequent behavior—with some 30,000 photons detected per second, and 500 billion in use during a full experiment.

Due to the tendency of identical photons to "buddy up" and continue travelling on together—the result of a delicate quantum interference effect—the new research setup offers the same precision and stability as existing one-photon techniques that are more costly because of the expensive equipment required.

The new research offers a range of potential uses, including research to better understand cell membranes and DNA as well as quality control for nanoscopic 2D materials such as graphene. The results provide an improvement on current two-photon techniques with up to 100× better resolution.

To measure the thickness of a transparent object, a pair of identical photons are fired along separate paths:

Photon A then continues into a beamsplitter, while Photon B is slowed down by a transparent object before entering the same beamsplitter.

The likelihood that the photons exit the beamsplitter together is then recorded, allowing researchers to measure the thickness of the transparent object Photon B passed through. As the thickness of the sample is increased, the photons are more likely to exit the beamsplitter separately.

Dr. George Knee of the University of Warwick's physics department, who developed the theory behind the new method, explains, "What's really exciting about these results is that we can now investigate objects down at the nanoscale with an optical sensor operating on a fundamentally different physical effect. Until now, so-called two-photon interference has not been able to achieve such great resolution, meaning that we are stuck with some of the downsides of the established methods based on single-photon interference—which requires more expensive technology than our new two-photon technique.

"We have managed to get a big improvement by tuning the interferometer into a more sensitive operation mode and removing slow drift by repeatedly switching the sample in and out. The advantages of being impervious to phase fluctuations and having large dynamic range mean that sensors such as ours could have a big impact on biological imaging and the associated research that it feeds into."

The research, "Attosecond-Resolution Hong-Ou-Mandel Interferometry," is published by *Science Advances.*

For more information, visit advances.sciencemag.org.

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TRAINING CALENDAR

Rosalinda M. Ring, Lam Research
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LIFELONG LEARNING

EDFAS believes in lifelong learning and supporting our members and customers in that endeavor. Our goal is to provide a list of educational resources in failure analysis and related topics in each issue of *EDFA* magazine. In addition, explore all EDFAS has to offer from regional events, chapter courses, and tutorials and courses during ISTFA. Find out more by visiting edfas.org.

August 2018

EVENT	DATE	LOCATION
Microscopy & Microanalysis 2018	8/5-9	Baltimore, MD
Contact: M&M 2018		
Austin (CTEA) Expo & Tech Forum Vendor Conferences 2018	8/14	Austin, TX
Southeast Asia Training Conference on Electronics Assembly Technologies	8/14-16	Penang, Malaysia
Capital Expo & Tech Forum	8/23	Laurel, MD
SMTA China South Technology and Vendor Conferences 2018	8/27-30	Shenzhen, China
Contact: SMTA		
Metallographic Techniques	8/20-23	Novelty, OH
Corrosion	8/27-30	Novelty, OH
Principles of Failure Analysis	8/29-31	Compton, CA
Contact: ASM International		

September 2018

EVENT	DATE	LOCATION
19th International Microscopy Congress	9/9-14	Sydney, Australia
Contact: IMC19		
CMOS, BiCMOS and Bipolar Process Integration	9/10-12	San Jose, CA
Contact: Semitracks Inc.		
Introduction to Metallurgical Lab Practices	9/5-7	Novelty, OH
Metallurgy for the Non-Metallurgist	9/10-13	Novelty, OH
Practical Fractography	9/17-18	Novelty, OH
Contact: ASM International		

October 2018

EVENT	DATE	LOCATION
29th European Symposium on Reliability of Electron Devices, Failure Physics, and Analysis	10/1-5	Aalborg, Denmark
Contact: ESREF 2018		
European Focused Ion Beam Users Group	10/1-5	Aalborg, Denmark
Contact: EFUG 2018		
IC Reliability, Fault Isolation and Failure Analysis	10/8-12	Dresden, Germany
Contact: CEI-Europe		
International Wafer-level Packaging Conference (IWLPC)	10/23-25	San Jose, CA
Contact: SMTA		
Materials Science & Technology (MS&T18)	10/14-18	Columbus, OH
International Symposium on Testing and Failure Analysis (co-located with ITC)	10/28-11/1	Phoenix, AZ
Contact: ASM International		
International Test Conference (co-located with ISTFA)	10/28-11/2	Phoenix, AZ
Contact: ITC 2018		

November 2018

EVENT	DATE	LOCATION
Introduction to Metallurgical Lab Practices	11/6-8	Novelty, OH
Contact: ASM International		

Contact Information

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INTERNET RESOURCES FOR ENGINEERING

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BODY OF EUROPEAN REGULATORS FOR ELECTRONIC COMMUNICATIONS

berec.europa.eu

This group is committed to independent, consistent, high-quality regulation of electronic communications markets for the benefit of Europe and its citizens. It contributes to the development and better functioning of the internal market for electronic communications networks and services.

AUTOMOTIVE ELECTRONICS COUNCIL (AEC) COMPONENT TECHNICAL COMMITTEE

aecouncil.com

The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high-quality electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. This website makes available the technical documents developed by the AEC Component Technical Committee.

EOS/ESD ASSOCIATION INC.

esda.org

The EOS/ESD Association is a professional voluntary association dedicated to advancing the theory and practice of electrostatic discharge (ESD) avoidance. The EOS/ESD Association has grown to more than 2000 members throughout the world. It is chartered to expand ESD awareness through standards, educational programs, local chapters, publications, tutorials, certification, and symposia.

THE EUROPEAN SPACE AGENCY (ESA)

esa.int

The ESA is Europe's gateway to space. Its mission is to shape the development of Europe's space capability and ensure that investment in space continues to deliver benefits to the citizens of Europe and the world. The ESA is an international organization with 22 member states. By coordinating the financial and intellectual resources of its members, it can undertake programs and activities far beyond the scope of any single European country.

LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Optics, Optical Techniques, and Fault Isolation

Michael R. Bruce, Consultant
mike.bruce@earthlink.net

This column covers peer-reviewed articles published since 2015 on optical microscopy, optical fault isolation techniques, and photon detectors. Optical methods and techniques are fundamental to nondestructive analysis of modern integrated circuits. Note that inclusion in the list does not vouch for the article's quality and category sorting is by no means strict.

If you wish to share an interesting, recently published peer-reviewed article with the community, please forward the citation to the email address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title, journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article topic.

- TW. Adams, M. Sadatgo, and D.Ö. Güney: **"Review of Near-Field Optics and Superlenses for Sub-Diffraction-Limited Nano-Imaging,"** *AIP Advances,* 2016, *6,* p 100701.
- U. Birk, J. von Hase, and C. Cremer: **"Super-Resolution Microscopy with Very Large Working Distance by Means of Distributed Aperture Illumination,"** *Scientific Reports,* 2017, *7,* p 3685.
- A. Boscaro, S. Jacquir, P. Perdu, et al.: **"Automatic Localization of Signal Sources in Photon Emission Images for Integrated Circuit Analysis,"** *Signal, Image and Video Processing,* 2018, *12,* p 775.
- A. Boscaro, S. Jacquir, P. Perdu, et al.: **"Pattern Image Enhancement by Automatic Focus Correction [Using a Confocal Laser Microscope],"** *Microelectron. Reliab.,* 2017, *249,* p 76-77.
- X. Chen, L Liu, and E. Li: **"Metal Defect Localization of GaAs or Si Based ICs by Dynamic Emission Microscopy,"** *Microelectron. Reliab.,* 2017, *72,* p 24.
- S. De Castro, J.-M. Dutertre, B. Rouzeyre, et al.: **"Front-side Versus Backside Laser Injection [Fault Attacks]: A Comparative Study,"** *J. Emerg. Technol. Comput. Syst.,* 2016, *13,* p 7.
- L. Gao, E. Yalon, A.R. Chew, et al.: **"Effect of Oxygen Vacancies and Strain on the Phonon [Raman] Spectrum of HfO_2 Thin Films,"** *J. Appl. Phys.,* 2017, *121,* p 224101.
- A.J. Gayle, L.H. Friedman, R. Beams, et al.: **"Two-Dimensional Strain-Mapping by Electron Backscatter Diffraction and Confocal Raman Spectroscopy,"** *J. Appl. Phys.,* 2017, *122,* p 205101.
- D. Hänschke, A. Danilewsky, L. Helfen, et al.: **"Correlated Three-Dimensional Imaging [Using X-Ray Diffraction Imaging and Light Microscopy] of Dislocations: Insights into the Onset of Thermal Slip in Semiconductor Wafers,"** *Phys. Rev. Lett.,* 2017, *119,* p 215504; also see M.K. Horton, **"Viewpoint: 3D Imaging of Dislocations,"** *Physics,* 2017, *10,* p 126.
- M.A. Hossain, J. Canning, K. Cook, et al.: **"Smartphone Laser Beam Spatial Profiler,"** *Optics Letters,* 2015, *40,* p 5156.
- M.Y. M. Huang, B. Liu, and J.C.K. Lam: **"Enhancement of Raman Signals from Low-K Dielectrics with Angle-Resolved Light Scattering on Nanostructure Patterned Cu/Low-K Interconnects of IC Devices,"** *Journal of Vacuum Science & Technology A,* 2015, *33,* p 020603.
- G. Huszka and M.A.M. Gijs: **"Turning a Normal Microscope into a Super-Resolution Instrument Using a Scanning Microlens Array,"** *Scientific Reports,* 2018, *8,* p 601.
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GUEST COLUMNIST

ARTIFICIAL INTELLIGENCE IN ELECTRONIC DESIGN AUTOMATION ASSISTING PHYSICAL FAILURE ANALYSIS

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Physical failure analysis (PFA) has relied exclusively on advanced FA equipment in the past. However, without the assistance of Electronic Design Automation (EDA) software, it has become very difficult to narrow down the location of defects on a big chip. State-of-the-art diagnostic EDA tools can report suspects within a very small region on a layout and can even pinpoint to a few transistors. Without such diagnostic EDA tools, PFA engineers may have a hard time initiating failure analysis. Typically, PFA engineers are not concerned with the techniques behind EDA tools, as long as the equipment can report the correct location and suspect for them to dive in. However, understanding the recent enhancements of EDA tools from a high level may help PFA engineers achieve their targets more effectively and efficiently. Among the recent enhancements in EDA diagnostic and yield learning tools are artificial intelligence (AI) technologies such as machine learning. This column reviews three AI technologies applied in state-of-the-art EDA diagnostic and yield learning tools and suggests how PFA engineers can benefit from them.

AI-ASSISTED ELECTRICAL DIAGNOSIS

In the past, simulation-based electrical diagnosis was widely used in EDA diagnostic tools. Physical defects are modeled as logical stuck-at or transition faults. Candidate faults were injected into the netlist and fault simulation was run. If the simulated failures "match" the silicon failures observed on the die tester, the injected logical fault(s) are reported as suspect(s). PFA engineers are then guided by the diagnosis report to dive in to the area containing the suspect(s). The criteria for a "match" varies from tool to tool. Essentially, it measures the similarity between logical failure models and observed electrical defective behavior. It is relatively accurate as long as the logical faults can model the real silicon defects. However, this scenario changed when new technology nodes moved to nanometers, FinFET and other advanced technologies became popular, and more complicated cell libraries emerged. Today it is very difficult and expensive to model silicon defects accurately, which leads to a reduced PFA success rate, if still using simulation-based EDA tools. Therefore, the current trend is to use AI to bridge the gap between fault model and real defect behavior, to tolerate inaccuracy and noises. One example is a paper recently published in the *Proceedings of Asian Test Symposium.*[1] Unsupervised machine learning techniques are used to partition scan cells on one faulty scan chain into multiple groups, where the defective cells are located at the boundary between two adjacent groups. The diagnostic score is calculated based on Bayesian inference equations. PFA engineers should interpret these scores as probabilities of the reported scan cell(s) being defective.

AI-ASSISTED SYSTEMATIC DEFECT ROOT CAUSE IDENTIFICATION

Root cause deconvolution (RCD)[2] is a novel yield analysis technology based on machine learning methodology. It works by analyzing many layout-aware diagnosis reports together to identify the underlying root cause distribution most likely to explain a particular set of diagnosis results. It has two benefits for PFA engineers: First, it can identify the failing die that most likely represent the systematic defect of interest. PFA on these failing die has a much higher success rate identifying systematic defects than PFA on randomly selected failing die. In that sense, RCD works as a "virtual PFA," with the ability to determine defect distribution for a population of failing devices before real PFA is performed. Second, the RCD results can be back annotated to the individual diagnosis suspect. Where layout-aware diagnosis points to a segment of interconnect, RCD can isolate a particular root cause in that segment, such that diagnostic resolution is enhanced. Therefore, it will increase the PFA relevance and success rate dramatically, while reducing PFA cycle time.

AI-ASSISTED HOT SPOT IDENTIFICATION

Identifying layout hotspots during the design stage is an important yet challenging design-for-manufacture (DFM) process. Due to its success in image-based classification applications, machine learning based on deep neural networks[3] promises an alternative that is faster and more accurate than rigorous model-based simulation.[4] Moreover, revealing the correlations between scan diagnostic results and DFM is an emerging field, driven by the increased usage of diagnosis combined with the necessity of identifying systematic critical features. In a recent Advanced Semiconductor Manufacturing Conference paper,[5] a novel flow to correlate diagnostic results and DFM rules was proposed. PFA engineers can use these new technologies not only to identify systematic defects, but also differentiate if a systematic defect is caused by design issues or manufacturing problems.

SUMMARY

In summary, PFA engineers should keep up with recent advancements in diagnosis and yield learning EDA tools, especially those based on AI and machine leaning technologies. These advancements can help them interpret diagnosis reports, such that picking the right die for PFA leads to a higher success rate; prioritize die for PFA based on their likelihood of revealing systematic defects; and differentiate the root cause between a design or a manufacturing issue to ensure an efficient and effective process to solve the yield problem.

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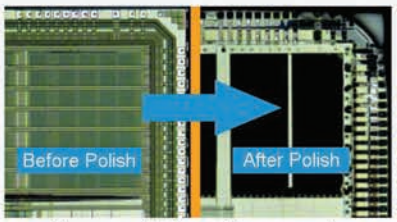
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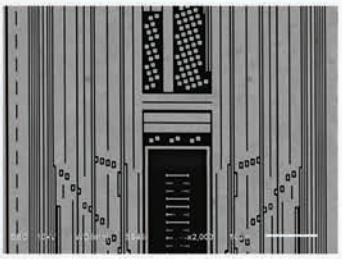
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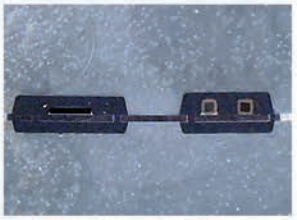
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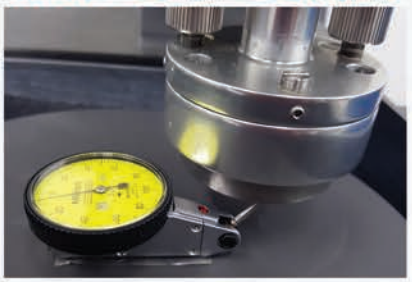


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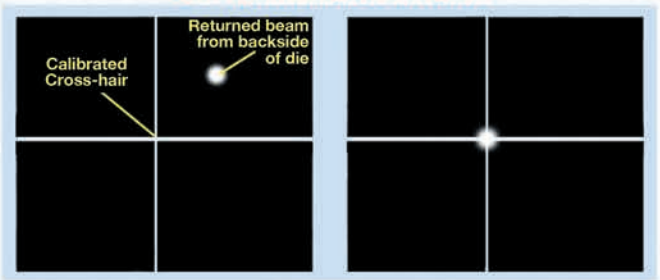


Better sample alignment produces better polishing results

MECHANICAL ALIGNMENT



OPTICAL ALIGNMENT



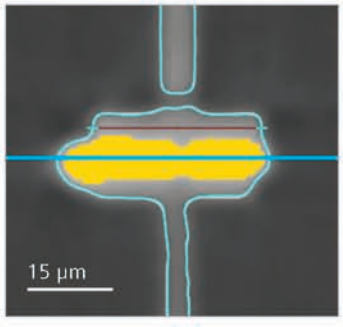
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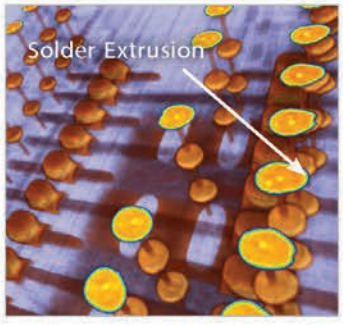
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