MAY 2018 | VOLUME 20 | ISSUE 2

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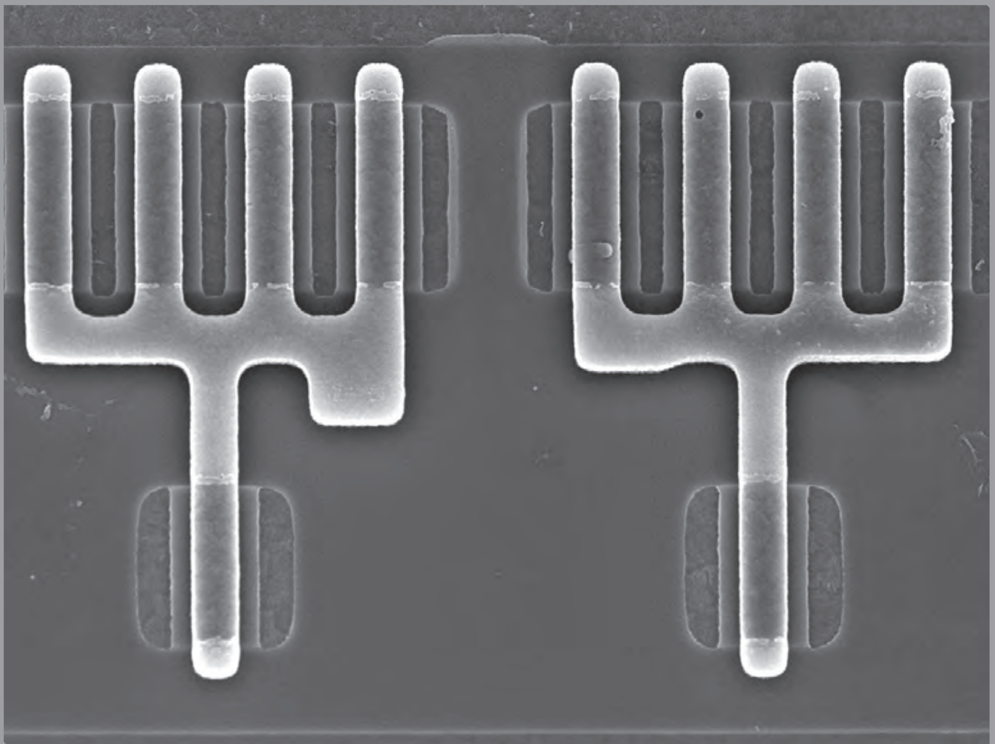
PAGES 38 & 39



4 FAILURE MECHANISMS OF ELECTROMECHANICAL RELAYS ON PCBAs: PART II

10 COMBINATIONAL LOGIC ANALYSIS WITH LASER VOLTAGE PROBING

18 DIAGNOSTIC TECHNIQUE SELECTION FOR SRAM LOGIC TYPE FAILURES

26 RECENT INNOVATIONS IN EX SITU LIFT OUT APPLICATIONS AND TECHNIQUES

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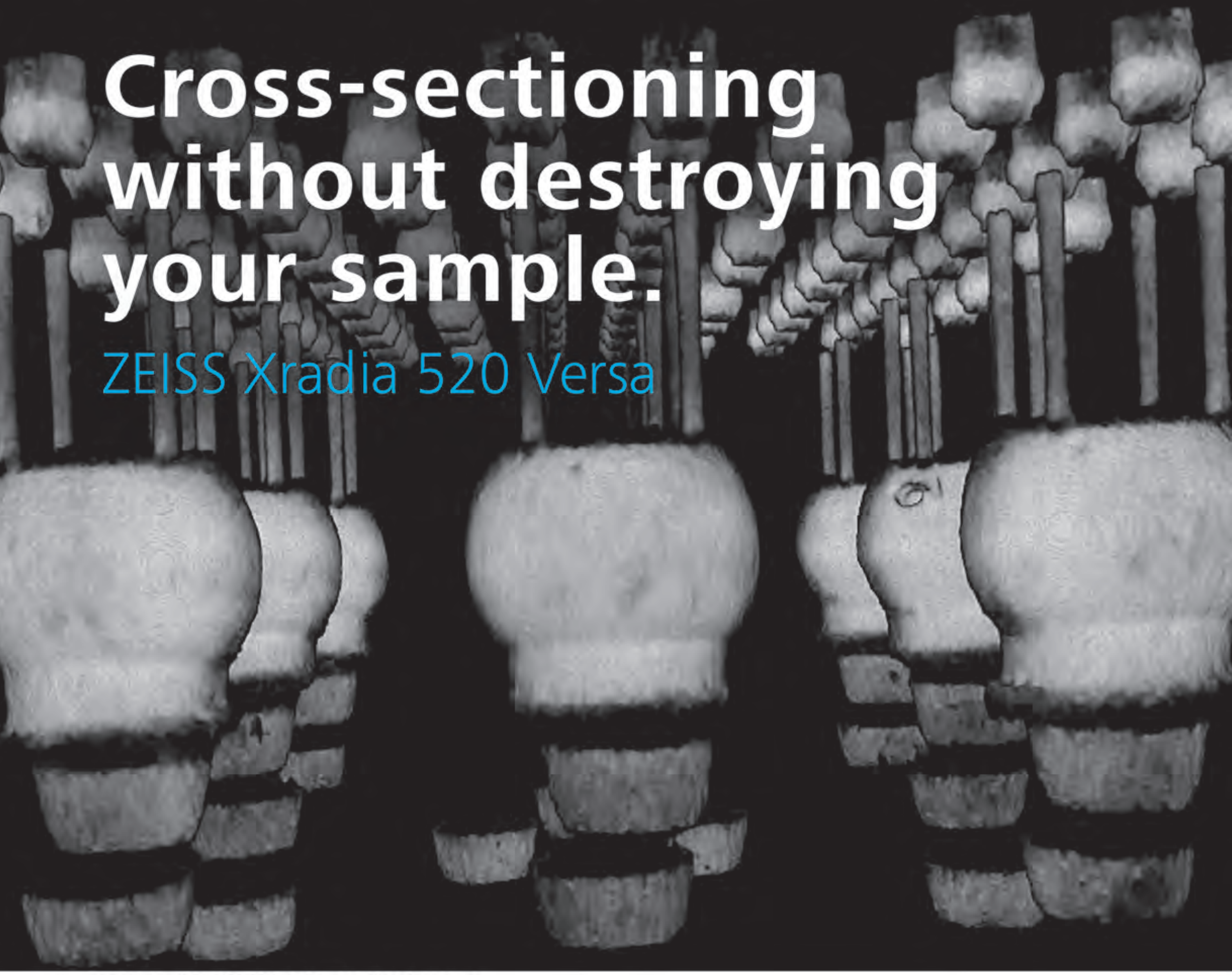

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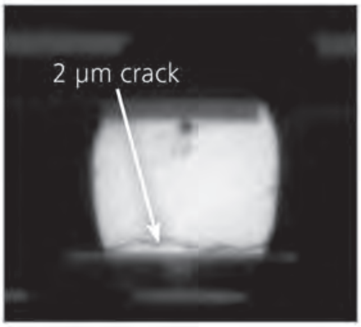

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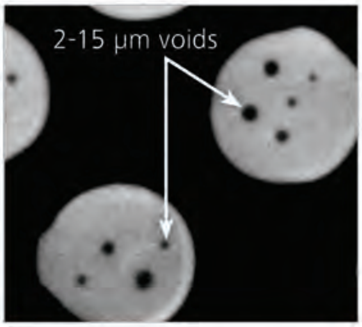

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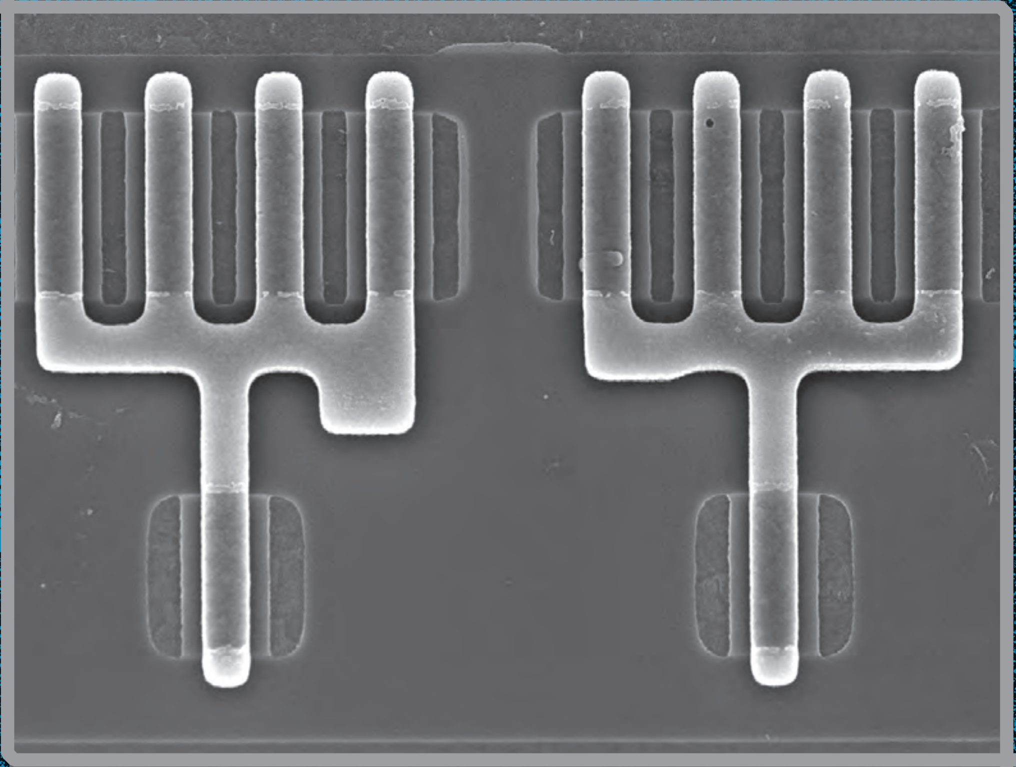

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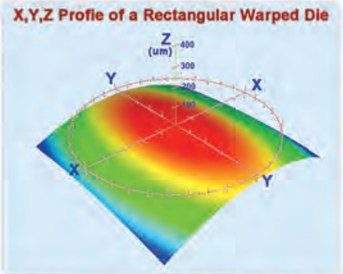

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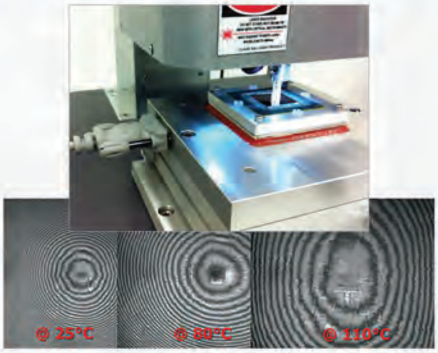

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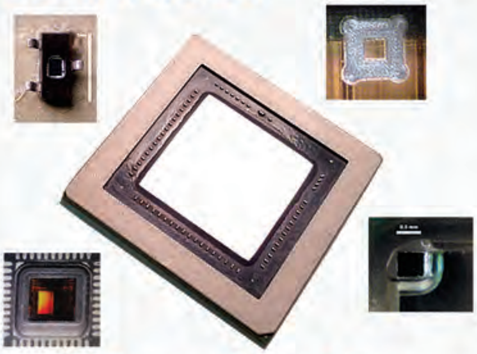

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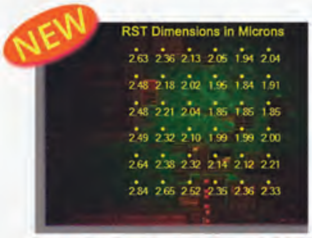

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2.48	2.21	2.04	1.85	1.85	1.85
2.49	2.32	2.10	1.99	1.99	2.00
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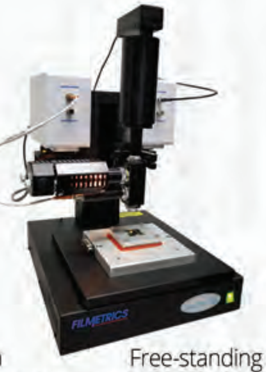

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4 Failure Mechanisms of Electromechanical Relays on PCBAs: Part II

Gert Vogel

Using case studies, this article continues the analysis of electromechanical component failures in printed circuit board assemblies and their corresponding root causes.

10 Combinational Logic Analysis with Laser Voltage Probing

Venkat Krishnan Ravikumar, Winson Lua, Gopinath Ranganathan, and Angeline Phoa

Laser voltage probing has become widely popular as an electrical fault isolation technique, but spatial resolution challenges still exist. Proposing combinational logic analysis as a solution, the authors show how establishing a waveform library and truth table can improve process reliability and speed.

18 Diagnostic Technique Selection for SRAM Logic Type Failures

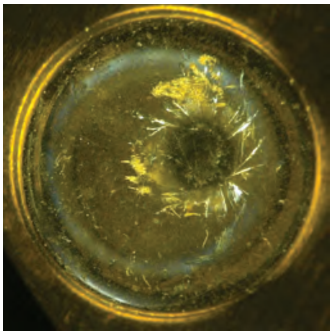
Zhigang Song and Laura Safran

Static random access memory is often used as a process qualification vehicle. However, this approach must frequently be coupled with a more detailed fault isolation technique for logic failures. By reviewing four case studies, learn how to select the proper diagnostic technique for a specific type of failure.

26 Recent Innovations in Ex Situ Lift Out Applications and Techniques

Lucille A. Giannuzzi

Read about recent advances in ex situ lift out processes applicable to focused ion beam specimen preparation using site specific scanning/transmission electron microscopy (S/TEM).



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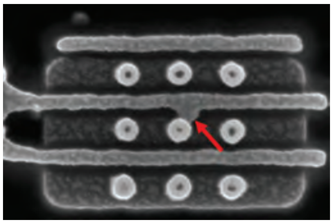

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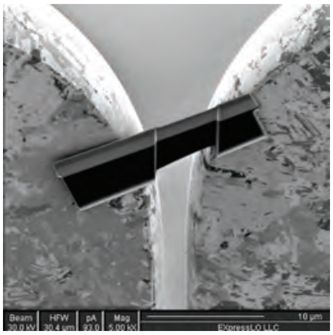

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ABOUT THE COVER

The world's smallest pair of forks. This SEM image shows tiny pinhole damage on a polysilicon gate (fork on right) that caused a current leakage failure. *Photo by Kah Chin Cheong, ON Semiconductor, First Place Winner in Black & White Images, 2017 EDFAS Photo Contest.*

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PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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GUEST EDITORIAL

CHALLENGES FOR AUTOMOTIVE FAILURE ANALYSIS

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Electronic systems in the automotive industry are becoming more and more complex. Modern cars require more signal processing resources than ever to increase levels of integration of various systems. Packaging technologies undergo complex changes by employing materials and material combinations previously unavailable to the automotive market (e.g., 3D system in packaging, bonding, and soldering within a single package). As a consequence, failures become increasingly complex and failure mechanisms are more difficult to understand. One key asset in this process is the successful utilization of failure analysis (FA). Implementation of the stringent requirements of automotive customers for zero-defect quality and reliability requires both FA and destructive physical analysis (DPA). Yet, a 100% success rate is expected, creating a complex area of conflict only solvable by a matching FA strategy.

In an automotive context, every step in the product cycle is assisted by FA. During the design phase, debugging is performed. Parts failing during qualification and reliability testing are analyzed in-depth to verify the failure mode. Samples passing the qualification and reliability tests are analyzed by various methods, including DPA to verify that non-catastrophic degradations within the tested devices are not critical for the product. Meeting the zero-defect quality target of automotive devices requires intense FA involvement during the ramp-up phase, by analyzing each failure. Finally, during series production, FA is expected to analyze even single customer return parts to identify problems in the field at a very early stage. Involving FA in all product phases ensures the extension of competence and the availability of capable FA techniques, when required.

Analysis of reliability test failures and customer returns is especially challenging due to the fact that only single devices are available. Successful analysis of a single failure means electrical characterization, fault localization, and physical preparation on one golden sample. For field return parts, the customer additionally expects containment actions within a constantly shrinking time frame, which consequently shortens the allowable time for performing FA. In the automotive industry, analysis is almost always performed on the product itself, not on test structures or process control monitors. Dedicated FA-friendly design elements and components specific to supporting FA (design for analysis) ease the tedious process of enabling successful FA in this environment. This integration becomes even more important: FA accompanies the overall product cycle, and thereby drives development of systematic methodology and competence during all phases of the product lifecycle.

There is a constant drive to improve FA. Cutting edge semiconductor technologies require development of adequate analysis equipment and

(continued on page 16)

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FAILURE MECHANISMS OF ELECTROMECHANICAL RELAYS ON PCBAs: PART II

Gert Vogel, Siemens AG, Digital Factory Division, Control Products, DF CP QM SQA 5
gert.vogel@siemens.com

INTRODUCTION

Many printed circuit board assemblies (PCBAs) not only have electronic components, but also electromechanical relays. The spectrum of root causes that lead to an increased contact resistance or a complete contact failure of these relays is completely different than failures of electronic components. A detailed analysis of some typical failures and the corresponding root causes are presented in this article.

Part I of this article (February 2018 *EDFA*) explained that many of the failure mechanisms that lead to contact failures of electromechanical relays are actually self-centering effects. Nonconducting silicon dioxide forms in the contact region out of silicon vapor or silicon oil, due to the fact that electric arcs only occur at the shortest distances between two contacts. As a result, the failure mechanism is self-centering. SiO_2 only forms where it can cause a fault.

The nonconductive plastic particle between two contacts is not positioned there by accident, but as a result of a driving force—a self-centering effect that results from the vibration of mechanical switching and the force of an inhomogeneous electrical field, which occur simultaneously. Countermeasures in the form of a thin contact oil film prevent particles from bouncing, but can also lead to a new self-centered failure mechanism—as sticking particles migrate into the contact region along the oily surfaces of the contacts. The driving force of this effect is the surface tension of the oil film, which wants to minimize itself and therefore contracts in the capillary around the contact point. When the contacts open, particles on the oil film are pulled in the direction of the contact area.

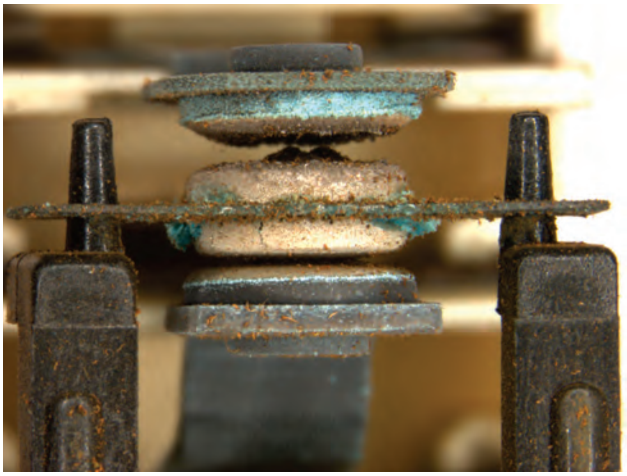

Fig. 1 **Due to contact "flutter," arcs occur over a long period of time, leading to the accumulation of nitrogen oxides in sealed relays. In conjunction with moisture, nitrous acid is formed, enabling significant corrosion.**

Particles in the contact region result in an elevated contact resistance if two conditions are met: They must be large enough to keep the contacts permanently apart, yet small enough that an electric arc can occur. Oxidation of the surface, and sometimes even material migration, can cause this increased resistance. Once again, the mechanism is only self-centering at the contact point.

ARCING AND FORMATION OF NITROUS OXIDES

Particles between two switching contacts do not always result in contact failure. If the applied voltage is high enough, the distance between contacts can be bridged by an arc. Small particles usually burn, leaving only a slight discoloration on the contact surface. If arcing occurs more frequently and acutely, e.g., due to increasing wear and abrasion between the contacts, then contacts may fail—or the contact resistance may increase.

However, arcs can also have unexpected effects: Arcing causes nitrous oxides (NO_x) to be formed from the oxygen and nitrogen in the air. In combination with moisture in the relay, nitrous acid, respectively nitric acid, is formed. For example, a fluttering relay can produce such a high amount of nitrous gases due to a defective capacitor that serious corrosion can occur in a sealed relay (Fig. 1). The actual cause, however, is the defective capacitor.

PHOSPHORUS DEPOSITS ON RELAY CONTACTS

An accumulation of noxious gases from arcing in an open, unsealed relay is unlikely, as the nitrogen oxides diffuse out of the relay, assisted by the pumping effect of the relay contacts. However, diffusion mechanisms work in both directions. Undesirable constituents from the environment can enter an unsealed relay and cause a failure, as we saw previously with silicon vapor. Deposition of solid phosphorus oxide or phosphoric acid on relay contacts is especially likely to trigger another self-centering failure mechanism (Fig. 2).

Phosphorus in the form of "red phosphorus" is often added to plastics as a flame retardant. The red phosphorous decomposes in the presence of heat and humidity to become phosphine (PH_3), which disperses in the ambient air and enters the relay through diffusion.

The source of phosphorous on relay contacts is rarely the plastic of the relay itself. The red phosphorous is mostly used in the plastic of the enclosure of the PCBA—or even in plastic enclosures or components somewhere else in the control cabinet. Once again, the comparatively cold relay contacts are in a unique position. On the metal surface, the phosphine gas oxidizes and is deposited as a solid phosphorous oxide or phosphorous acid. The relay contacts work as a sink for the phosphine gas. More and more of the phosphorous acid appears in the form of a

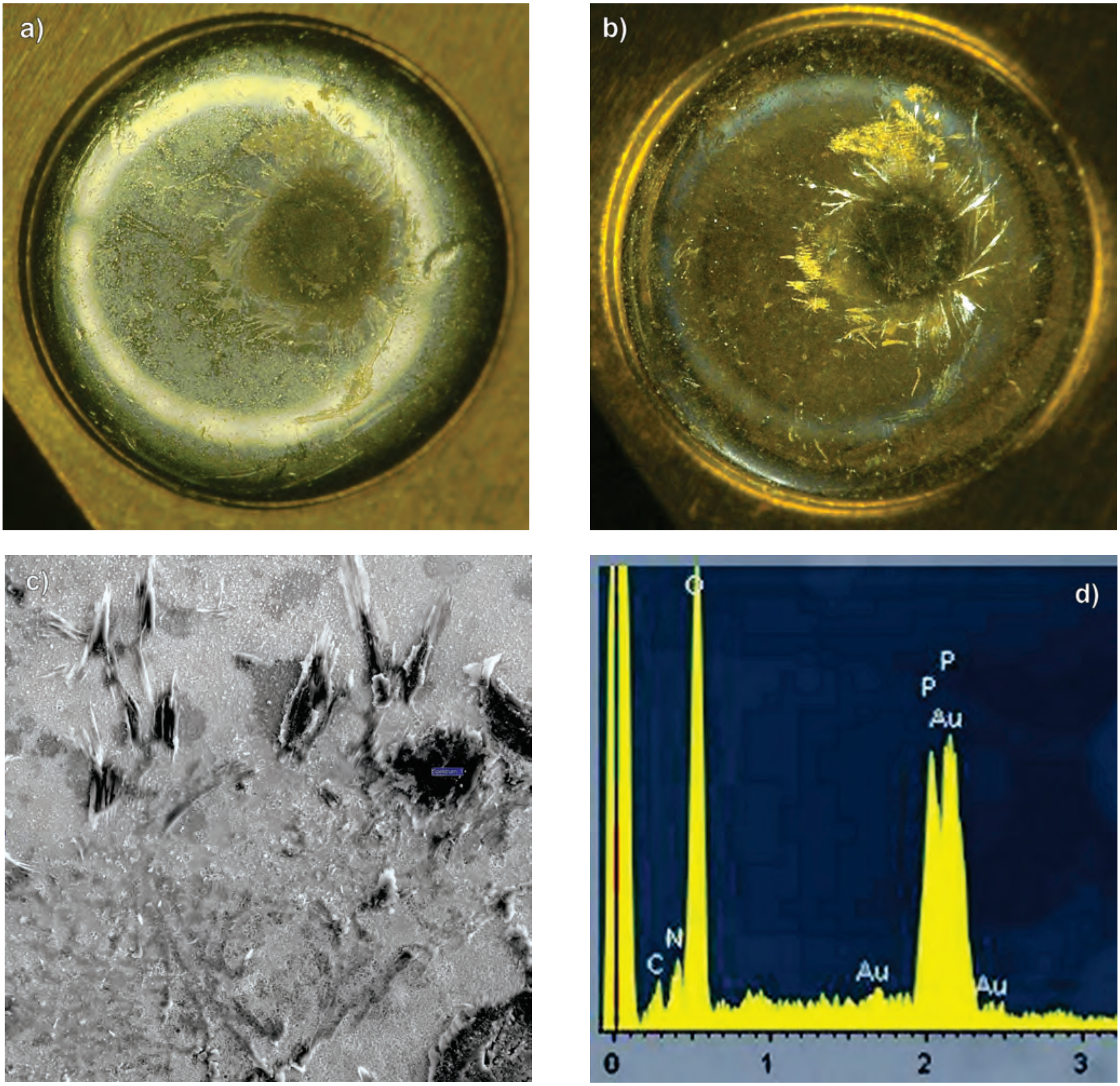

Fig. 2 **Failed contact: (a) optical microscope; (b) optical microscope, polarized light; (c) SEM image of nonconductive crystals; and (d) EDX analysis of phosphorus and oxygen.**

soft, powdery dust layer. In this form, a failure is unlikely because the amount of precipitated phosphorous at the contact point itself is even less than on the outer regions of the contact surface.

However, phosphorous acid (H_3PO_3)—and even more so, phosphorous oxide (P_4O_{10})—are hygroscopic. In fact, phosphorous oxide is used as a desiccant. This means it attracts and holds relatively large amounts of water from the atmosphere, forming an aqueous solution. Only a moderate amount of relative humidity is required to create this effect.

This leads to a contact surface that is covered with myriads of small liquid droplets. The shock of switching the contacts lets them coalesce. As a result, the complete contacts are covered with a layer of a liquid—a saturated phosphoric acid solution. As we learned with oily surfaces, this liquid also flows into the capillary between the closed contacts. Once the contacts have separated, a large drop of the liquid is left at each contact point.

As the humidity decreases, a dense layer of solid phosphorous oxide and acid at both contact points may be observed. Contact failures can occur if this layer is thick enough (Fig. 3,4). This is yet another self-centering failure mechanism.

The hygroscopy of the precipitation can be used to make a quick test for phosphorous. When you blow onto the contacts, the moisture in your breath will create a droplet around every white crystal (Fig. 5). A short time later, the liquid dries and transforms back into a small white crystal. The probability that these precipitations are phosphorous compounds is very high, because other white powdery dust—which is sometimes found inside plastic housings, such as adipic acid from decomposing polyamide—is not hygroscopic.

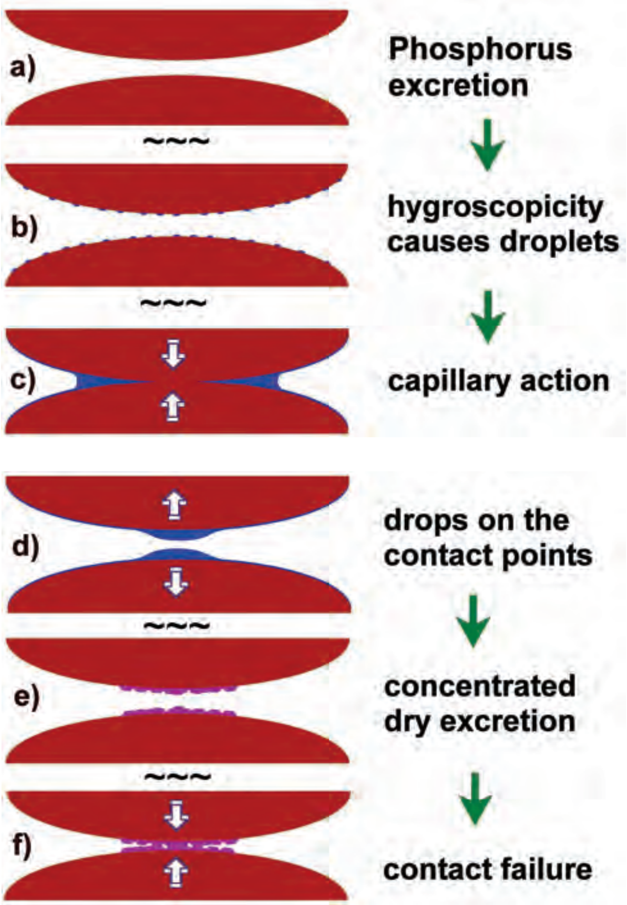
a)
Phosphorus excretion
b)
hygroscopicity causes droplets
c)
capillary action
d)
drops on the contact points
e)
concentrated dry excretion
f)
contact failure

Fig. 3 (a) Phosphine is excreted on the contact surface and oxidizes to hygroscopic phosphorous oxide and phosphorous acid. (b) Depending on relative humidity, droplets of wet phosphoric acid form. (c) Fluid gathers in the capillary around contact points. (d) When contacts open, two large drops remain at the contact points. If they dry out (e), the concentrated excretion can cause contact failures (f).

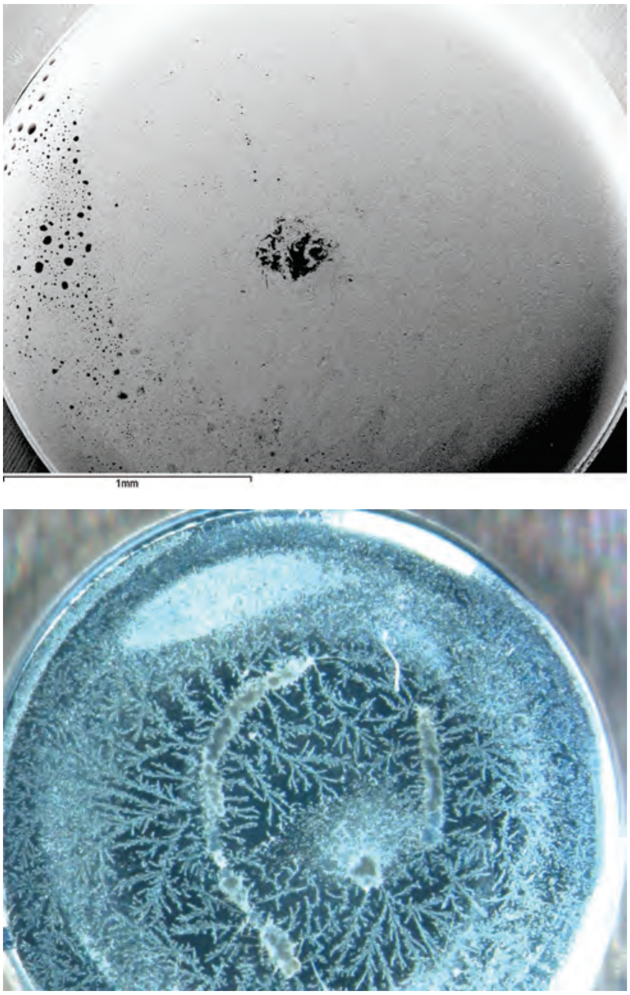

Fig. 4 Top: SEM image of a typical contact surface manifesting phosphorous excretion resulting in contact failure. Bottom: Optical microscope, polarized light, dendrites crystallized from concentrated phosphoric acid.

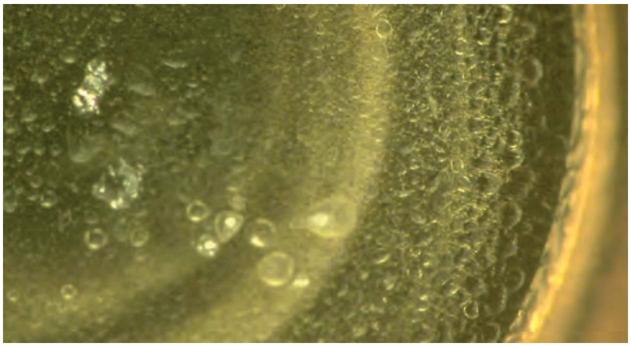

Fig. 5 With humidity, small droplets form on the phosphorous excretion, e.g., when someone blows onto the contacts.

Such failures can also occur on sealed relays. Particularly large relays tend to pop during soldering because the trapped air expands and the bonding cracks open. The contacts next to the crack in the glue are vulnerable to failures caused by phosphorous deposition.

WAX ON CONTACTS OF MINIATURE CONTACTORS/RELAYS

Wax is another substance that may cause failures in relays or miniature contactors. It is often used as a glide agent on enameled copper wires to achieve perfect wound coils. Wax adheres to the wire until the coil is heated, causing it to evaporate. Subsequently, the complete inner surface of the relay or miniature contactor involved is covered with a thin film of liquid wax. Solidifying wax in capillaries between moving parts can act like a hotmelt adhesive and mechanically inhibit switching.

Frequently, another self-centering failure mechanism occurs as more and more wax collects on the coldest parts in the relay, which are the contacts. In operation, the relay is hot, i.e., the wax is liquid and as long as it remains liquid on the contacts, no problems occur. However, once the relay cools down after operation, the drops of wax harden; these are the drops that converge at the contact points every time the contacts open. If the wax is very hard, the contact pressure is not sufficient to penetrate the wax deposit. In low temperature environments, such as a parking garage on a winter morning, this can lead to a contact failure and an elevator may not respond. When the technician arrives two hours later, the elevator operates perfectly—until the next cold morning (Fig. 6).

Such faults mainly occur with small contactors, which have a similar design to relays, but in which larger quantities of enameled copper wire are processed. The contact force of bigger contactors is usually high enough to avoid contact problems.

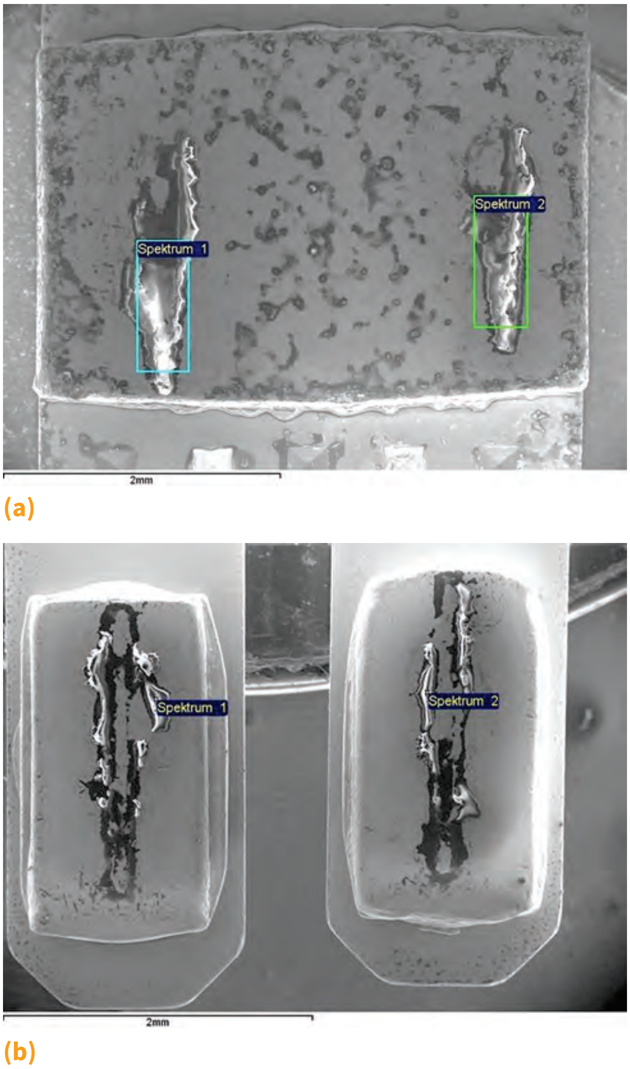

Fig. 6 Contacts of a control relay that have failed due to wax accumulation at the contact points. Design: (a) One large contact. (b) Two separate small contacts with contact edges, usually duplicated, as contactors use bridges with two contacts; shown here are two parallel double bridges. Liquid wax flows into capillaries between contacts and causes failures after cooling as the wax drops solidify directly on contact points. The theoretical advantage of double contacts with regard to contact reliability regarding particles, e.g., dust, does not apply to vapors. Enameled copper wires with wax-free glide agents must be used.

SUMMARY

Based on many case studies, complicated interrelationships that appear when analyzing the contact failure of a mechanical relay have been observed. Particles and fibers are often the immediate concern. However, it is usually the complicated physical/chemical interactions in which phase transitions occur between gaseous, liquid, and solid forms of a material—such as wax —that create problems on a more frequent basis. The influence of additives, such as red phosphorous as a flame retardant in plastics, is also to blame for a large number of failures. The chemical transformation of phosphine to phosphoric oxide and phosphoric acid on the noble metal surfaces of contacts is remarkable. This is also true for the formation of silicon dioxide due to silicon contamination. Even the use of fully sealed relays can be inadequate if they subsequently burst during soldering. Under certain circumstances, sealing relays is also counterproductive, because arcing can cause nitrous gases to form in the sealed enclosure when switching. A ventilated relay is recommended in these situations.

Understanding the various failure mechanisms, especially the self-centering mechanisms, is a great help in eliminating failures caused by mechanical relays.

ABOUT THE AUTHOR

Gert Vogel studied physics in Stuttgart, Germany. He has been with Siemens for more than 33 years. Dr. Vogel was a semiconductor technologist in the Siemens DRAM production group in Munich and Regensburg for seven years. He then moved to Siemens Amberg, where one of his specialties is the failure analysis of electronic components on printed circuit board assemblies. He led a tutorial, "Avoiding Flex Cracks in Ceramic Capacitors," at ESREF 2015. This was followed by a tutorial, "Creeping Corrosion of Copper on Printed Circuit Board Assemblies," at ESREF 2016.

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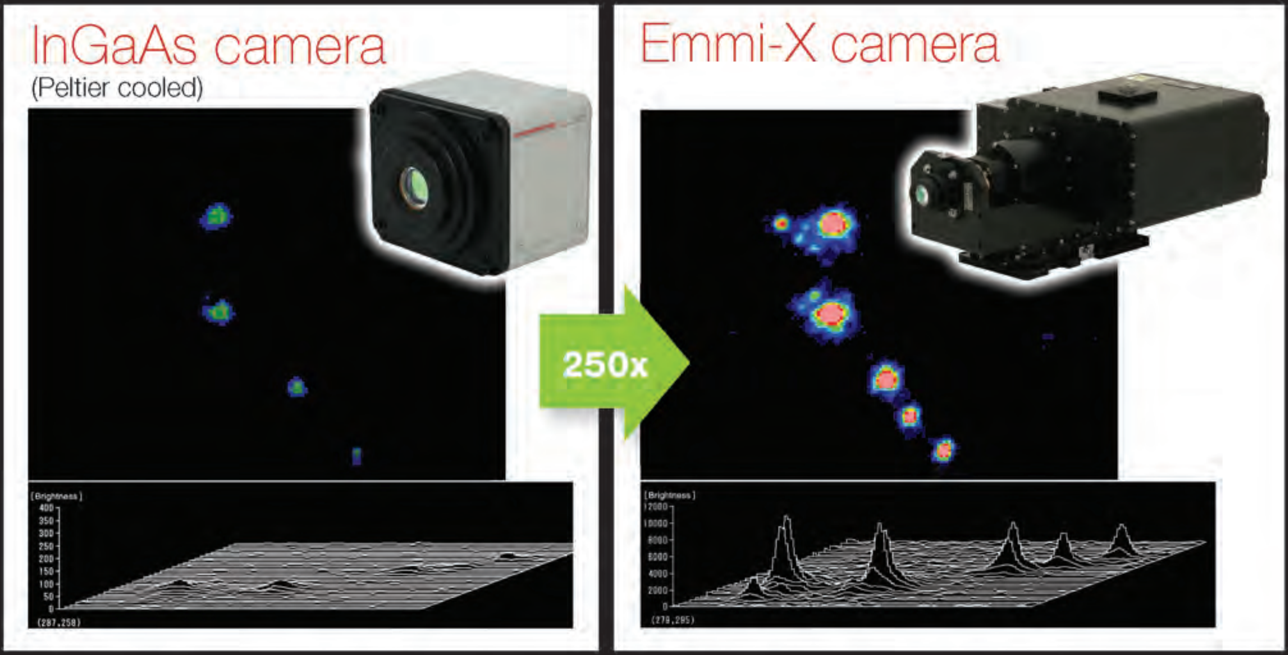
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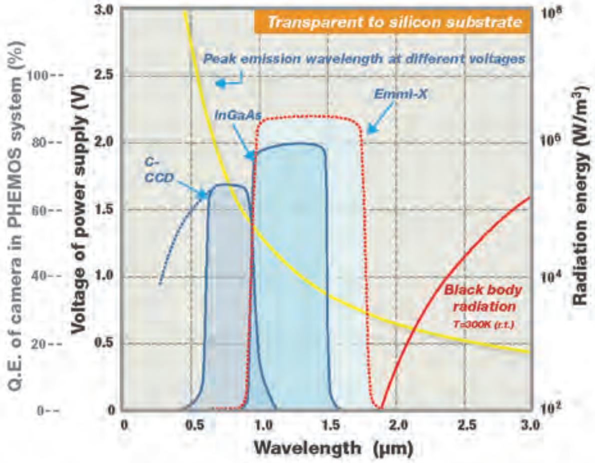

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COMBINATIONAL LOGIC ANALYSIS WITH LASER VOLTAGE PROBING

Venkat Krishnan Ravikumar, Winson Lua, Gopinath Ranganathan, and Angeline Phoa
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INTRODUCTION

As technologies scale, integrated circuits (ICs) now have incredibly dense transistor packing that can fail due to miniscule defects, which require electrical fault isolation (EFI).[1] Of several available EFI techniques, laser voltage probing (LVP) and derivatives (such as LVx) using continuous-wave near-infrared laser are very popular.[2-5] The operating principle of LVx is that the absorption of light gets modulated by changes in the electrical field and the free carrier (plasma) density within a transistor as it switches.[6] The fault isolation precision of these tools ultimately depends on the resolution of the optical probe.

Of the various LVx tools, LVP has the most potential to detect a single electrical toggle within one or a small group of transistors while the IC is in operation. LVP waveforms are useful in verifying the functionality of individual transistors, identifying broken links in chains, measuring timing delays between circuits, as well as troubleshooting pattern issues. Versatile as the applications are, interpreting LVP waveforms is often complicated because the waveforms are created using the interaction of light with a physical area surrounding the transistor of interest. To begin with, the distribution of charges and electric fields within a transistor is nonuniform. The modulation will therefore depend on the field and carrier distribution on each of the nodes (source/drain/gates). In addition, when multiple transistor nodes fall within the optical probe spot, the reflected light is a combination of modulations by each of the additional nodes.

When two or more unconnected transistors modulate the LVP waveform, due to their proximity to each other and within the probe spot, the signal is a linear superposition of individual waveforms. This is usually referred to as LVP crosstalk. In most cases, this problem can be overcome by changing the test pattern, fine-tuning the probe placement, comparing signals between NMOS and PMOS transistors, and inspecting the inputs and outputs of the transistor of interest.[7] In other words, while the spatial resolution has limitations, the resolution and assessment of toggles occur at different time intervals.

Figure 1 is an example of LVP crosstalk. The target transistor is indicated by the red rectangle and the neighbor

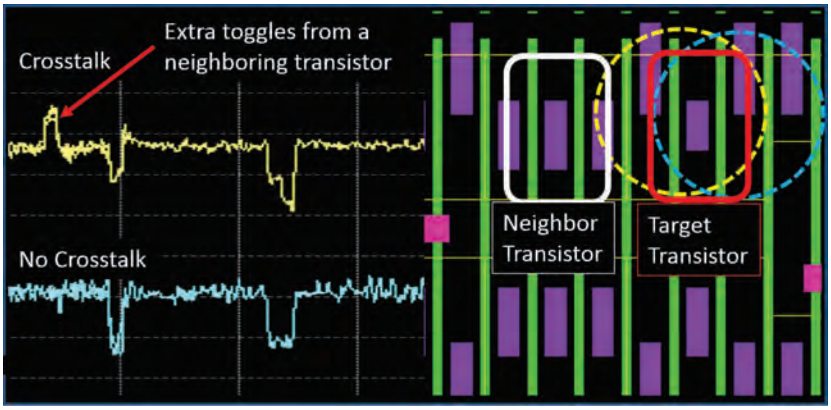

Fig. 1 **Crosstalk occurs (yellow waveform) when two transistors are closer than the optical resolution limit (dotted circles). Careful adjustment of the probe position from the yellow dotted circle to the blue dotted circle helps mitigate crosstalk (blue waveform).**

in white. The crosstalk present in the yellow waveform disappears when the probe is moved from the yellow to the blue position. Additional toggles appear in the yellow waveform—due to modulations from the neighboring transistor—and occur at a different time interval.

Complexity further increases when the transistors connected to each other are in close proximity and create a convoluted waveform. Here, changing patterns or inspecting upstream and downstream signals may not help if these transistors are in the same path and thus toggle during the same time interval. Such cases cause difficulty in predicting the logic state of a single node, as one can observe additional troughs or peaks within the same logic state. This leads to incorrect interpretations and false conclusions during LVP. While it may not be possible to separate the modulations in time or space, it is possible to look at the waveforms from the group of transistors as a whole, rather than as individual transistors. Very often, a group of related transistors form a more complex unit and perform a particular operation. We refer to these as combinational cells or logic gates.

A careful way to study combinational cells is to comprehensively investigate the electrical conditions of every node within the optical probe with techniques such as spice models,[8] but such resources may not be readily available to the failure analysis (FA) engineer. Here, the authors share the technique of combinational logic analysis (CLA) using laser voltage probing.[9,10] The process consists of developing a library of waveforms by observing simple combinational elements such as NAND and NOR gates and correlating the waveforms to a corresponding truth table.

CLA as presented in this article offers significant advantages over the conventional process.

REDUCED NEED FOR RESOLUTION

The generally accepted resolution requirement[11] for LVP is about two or three times the contacted poly pitch (CPP), which is the distance between the source and the drain contacts of a transistor at a particular technology. This forces a constant search for resolution improvement with technology, by migrating to higher numerical aperture solid immersion lenses (NA SILs) or shorter probing wavelengths, both of which have stringent sample preparation requirements. Multiple short wavelength tools have been developed over the past few years and the residual silicon thickness (RST) needs are between 1 and 5μm.[12-14] Such ultra-thin samples bring about challenges for sample preparation, as well as thermal and mechanical stability. The thermal and mechanical stability of such samples has not been completely characterized, but initial investigations[15] are concerning. These challenges make sample preparation for short wavelength light probing undesirable, especially if the failing sample is a qualification reject or a customer return.

CLA works by considering convoluted waveforms from the entire combinational logic cell instead of individual transistors, thereby reducing the raw resolution requirement imposed by LVP. While it is not possible to completely overcome the resolution constraints, CLA has potential within its limited scope to determine if cell functionality is affected by a defect.

FASTER AND MORE RELIABLE

The CLA process is quite often faster than conventional LVP. Scan logic testing for the structural test of digital circuits is limited by the efficiency of the test vectors.[16,17] To effectively test all input combinations, multiple iterations of vectors are required, which makes the LVP process long and tedious. The problem is exacerbated when the failing signature is a logical mismatch that requires specific input vectors for stimulating the failure. Observing toggles within an LVP waveform does not always mean that the observed cell is functional. CLA ensures that every possible input combination of the cell is observed, and by doing so, reliably assesses cell functionality.

CLA PROCESS

PATTERN

For effective CLA, as with LVP, appropriate patterns are required to be looped by the tester. The authors employ generic scan patterns, which are used in standard structural testing for modern digital circuits. The primary advantage of using scan is that scan flops are connected directly or indirectly—through a combinational path—to almost every digital net within the IC as shown in Fig. 2. By using a single load pattern with LVP, it is usually possible to capture enough input combinations to evaluate the entire truth table.

THE OPTICAL PROBE

The optical probe size of LVP is usually limited by the resolution of the tool.[12] The distribution of laser power within the target spot is typically Gaussian but can be altered by polarization, wavelength, and numerical aperture. This laser profile affects the number of transistors modulating the laser, as well as the strength of modulation of each node under the probe. Consequently, the position of the probe within the cell also significantly affects the resultant waveform. Care must be taken to collect signals

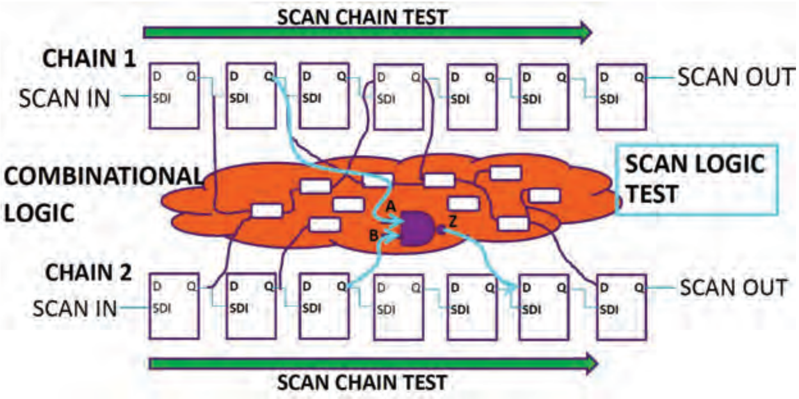
SCAN CHAIN TEST
CHAIN 1
SCAN IN
D
Q
SDI
SCAN OUT
COMBINATIONAL
LOGIC
SCAN LOGIC
TEST
A
B
Z
CHAIN 2
SCAN IN
SCAN OUT
SCAN CHAIN TEST

Fig. 2 Scan flops connect to most digital circuitry directly or through a combinational logic path. When the flops toggle, the stimulus propagates to the logic elements under inspection.

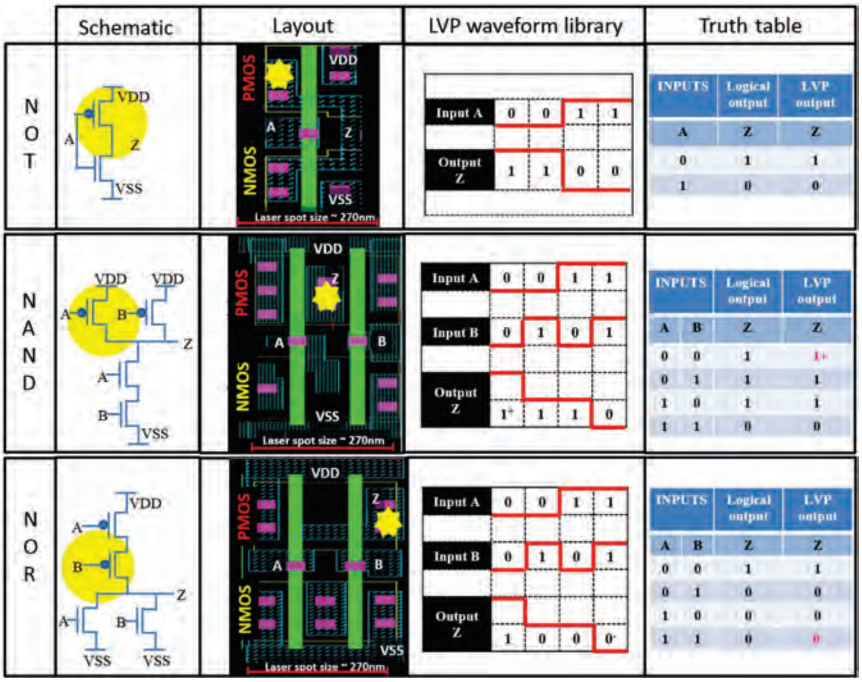
Schematic
Layout
LVP waveform library
Truth table
NOT
VDD
A
Z
VSS
PMOS
NMOS
Laser spot size ~ 270nm
Input A 0 0 1 1
Output Z 1 1 0 0
INPUTS
Logical output
LVP output
A Z Z
0 1 1
1 0 0
NAND
VDD VDD
A B Z
Input A 0 0 1 1
Input B 0 1 0 1
Output Z 1* 1 1 0
A B Z Z
0 0 1 1*
0 1 1 1
1 0 1 1
1 1 0 0
NOR
VDD
VSS VSS
Input A 0 0 1 1
Input B 0 1 0 1
Output Z 1 0 0 0*
A B Z Z
0 0 1 1
0 1 0 0
1 0 0 0
1 1 0 0

Fig. 3 Summary of the CLA library of an inverter, a 2-input NAND, and a 2-input NOR cell. The first two columns show the schematic and layout, with the yellow polygon indicating probe position. The last two columns show the LVP library and truth table. While an inverter has only two LVP states, the NAND and NOR cells have multiple states due to the modulation effects of multiple interacting transistors within the probe spot.

from the same position when comparing against a reference waveform.

BUILDING UP A REFERENCE LVP LIBRARY

Once an optimum probe position is selected for a cell—usually on the active device that drives the output—a reference library can be built. If a combinational cell has N-inputs, the number of elements in the truth table = 2^N. Therefore, a 2-input NAND gate will need at least four vectors, a 3-input NAND will need eight, and so on.

The following list summarizes the CLA steps:

1. The load cycles of a scan logic pattern are usually looped with care to ensure the scan flops connected to the cell of interest are toggled frequently.
2. The inputs of the cell are first probed at a random interval of the loading cycle using a relatively large time span.
3. A suitable time window is selected in which the toggles create all the combinations needed to completely fill up the truth table.
4. A reference library is built from known good cells and compared against the cell under inspection.

LVP LIBRARY

Most standard cells have complementary NMOS and PMOS transistors, either of which can describe the cell's logic state. The CLA library presented in Fig. 3 is based on signals from the PMOS, but a similar one can be

(continued on page 14)

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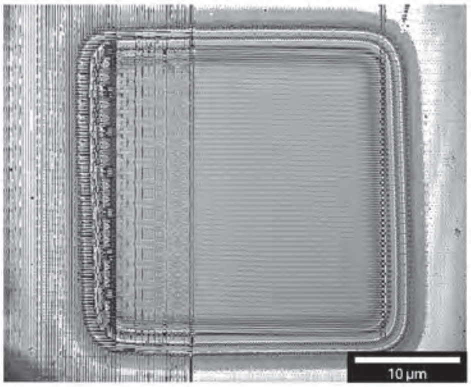

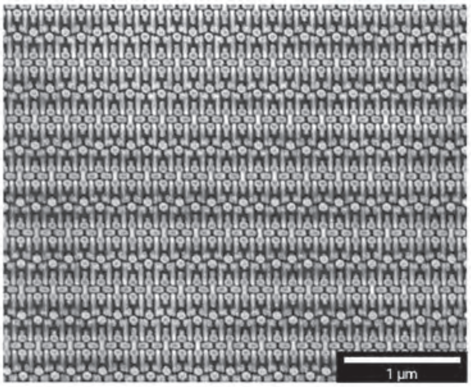

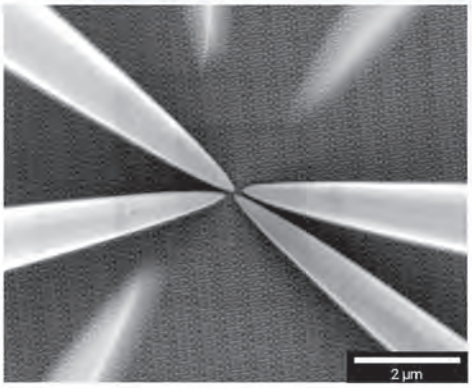

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COMBINATIONAL LOGIC ANALYSIS WITH LASER VOLTAGE PROBING

(continued from page 12)

constructed with NMOS as well. The first two columns contain the schematic and layout of the cell. The last two columns contain the LVP waveform library and the truth table. Note that unlike a regular truth table, this table contains an additional column for LVP output. This is because LVP output can contain multiple levels for a single logic output depending on the modulation from a number of transistors under the optical probe.

For example, consider the NAND gate. Output Z is sandwiched between two PMOS transistors. The spot size of the laser is big enough to cover both PMOS transistors. Total modulation includes the common drain between transistors, as well as the channel regions, assuming the sources are at constant voltage (VDD). When transistors in parallel are turned on at the same time, the number of gates turned on does not make any difference to the voltage on the drain. Therefore, the electrical logic stage of the output does not change and the voltage on the drains are constant. However, the amount of modulation depends not only on the voltages, but also the number of transistors that are ON within the probe spot. As a result, multiple LVP logic states corresponding to the same electrical logic state of the cell can be observed in the output waveform of Fig. 3c. To match the electrical truth table, when both transistors are on, the LVP state is denoted as 1^+, and when only one of the transistors turns on, the LVP state is denoted as 1. The minimum state occurs when neither transistors contribute to the modulation, i.e., when both are OFF.

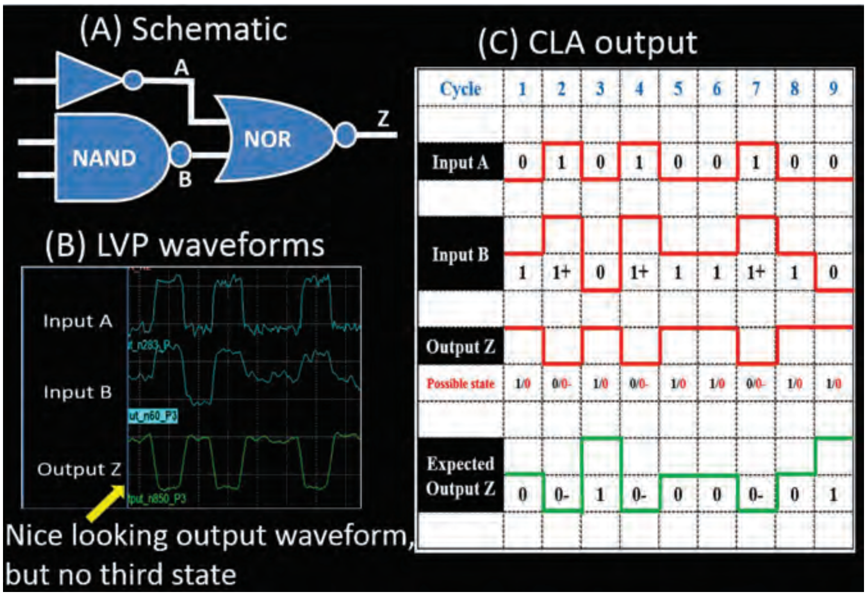
Another interesting observation is that the modulation depends on whether the transistor is turned ON or OFF, irrespective of whether the source is connected in series or in parallel to another transistor. While in series, the modulation due to the gate voltage will still affect the LVP signal even though the series transistor is turned OFF. This is clearer when we consider the 2-input NOR gate. Here, the three LVP states are 1, 0, and 0^- to match the logical truth table.

If we compare the waveform libraries of the NOR gate in Fig. 10 with the NAND gate in Fig. 7, they look the same. As mentioned earlier, the modulation by the gate does not depend on whether the transistors are in series or in parallel. Consequently, the strongest modulation occurs when both transistors are ON, which is denoted as the "1" state. When both transistors are OFF, modulation is the weakest and is denoted a "0^-" instead of "0." This helps match the electrical truth table of the NOR gate to the LVP library.

A couple of simple 2-input standard cells have been presented here. More complex logic gates can be approached in a similar manner. Knowing which waveforms to expect from logic gates is extremely beneficial to fault isolation. The following case study showcases the value of employing CLA in conventional fault isolation.

CASE STUDY

The device under test failed scan logic and the schematic, as shown in Fig. 4. Schematic A is comprised of an inverter and a 2-input NAND cell feeding to a 2-input NOR



Nice looking output waveform, but no third state

Cycle	1	2	3	4	5	6	7	8	9
Input A	0	1	0	1	0	0	1	0	0
Input B	1	1+	0	1+	1	1	1+	1	0
Output Z									
Possible state	1/0	0/0-	1/0	0/0-	1/0	1/0	0/0-	1/0	1/0
Expected Output Z	0	0-	1	0-	0	0	0-	0	1

Fig. 4 **Case study highlighting use of CLA. (a) Schematic of failing circuitry. (b) LVP waveforms at the drivers of the inputs and the NOR output indicate no obvious failing signature except the missing third state predicted by CLA. (c) CLA results show logical mismatches between output waveforms collected and the expectations based on the library.**

cell. Waveforms were collected from the PMOS drivers of each of the cells and are shown in Fig. 4b. The output of the NOR shows sharp transitions and flat levels, which usually occur on good transistors. However, through CLA (Fig. 4c), three states were expected, but were completely missing. This mismatch in the LVP state indicated that the NOR gate contained a defect, a metal short verified by physical FA. This case study shows that waveforms with flat states and sharp transitions, which are usually exhibited by good nets, could still be defective. Therefore, a thorough investigation of the cell, by observing all input combinations, is necessary to ensure functionality. An exhaustive truth table construct helps identify the cycles at which the signal clearly does not match expectations, thereby further isolating the potential failing locations. Finally, an entire analysis could be completed using just three waveforms from each of the output drivers, underlining the efficiency of this process.

CONCLUSIONS

Shrinking technology footprints create increasing spatial resolution challenges for laser voltage probing. It is useful to consider signals from multiple transistors within combinational elements at the same time. Combinational logic analysis is a process by which LVP signals for combinational elements such as NOR and NAND are better understood. This process speeds up laser voltage probing, despite restrictions in spatial resolution. In addition to accelerating the process, it increases the reliability of fault isolation and helps to further narrow down the defect.

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Venkat Ravikumar is a senior member of the technical staff at Advanced Micro Devices (AMD) and spent the past decade working on fault isolation at the Device Analysis Laboratory. His key expertise is in bring-up and use of tester-based fault isolation techniques such as photon emission, soft defect localization, and timing analysis tools, such as time-resolved emission, laser voltage probing, and its derivatives. Graduating from the National University of Singapore with an M.S., he is currently pursuing a Ph.D. at Singapore University of Technology and Design, in addition to his role at AMD.

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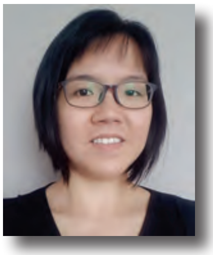

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GUEST EDITORIAL

CONTINUED FROM PAGE 2

techniques. The zero-defect quality and high reliability requirements in the automotive industry drive the improvement of analysis methodology and strategy to enable successful analysis of every failure. Involvement during all product phases to improve FA and support design for successful FA is complemented by a third factor: Competence management across all product levels, from application-specific integrated circuit to module to component. The intertwined and complex nature of automotive components and their environment requires deep knowledge of the whole ecosystem to meet high reliability and zero-defect quality targets. Returning valuable information from FA to all product levels can further improve this approach. Engineering of FA integration and FA processing enables automotive products to be built to meet ambitious customer expectations. This capability is unique to system suppliers with experience in design and manufacturing from semiconductor technology to complex automotive systems.

NOTEWORTHY NEWS

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The IPFA 2018 Organizing Committee is chaired by Szu Huat Goh of GlobalFoundries, Singapore. The symposium is technically cosponsored by the IEEE Electron Device Society and IEEE Reliability Society.

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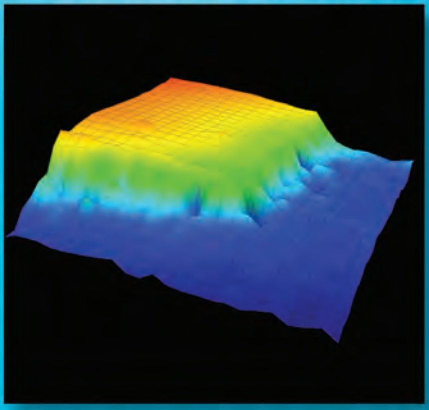

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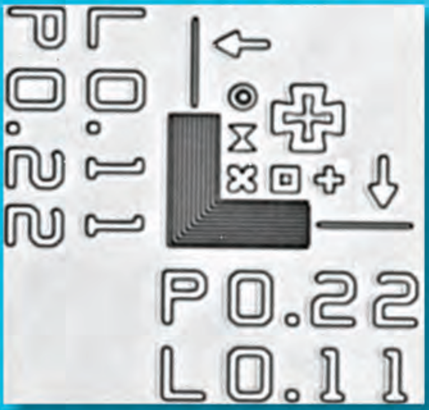

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DIAGNOSTIC TECHNIQUE SELECTION FOR SRAM LOGIC TYPE FAILURES

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INTRODUCTION

Static random access memory (SRAM) is often chosen as the process qualification vehicle during technology development, and consequently, failure analysis of SRAM is the main feedback for process improvement and yield learning.[1,2] Because SRAM is very dense and has small features, its functionality is highly sensitive to process variation. Another advantage of using SRAM as a process qualification vehicle is that single-bit failure and many multi-bit failures can be precisely localized by a functional test and are easy for physical failure analysis. Generally, the defect causing a single-bit failure is precisely located at the failing bit site. In the case of paired-bit or quad-bit failures, the defect is often found at their shared stacked interconnects. For such failures, the passive voltage contrast (PVC) technique,[3] scanning electron microscope (SEM) inspection, focused ion beam (FIB) cross-section, and electrical probing by atomic force probe[4] or SEM in-chamber probe[5] can be employed to locate and image the defect. Since SRAM is organized as an array structure of single-bit storage cells, which are accessed and selected through the hierarchy bit-line (BL) and word-line (WL) decoder schemes, any defect in the address decoder circuitry will result in a uniquely failing spatial pattern. In general, these spatially patterned failures can be classified into three categories, namely bit-line, word-line, and entire block failure. It is also worth noting that in modern SRAM designs, the entire array becomes vulnerable to a defect within the control scan chain. A defect within such circuitry may cause the whole SRAM device to malfunction or may prevent functional testing of the array.

In this article, SRAM failures caused by defects in the address decoder or scan chain circuitry are categorized as SRAM logic type failures. Conventional failure analysis methods for single and multiple-bit failures are not effective for these types of failures. Consequently, more detailed fault isolation work is required prior to starting destructive physical failure analysis. Many diagnostic techniques such as photon emission microscopy (PEM),[6,7] thermally induced voltage alteration (TIVA),[8,9,10] optical beam induced resistance change (OBIRCH),[8,11] critical parameter analysis (CPA)[12,13] and laser voltage imaging (LVI)[14,15]/laser voltage probing (LVP)[16,17] are available for the fault isolation work. These techniques offer alternatives for stimulating the SRAM device and detecting a response, and therefore provide a means for localizing a variety of faults for different failure types. Thus, selecting the right diagnostic technique for a particular SRAM logic failure is important for an efficient and successful analysis.

COMMON DIAGNOSTIC TECHNIQUES

The proper selection of a fault isolation technique for a specific SRAM logic type failure requires an understanding of available techniques. The most common and frequently used fault isolation techniques include: PEM, TIVA/ OBIRCH, CPA, and LVI/LVP. Among these diagnostic techniques, the PEM setup is the simplest, involving an optical microscope equipped with a very sensitive photon detector (Fig. 1). PEM can pinpoint the defective location by detecting a very faint photon emission from the defective circuit when a device under test (DUT) is electrically powered. Photon emission occurs as a result of the transition of carriers from a higher energy state to a lower energy state and is generally associated with forward or reverse biased PN junctions, transistors in saturation, or dielectric breakdown.[7] Thus, the faults isolated by PEM are more likely to occur at the front end of line (FEOL), except for the case of a floating gate, which can be due to an open fault in the back end of line (BEOL).

Both TIVA/OBIRCH and CPA are laser stimulation techniques,[8] which capture the change in the electrical characteristic of the circuit being illuminated by a focused laser beam. The effect is two-fold and varies according to the laser's wavelength. The 1064-nm laser causes more generation of electron-hole pairs, while the 1340-nm laser causes more thermal effect. Both are effective in fault localization and can be applied to various laser stimulation techniques to capture the changes in different electrical characteristics. TIVA captures the change in voltage of a device biased at a constant current through the thermal-conductive effect, while OBIRCH monitors the change in current of a device biased at a constant voltage. Figure 2 is a diagram of a TIVA setup. Both TIVA/OBIRCH are capable of isolating ohmic short faults due to large resistance changes caused by the thermal effect when a near-infrared laser shines on the shorts.

CPA, also known as soft defect localization (SDL),[18] is a tester-based laser stimulation fault isolation technique. Figure 3 is a diagram of a CPA setup. CPA captures the change between the fail and pass status of a device under a repeated test pattern loop while the laser is scanned across the device. As the laser moves pixel-by-pixel, the tester provides a pass/fail signal back to the laser scanning microscope. CPA can be labeled "positive" or "negative" depending on the laser induced change between the pass and fail status of the device under test. If the DUT is operating in a failing condition without the laser shining, and the laser causes it to pass, the CPA is considered "positive." If the DUT is operating in a passing condition, and the laser causes it to fail, the CPA is considered "negative." Therefore, CPA is the most suitable method for isolating the faults of soft failures.

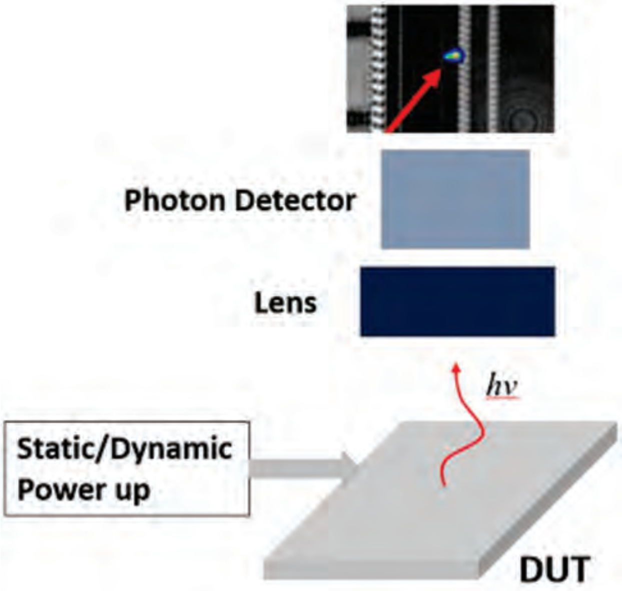


Fig. 1 **Diagram of a PEM setup.**

Although a laser scanning microscope is also employed for LVI/LVP, the technique is quite different from TIVA or CPA. Instead of detecting the electrical characteristic change through the biased pins on the DUT, this technique monitors the modulation in the reflected laser beam from the active regions, such as drain and channel through silicon backside. Figure 4 is a simple diagram of the LVI/LVP setup. The LVI detector collects data in the frequency-domain from numerous points in the field of view. The resulting image (frequency map) can be overlaid onto the reflected image, creating a map showing

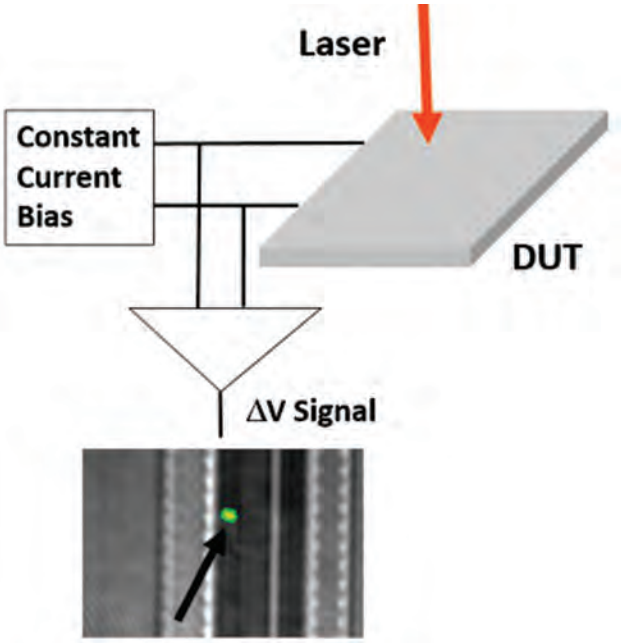


Fig. 2 **Diagram of a TIVA setup.**

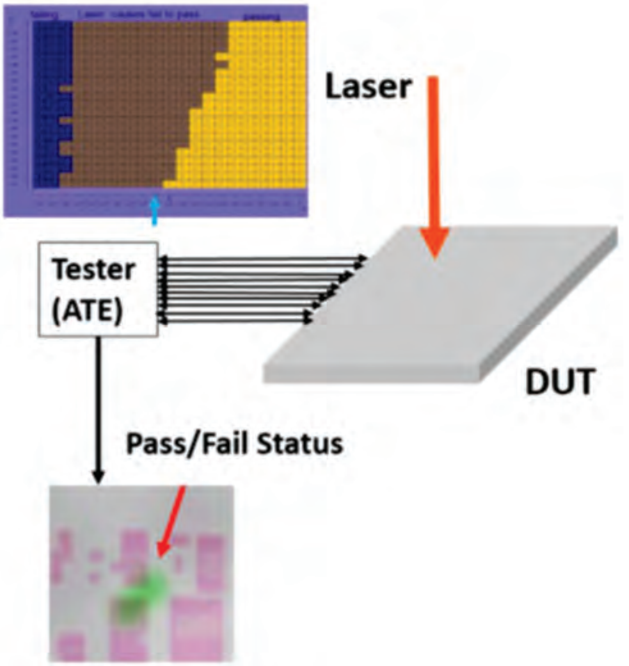


Fig. 3 **Diagram of a CPA setup.**

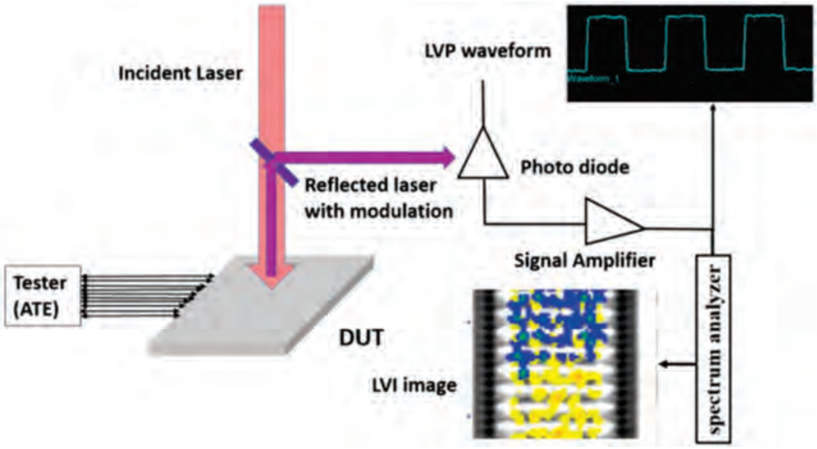


Fig. 4 **Diagram of an LVI/LVP setup.**

transistors switching at a given frequency. It is convenient to run the DUT's clock and data at different frequencies, so that both signal paths can be individually and simultaneously mapped. The unique ability to map periodic signals in a DUT makes LVI well suited for scan chain diagnosis because the data propagation through the scan chain is clocked with a periodic signal. The LVI map can easily identify the broken point for a scan chain failure, whether the defect is in the data signal path or in the clock signal path. LVP enables acquisition of a waveform in the time domain at a specific physical location. For example, waveforms may be obtained at the broken scan chain location identified with LVI. Through layout tracing and waveform comparison with a reference sample, the fault location may be narrowed down to an inverter or a node. Because the scan chain concept has been incorporated into SRAM design, scan chain failures are additional failure modes in SRAM, and these require fault isolation prior to PFA. For such failures, LVI/LVP is the primary choice of diagnostic techniques.

DIAGNOSTIC TECHNIQUE SELECTION: CASE STUDIES

The features of each diagnostic technique determine its application. PEM and TIVA/OBIRCH are suitable for hard failures. PEM analysis is often performed first because its setup is simpler than that of TIVA/OBIRCH. As PEM and TIVA/OBIRCH are sensitive to different defect types, whenever PEM analysis fails to detect an abnormal emission site, TIVA/OBIRCH analysis is attempted. For soft failures, CPA is naturally the right choice, as it captures the change between pass and fail status caused by laser stimulation. LVI/LVP is the primary choice for SRAM scan chain failures because it has the unique capability of mapping the periodic signal in a DUT. In this section, four cases of SRAM logic type failures analyzed with the appropriate diagnostic techniques are presented.

CASE #1: PEM ANALYSIS FOR A BLOCK FAILURE

The first case study is a block 512BLX128WL failure for an 8Mbit SRAM. Figure 5 shows the failure bitmap of two segments (1Mbit per segment) of the 8Mbit SRAM. The dark rectangular shape represents the block 512BLX128WL failure. First, static PEM analysis through backside silicon was performed. It failed to detect any abnormal emission site because static power-up could not exercise the failure. So dynamic PEM analysis, running a repeating functional

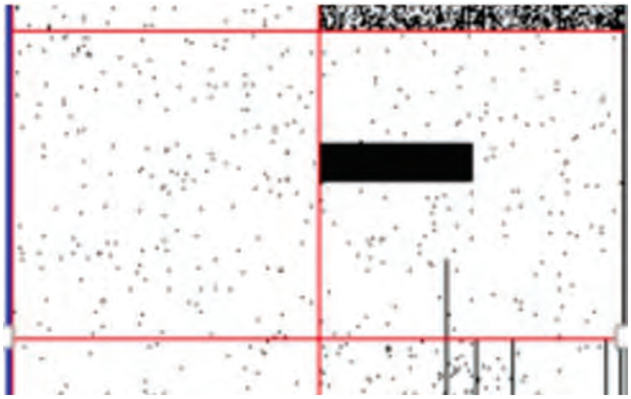


Fig. 5 **Failure bitmap showing a block 512BLX128WL failure in an 8Mbit SRAM.**

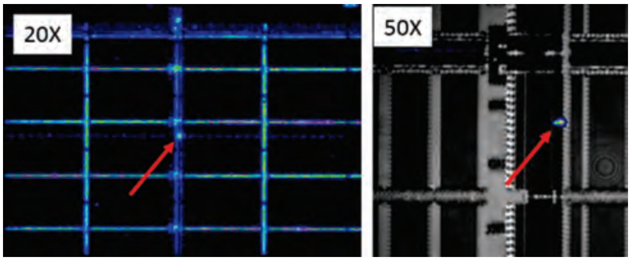


Fig. 6 **PEM analysis image showing an emission site at word-line driver area for the block 512BLX128WL failure.**

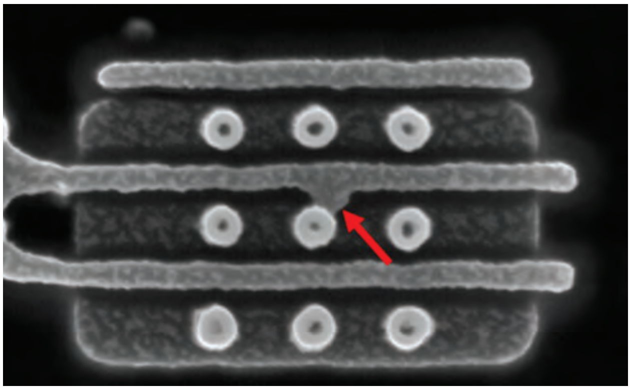


Fig. 7 **SEM image showing a poly micro-mask, causing a poly-contact short.**

test pattern, was performed. An emission site associated with the block failure was detected at the word line driver area, as shown in Fig. 6 (20× at left and 50× at right). After the failing area was located, the sample was subjected to layer-by-layer deprocessing and SEM inspections. At the polysilicon gate level, the SEM inspection found a poly micro-mask defect, causing a poly-contact short at the emission site as shown in Fig. 7. The defect forced the transistor into saturation, leading to photon emission.

CASE #2: TIVA ANALYSIS FOR A BLOCK FAILURE

Another 8Mbit SRAM chip suffered from a block 128BLX128WL failure. Fig. 8 shows a two-segment failure bitmap, where the dark square shape represents the block 128BLX128WL failure in a 1Mbit segment. Again, first backside PEM analysis was performed. Neither static nor dynamic PEM analysis could detect abnormal emission on the failing segment when compared to a good segment. Then, backside TIVA analysis with 1340 nm laser stimulation was performed. Figure 9 shows the TIVA analysis image (10× on top, 100× on bottom). It is clear that an abnormal signal is present at the word line rebuffer area correlating to the block 128BLX128WL failure. Based on the TIVA analysis result, follow-up physical analysis was performed. At metal 1 (M1) level, SEM inspection found a metallic particle bridging two M1 lines, as shown in the SEM backscattered electron (BSE) image in Fig. 10. Because the defect in the BEOL caused an ohmic short, it is reasonable that neither static nor dynamic PEM analysis detected any abnormal emission. Instead, the TIVA technique was successful in localizing the defect. When the 1340-nm laser illuminated the defect, the thermal effect caused a large change in its resistance, enabling TIVA to capture the location.

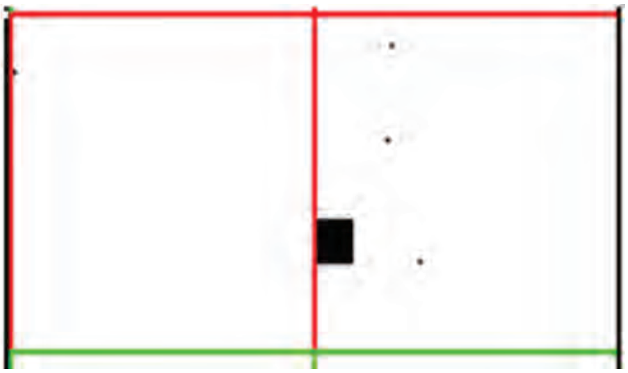


Fig. 8 **Failure bitmap showing a block 128BLX128WL failure in an 8Mbit SRAM.**

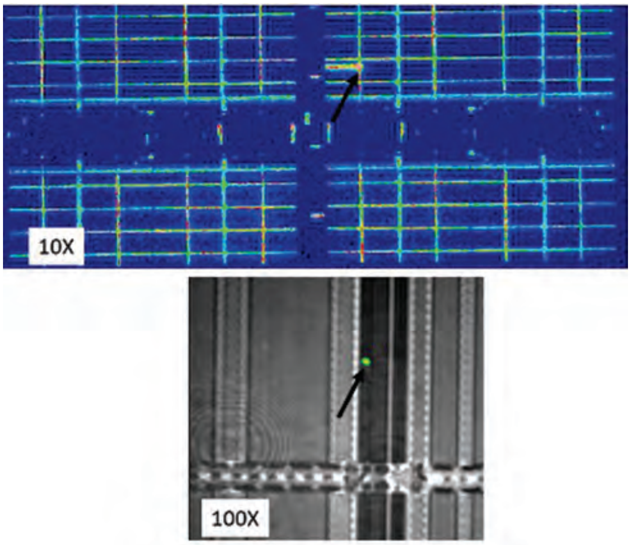


Fig. 9 **TIVA analysis image showing response to the laser at the word-line re-buffer area for the block 128BLX128WL failure.**

CASE #3: CPA ANALYSIS FOR A SOFT BLOCK FAILURE

The third case study is a soft block failure. A block 192BLX512WL in a 48Mbit SRAM failed at low voltage only, as shown in Fig. 11. Because this case was a soft failure, CPA was the right choice for its fault isolation. First, a shmoo plot was generated to find the exact V_{DD} voltage where the failure occurred and to identify the pass/fail

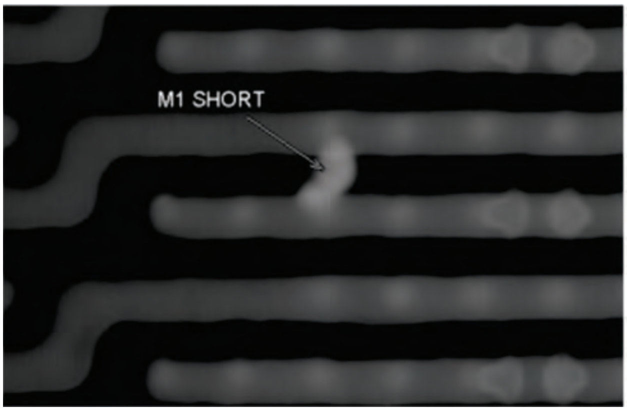


Fig. 10 **SEM BSE image showing a metallic particle bridging two M1 lines.**

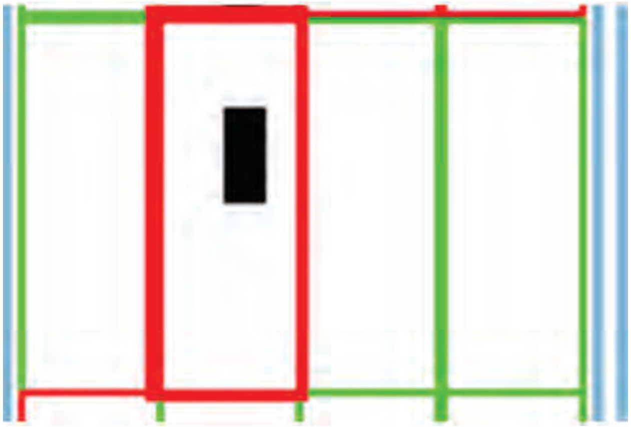


Fig. 11 **Failure bitmap showing a soft block 192BLX512WL failure in a 48Mbit SRAM.**

boundary of the soft block failure. Next, CPA analysis was performed with the device under a repeating test at the failing condition close to the voltage of pass/fail boundary. Figure 12 shows where a CPA spot was detected in a bit-line decoder area with a positive CPA experiment. Later, electrical nanoprobing and physical analysis showed Si dislocations at the interface of channel SiGe and Si, causing source-drain leakage in PFET P6 (Fig. 13). Why did a leaky P6 cause a positive CPA spot near N6? N6 and P6 formed a voltage divider, as shown in Fig. 14. When the laser illuminated N6, it caused the N6 I_{on} to be higher than normal, which compensated for the leakage in P6, allowing the circuit to pass from its initial failing condition.

CASE #4: LVI/LVP ANALYSIS OF AN SRAM SCAN CHAIN FAILURE

Today's SRAM devices usually include a simple scan chain, which is used for setting test conditions or internal functionality. At the beginning stage of technology development, scan chain failures are often the main yield detractors and prevent further testing of SRAM functionality. The fourth case study involves a 32-bit configuration register scan chain failure in an SRAM device. Because a functional test could not identify the failing register, LVI/LVP was used to isolate the exact fault location. First, LVI diagnosis was performed to map the clock and data signals for a reference scan chain, as shown on the left side of Fig. 15. The yellow clock signal and blue data signal are clearly distributed across the entire scan chain. Next, LVI diagnosis was performed on the failing scan chain, and the acquired LVI image is shown on the right side of Fig. 15. It is clear that the clock signal is fine, as it continues through the entire scan chain, while the data signal propagation stops at register 10. The high-magnification LVI image shown on the left side of Fig. 16 indicates that the data signal is still strong at point 4, but faint at point 6, and then disappears beyond that. LVP waveforms were collected from points 4, 6, and 8, as shown on the right side of Fig. 16. The data signal is still strong at point 4, but is corrupted at point 6, consistent with the observation on the LVI image. The LVP waveform collected from point 8 is the clock signal, which is good. So, the fault location of the scan chain failure is isolated to a small area in register 10, suitable for PFA. Subsequent PFA found hollow contacts near point 6.

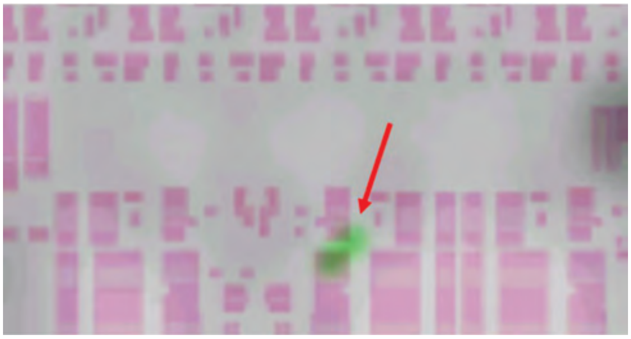


Fig. 12 **CPA analysis showing a CPA spot in a bit line decoder area.**

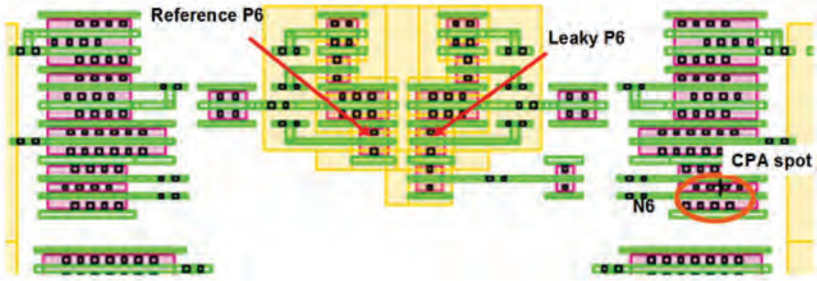


Fig. 13 **Layout view with the leaky PFET and CPA spot labeled.**

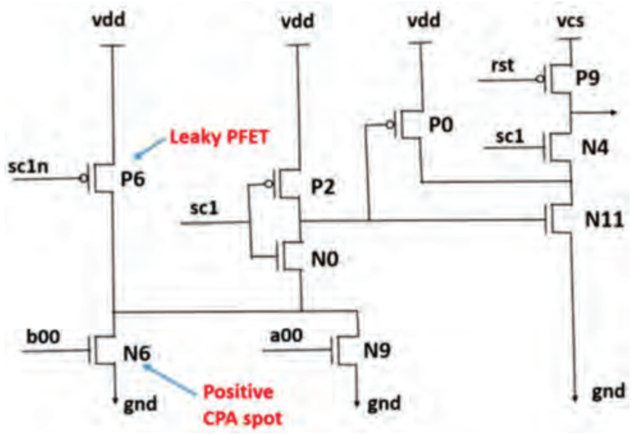
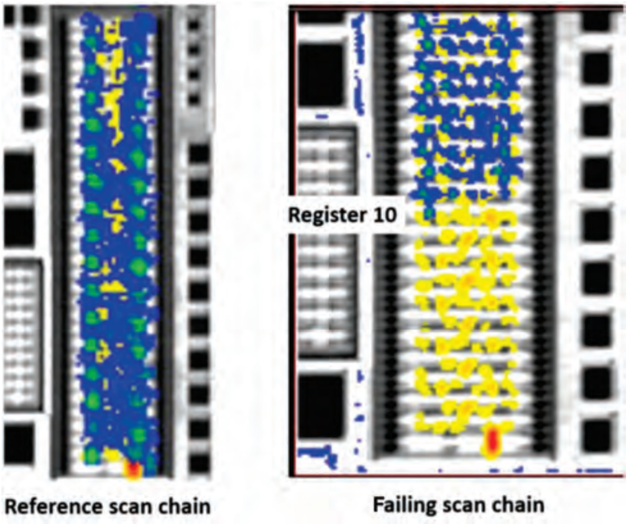


Fig.14 **The bit-line decoder schematic with leaky PFET and CPA spot (NFET) labeled.**

CONCLUSION

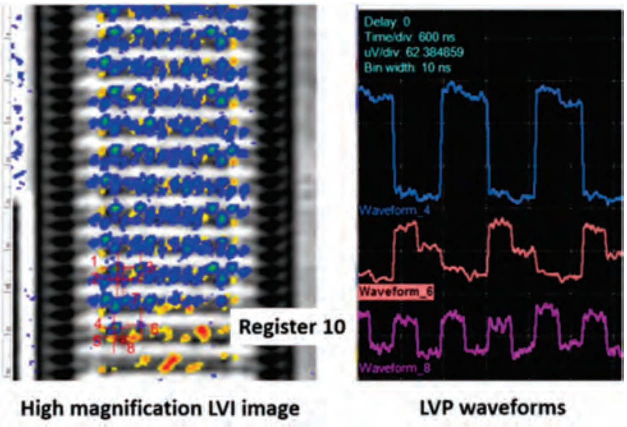
Due to the SRAM array architecture in which bitcells are accessed through a hierarchy of bit-line and word-line decoder schemes, and with the introduction of scan chain design, SRAM devices often suffer from logic type failures. For such failures, a functional test alone cannot localize the defective area. More detailed fault isolation work is required prior to destructive physical failure analysis. Many diagnostic techniques are available for the fault isolation work. These techniques employ alternatives for stimulating the SRAM device and detecting a response and therefore provide a means for localizing various faults for different failure types. Thus, careful selection of diagnostic techniques for a particular SRAM logic failure is important for an efficient and successful analysis. For certain cases, a combination of two or more selected diagnostic techniques may be beneficial.



Reference scan chain

Failing scan chain

Fig.15 **LVI image mapping the clock and data signals for a reference scan chain and failing scan chain. Yellow for clock signal and blue for data signal.**



High magnification LVI image

LVP waveforms

Fig. 16 **High-magnification LVI image and LVP waveforms collected from points 4, 6, and 8 in register 10.**

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NOTEWORTHY NEWS

NANOTS 2018

The 38th annual NANO Testing Symposium (NANOTS 2018) will be held **November 19-20** at the KFC Hall, Kokusai Fashion Center, in Tokyo. NANOTS is one of the leading technical symposiums for discussing solutions that improve the testing process of nanoscale devices and materials. The two-day event will consist of a symposium with a special invited talk, a special session, technical sessions, a commercial session, an equipment exhibition, and an evening session.

Presentations on original, noncommercial, and nonpublished works are being solicited. Papers for the special session and technical sessions are peer-reviewed and selected based on a clear outline of problem, analysis, solution/results, and conclusion. **Abstracts are due July 27,** with abstract submission beginning in June.

NANOTS is sponsored by the Institute of NANO Testing in cooperation with the Institute of Electronics, Information, and Communication Engineers, the Japan Society of Applied Physics, the Reliability Engineering Association of Japan, and the Union of Japanese Scientists and Engineers.

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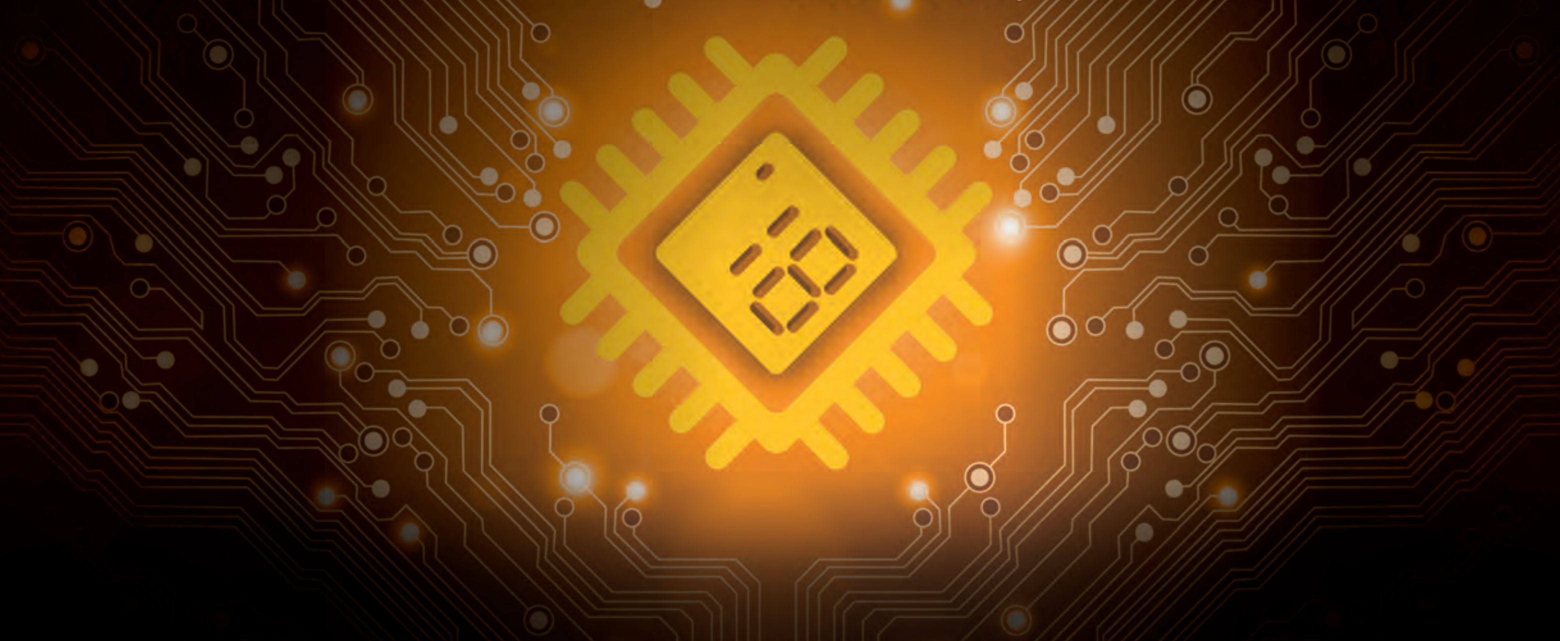

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RECENT INNOVATIONS IN EX SITU LIFT OUT APPLICATIONS AND TECHNIQUES

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INTRODUCTION

The ability to apply focused ion beam (FIB) milling to just about any material for site-specific scanning/transmission electron microscopy (S/TEM) was realized in the mid 1990s to early 2000s. The first technique used to extract or "lift out" site-specific FIB milled specimens, now commonly referred to as "ex situ lift out" (EXLO), also proved successful for many different materials.[1-4] With the EXLO method, specimen extraction is performed outside of the FIB instrument (i.e., not with an in situ probe) using a light optical microscope and micromanipulator station. The semiconductor industry immediately embraced EXLO and continues to rely on this technique due to its ease of use, reproducibility, and high throughput. For example, it is possible to lift out and manipulate 20 specimens (or more) per hour using EXLO.[5]

The EXLO technique relies on the physics of adhesion forces, and more specifically, van der Waals forces (i.e., not electrostatic forces as previously believed) to transfer a FIB milled specimen confined within its trench to a specimen carrier using a glass probe micromanipulator.[6] S/TEM EXLO specimens are usually manipulated to carbon, formvar, or holey carbon coated 3-mm grids or similar. In addition, S/TEM EXLO specimens can also be manipulated to MEMS devices for heating, electrical, or other in situ S/TEM observation of materials,[6,7] or more recently, to slotted half-grids.[6] The slotted half-grids allow additional processing of EXLO specimens, such as FIB milling for backside thinning, including low energy FIB or ion milling.[6,8-9] These innovations and advances in EXLO are detailed below.

EXLO AND VAN DER WAALS FORCES

As previously shown,[6] the EXLO method relies on adhesion forces, and specifically van der Waals (VDW) forces, to pick up a specimen and manipulate it to a carrier of choice. Figure 1 compares the adhesion forces and the force of gravity acting on a typical Si FIB specimen with dimensions of 10 µm × 5 µm × 100 nm and a glass probe manipulator pulled to 2 µm in diameter. Glass probes are typically used because they are inexpensive, easy to prepare, and flex without deforming during the lift out and manipulation process. A single glass needle may be used to manipulate tens of samples or more. As shown in

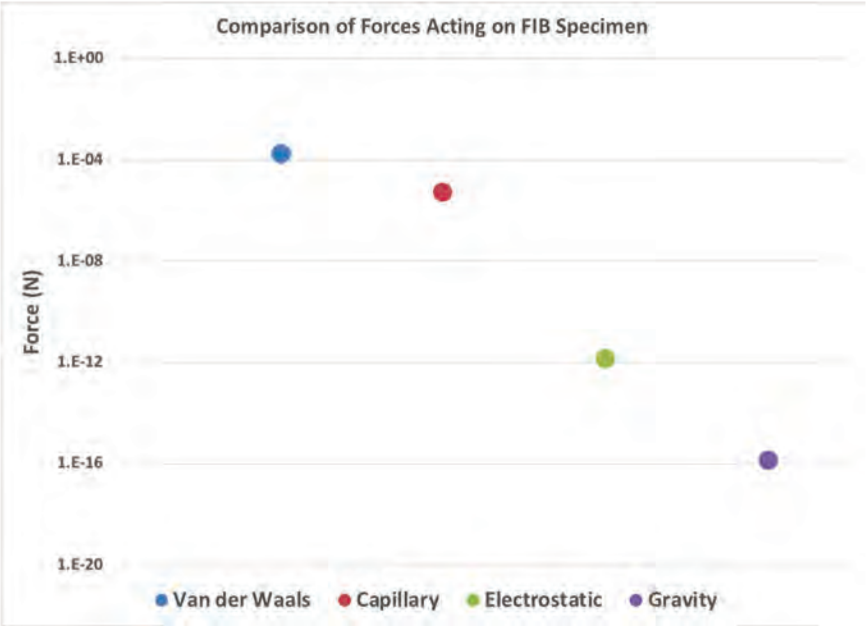

Fig. 1 **Comparison of adhesion forces and force of gravity acting on a Si FIB specimen 10 µm × 5 µm × 100 nm.**

Fig. 1, VDW forces are more than one order of magnitude large than capillary forces, more than eight orders of magnitude larger than electrostatic forces, and more than 13 orders of magnitude larger than the force of gravity.

VDW forces are directly proportional to the Hamaker constant, which varies by two orders of magnitude across the periodic table.[6] Thus, a change in material is essentially irrelevant for the EXLO method and van der Waals forces dominate the adhesion process of the smooth FIB specimen manipulated with a smooth probe surface. As a rule, excessive repulsive or attractive electrostatic forces should be avoided whenever possible. An easy way to avoid electrostatic forces, relying solely on VDW forces, is to metallize only the glass probe. This may be accomplished by sputter coating a conductive layer on the glass probe[6] or by dipping the probe into permanent marker ink (e.g., carbon or conductive particles in a solvent).[9,10] Figure 2 shows the solid glass probes used in EXLO where the probe labeled (a) has been dipped into and painted with permanent ink, and the probe labeled (b) has no coating applied.

Thus, the EXLO process works by optimizing the surface area. The specimen is easily extracted from its trench because the probe-to-specimen surface area is greater than the surface area created by the specimen edges touching the trench sidewalls. The specimen releases from the probe and adheres to the carrier because the surface area between the specimen and carrier becomes larger than the surface area between the probe and specimen. Therefore, the specimen will remain either in the trench, on the probe, or on the carrier, unless acted upon by larger VDW or other forces.

REPRODUCIBILITY AND THROUGHPUT WITH EXLO

EXLO is easy to learn and master, and as previously mentioned, is highly reproducible and fast. A series of images illustrating this point is shown in Fig. 3, which includes still images acquired from a real-time video during the lift out and manipulation of two specimens to a carbon-coated grid. The specimens are ~12-15 μm long and the grid square openings are ~40 μm wide. Note the images include time stamps in minutes:seconds:milliseconds showing that two lift outs may be manipulated in < 5 minutes.[5,6] This translates to the achievable manipulation of 24 samples or more per hour. Ease of use aided by a semi-automated instrumentation processes helps achieve this speed.

DEVELOPMENT OF SLOTTED HALF-GRIDS: NO CARBON FILM NEEDED

Over the years, a perceived disadvantage to EXLO arose due to supposed limitations in S/TEM analysis and the ability for further FIB or ion milling due to the presence and interference of the thin carbon film support. However, much S/TEM work can be performed through the carbon film or with a FIB specimen manipulated and centered over a hole in holey carbon film. In addition, recent advances in slotted half-grids allow electron transparent FIB specimens to be manipulated, supported, and protected directly by the smooth recessed regions provided by the grids.[6] The half-grid design also allows FIB specimens to be processed after EXLO manipulation, if desired. This allows for easy EXLO manipulation of

(continued on page 30)

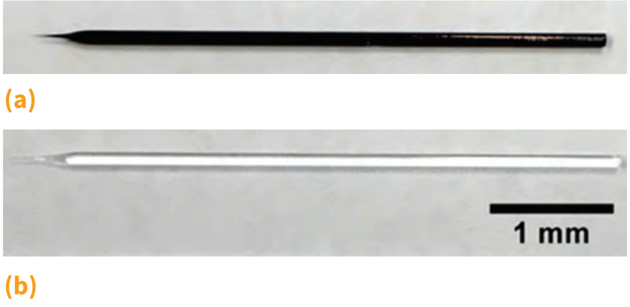

Fig. 2 **Solid glass probes used in EXLO. (a) Dipped into and painted with permanent ink and (b) as-pulled glass probe with no coating.**

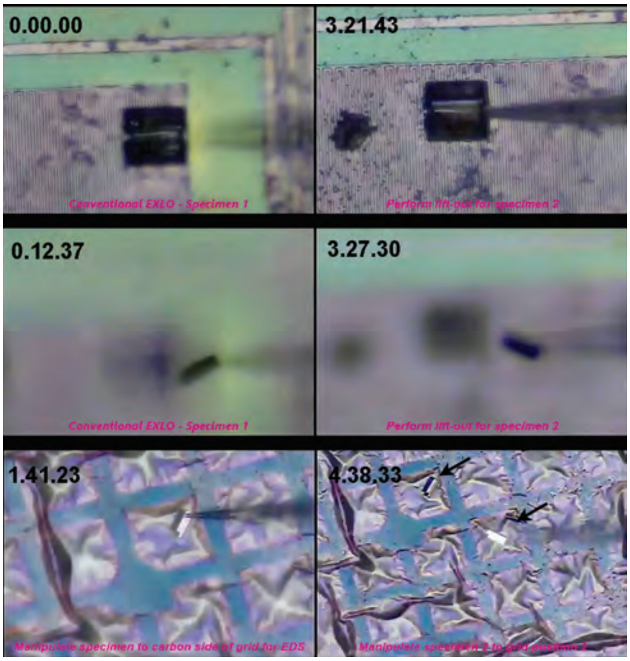
0.00.00
Conventional EXLO - Specimen 1
3.21.43
Perform lift-out for specimen 2
0.12.37
Conventional EXLO - Specimen 1
3.27.30
Perform lift-out for specimen 2
1.41.23
Manipulate specimen to carbon side of grid for EDS
4.38.33
Manipulate specimen 2 to grid position 2

Fig. 3 **Image of the EXLO process of two specimens in < 5 minutes. Still images with time stamps (minutes: seconds:milliseconds) acquired from a real-time video.[5]**

MULTIPREP
PLATEN CONTROLS
SAMPLE CONTROLS
RPM
200
ROTATION
CYCLE TIME
1:15
FLUID
OSCILLATION
FULL ROTATION
LIMIT ROTATION

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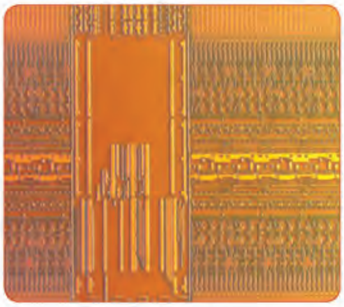
For over 20 years, the **MultiPrep™ System** has been the premiere tool for electronic failure analysis. It enables precise semiautomatic sample preparation of a wide range of materials for microscopic (optical, SEM, FIB, TEM, AFM, etc.) evaluation.

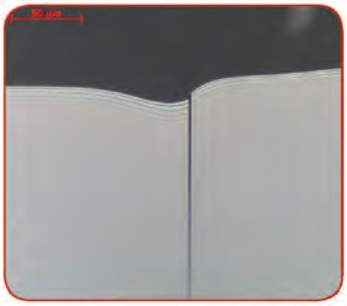
Capabilities include:

- **Parallel polishing**
- **Angle polishing**
- **Site-specific polishing**
- **Any combination thereof**

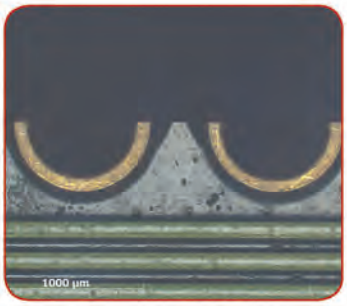
It provides reproducible results by eliminating inconsistencies between users, regardless of their skill.



IC Delayering

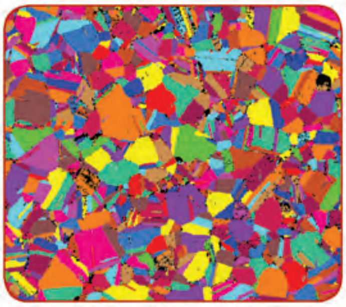


TEM Preparation



Sample Shaping

Cross-Sectioning



EBSD Preparation

Advancing Technology Through Sample Prep

RAISE
MULTIPREP

COMMON APPLICATIONS

- **Circuit Delayering**
  Supporting both front and back end failure analysis, delayering for defect review & physical FA can be done with a high level of precision.
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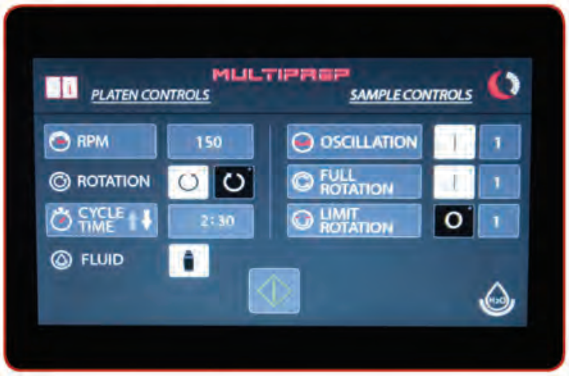
- **SIMS Analysis**
  Using parallel preparation techniques, thinning silicon or other substrates to less than 200 nm can be done to enable backside SIMS analysis.
- **TEM Cross-Sectioning**
  Prepare artifact-free, polished cross-sections ready for TEM analysis to as little as 100 Angstroms without ion-milling.
- **Serial Sectioning**
  Preparing polished regions of 2D structures at specific intervals supports 3D reconstruction and analysis.

NEW LCD Touchscreen

The 7" color LCD touchscreen is used to control all functions and is extremely easy to navigate, allowing greater efficiency among users. The intuitive interface includes icons and is optimized for productivity and function.



RPM 150

CYCLE TIME 2:30

MONOGRAIN DEFECT IN POLYSILICON GATES

(continued from page 27)

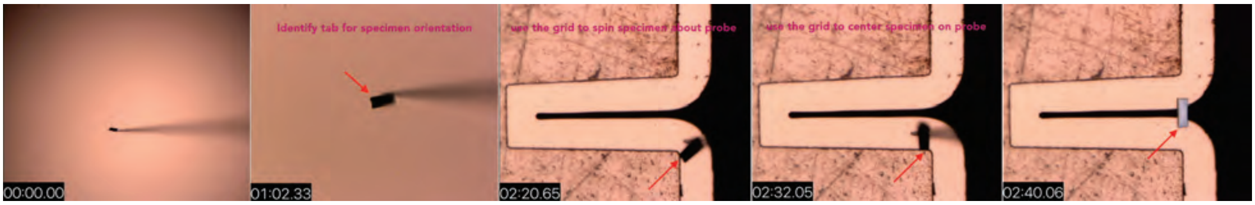
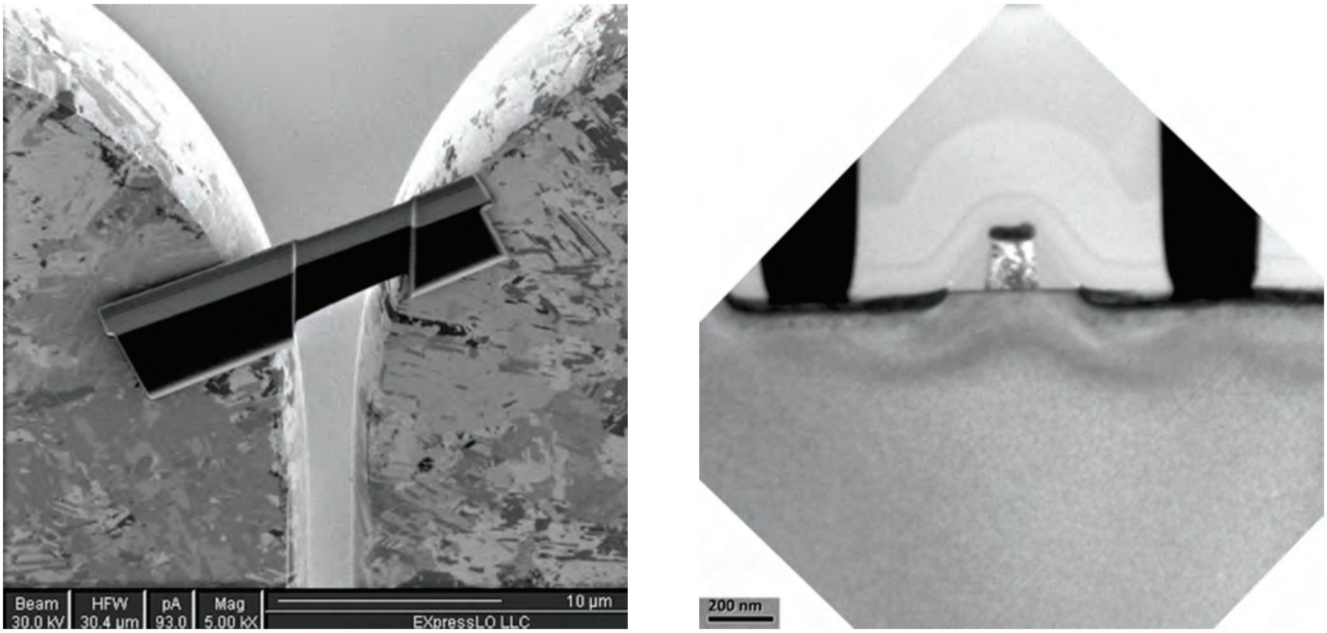

00:00.00
Identify tab for specimen orientation
01:02.33
use the grid to spin specimen about probe
02:20.65
use the grid to center specimen on probe
02:32.05
02:40.06

Fig. 4 **Still images from a real-time video with time stamps (minutes:seconds:milliseconds) showing lift out and manipulation onto a slotted Cu half-grid into a backside orientation.[12]**

"thick" (e.g., > 100 nm) specimens into the "backside" orientation (i.e., substrate "up"). Subsequent FIB thinning from the substrate or backside eliminates curtaining artifacts extending into the substrate, since FIB milling is performed from the substrate side of the specimen.[6,9] In addition, specimens manipulated to these slotted half-grids may be Ar$^+$ ion milled.[8] Further, advances in Ar$^+$ ion probe sizes and functionality allow lift out specimens to be further ion milled and thinned even when manipulated onto thin films.[11]

Figure 4 shows still images from a video acquired in real-time of a lift out sample manipulated to a slotted Cu half-grid.[12] The time stamps in minutes:seconds:milliseconds are inset in the images. The time denoted by 00:00:00 starts just a few seconds after lift out. The probe is raised above the sample surface and the specimen position with respect to the probe is assessed by adjusting the light optical microscope focus plane. The probe is rotated to position the specimen on top (at 01:02:33). At this step, the orientation of a tab in the specimen created by an asymmetric FIB undercut is also noted. This tab indicates the "top" of the FIB specimen. Then the grid slot of interest is positioned in the field of view and the probe with specimen is lowered near the plane of the grid. The grid slot edge is used to spin the specimen noting the tab orientation (at 02:20:65). The grid slot edge is also used to center the specimen on the probe (at 02:32:05). Then the probe is lowered through the slot allowing the specimen to rest flat and adhere across the open grid slot (at 02:40:06) in the desired backside orientation. The specimen may now be FIB thinned as usual, including any low energy polishing steps, avoiding curtaining artifacts.

The smooth FIB specimen also adheres to the smooth surface provided by the slotted half-grid via VDW forces. As shown in Fig. 5a, it is possible to FIB mill a specimen adhered to the grid only by VDW forces holding the specimen in place. It is also possible to Ar$^+$ ion mill a specimen on these slotted half-grids with no additional attachment



(a)

(b)

Fig. 5 **(a) FIB image of FIB milled specimen secured to slotted half-grid via only van der Waals forces. (b) TEM image of FIB specimen manipulated to slotted half-grid into a backside orientation and then further FIB milled eliminating curtaining artifacts.**

(e.g., FIB deposition) needed.[8] The TEM image in Fig. 5b shows a gate structure that was FIB milled in a backside orientation after being manipulated to a slotted half-grid. Note the absence of curtaining artifacts due to the fast and easy geometry achieved.

OPTIMIZING VAN DER WAALS FORCES

As previously mentioned, van der Waals forces are directly proportional to the surface area of the features touching. Thus, the probe surface area can be shaped to create large flat solid surfaces, thereby increasing the VDW forces by a factor of two to 10 or more.[9] The probe angle and the FIB specimen's orientation relative to the probe can be adjusted to match the orientation of the beveled probe surface. Elliptical flat surfaces or polygonal-shaped probe surfaces similar to that shown in Fig. 6 can be used to lift out the specimen and optimize the manipulation techniques to slotted half-grids.[9]

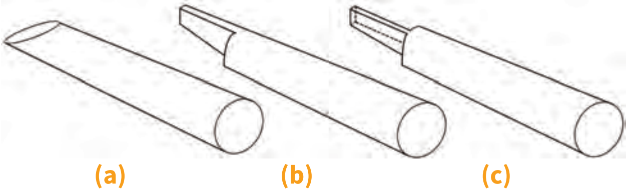


Fig. 6 **Schematic diagram of solid probe flat tip shapes (a) elliptical and (b,c) polygonal surfaces.**

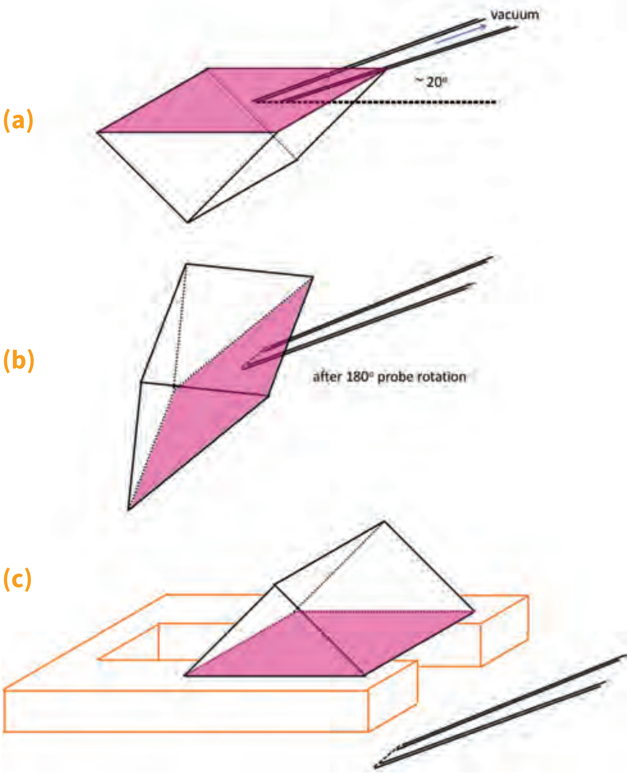


Fig. 7 **Schematic diagram of process steps for plan-view vacuum-assisted lift out including (a) lift out (b) rotation, and (c) manipulation to a slotted half-grid.**

VACUUM-ASSISTED EXLO FOR PLAN-VIEW SPECIMEN PREPARATION

In addition to using solid cylindrical or shaped probes for EXLO via VDW forces, it is also possible to supplement VDW forces by using beveled hollow glass tubes combined with vacuum suction.[6] Plan-view specimen preparation via EXLO has previously been reported.[13] Recently, the application of vacuum-assisted EXLO specifically for FIB preparation of plan-view specimens has been employed.[14] Vacuum-assisted EXLO methods aid in tracking the precise direction and orientation of the specimen during the lift out and manipulation steps. A schematic diagram of the process is shown in Fig. 7. First, the FIB is used to completely mill free a triangular prism shape from a region of interest as in Fig. 7a. Then the sample is lifted out via EXLO, using a beveled hollow probe attached to a vacuum pump to provide suction through the probe (Fig. 7a). In this orientation, the probe bevel and attack angle are orientated parallel to the lift out surface. After the specimen is secured to the probe, the probe is raised and rotated 180° (Fig. 7b). The probe is lowered and the vacuum is turned off just prior to manipulating the lift out specimen to the grid. The probe slides through the slot, allowing the specimen surface to rest on the slotted half-grid (Fig.7c). Finally, the grid with the specimen is returned to the FIB for milling on the plane of interest for plan-view analysis. S/TEM results from various materials will be presented in a future publication.[14]

SUMMARY AND CONCLUSIONS

This article presents recent advances in EXLO processes. In summary, the EXLO process is fast, easy, reproducible, and cost effective for high throughput FIB specimen preparation for conventional and high-resolution S/TEM. In addition, site-specific FIB lift out specimens can be easily manipulated via EXLO for other site-specific materials characterization methods. New EXLO methods allow for additional flexibility of techniques, eliminating the need for a thin film support, allowing for fast and easy backside thinning, reducing curtaining artifacts, and adding vacuum-assisted lift out for plan-view specimen preparation and more.

ACKNOWLEDGMENTS

EXpressLO grids and methods are covered under U.S. Patents 8,740,209 and 8,789,826. Optimization of van der Waals forces using beveled solid probes is patent pending.

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ABOUT THE AUTHOR

Lucille A. Giannuzzi earned B.E. and M.S. degrees from Stony Brook University and a Ph.D. from Penn State University. Giannuzzi has applied FIB and electron microscopy techniques to the study of structure/property relationships in numerous materials systems for over 20 years while holding positions as professor at the University of Central Florida, product marketing engineer at FEI Company, and founder and president of both L.A. Giannuzzi & Associates LLC and EXpressLO LLC (provider of EXpressLO grids and the Nicola and edu101 lift out and micromanipulation systems). She maintains professional affiliations in ASM International, AVS, ACerS, TMS, MRS, MSA, and MAS and is a Fellow of AVS and MSA. Giannuzzi has taught FIB theory and techniques to thousands of students, has over 125 co-authored publications, several FIB-related patents, several invited book chapters, and is co-editor of a book entitled *Introduction to Focused Ion Beams.* ■

NOTEWORTHY NEWS

ESREF 2018

The 29th European Symposium on Reliability of Electron Devices (ESREF 2018) will take place **October 1-5** in Aalborg, Denmark. The international symposium continues to focus on recent developments and future directions in failure analysis, quality and reliability of materials, devices and circuits for micro-, opto-, power, and space electronics. It provides the leading European forum for developing all aspects of reliability, including management and advanced analysis techniques for present and emerging semiconductor applications. All aspects related to specification, technology and manufacturing, testing, control, and analysis are addressed. In 2018, ESREF celebrates its return to Denmark after exactly 20 years. The host city is known for the efficiency and reliability of its renewable energy plants, including photovoltaic and wind turbine technologies.

For more information, visit esref2018conf.org. ■

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CENTRE de CONGRES de la CITE
CIC

The Centre de Congrès Bordeaux, at Cité Mondiale, was the site of ESREF 2017.

The 28th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2017) was held on September 25-28, 2017, in Bordeaux, France. This charming town is on the UNESCO World Heritage List, classified as a "City of Art and History." It is also the European capital for optical and laser engineering and home to the Laser Mégajoule, one of the most powerful lasers in the world. Some of the largest companies in the aeronautics and aerospace industry are located around Bordeaux.

This international symposium continued its focus on recent developments and future directions in quality and reliability management of materials, devices, and circuits for micro-, nano-, and optoelectronics. The meeting provided a European forum for developing all aspects of reliability management and innovative analysis techniques for present and future electronic applications. For the 28th edition of this conference, major players in aeronautics, space, and the embedded systems industry were invited to provide specific topics such as radiation hardening, very long-term reliability, high/low temperature challenges, obsolescence, and counterfeit issues, wide band gap power devices for modern aircraft, and other embedded system applications.

The Technical Program Committee (TPC) led by Hélène Frémont (IMS, University of Bordeaux) and Marise Bafleur (LAAS, University of Toulouse) gathered about 200 volunteers who selected 130 scientific papers to be presented during oral and poster sessions. Authors of accepted papers addressed their reviewer's comments in the manuscript submitted for the ESREF 2017 special issue of *Microelectronics Reliability.* In addition, the Elsevier Editorial System implemented a strict review by two anonymous reviewers.

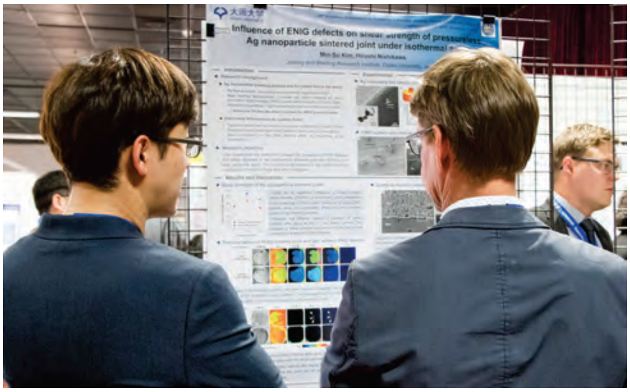
Accepted papers from around the world covered the following topics:

- Topic A – Quality and Reliability Assessment Techniques and Methods for Devices and Systems
- Topic B – Semiconductor Failure Mechanisms & Reliability: Defect Analysis from Devices to Product, Circuit Reliability Analysis
- Topic C – Progress in Failure Analysis: Defect Detection and Analysis
- Topic D – Reliability of SiC Devices, Millimeter Wave Power Devices and High-Power GaN Devices
- Topic E – Interconnections and New Failure Mechanisms
- Topic F – Power Devices Reliability and Failure Analysis: Interconnections, Model and Simulations, Power Devices, and Modules
- Topic G – Photonic Devices Reliability
- Topic H – MEMS Reliability
- Topic I – Extreme Environments: Ionizing Radiation, EMC, ESD, Electric Fast Transient

To draw new attendees and offer a compelling conference, organizers expanded the topical structure of the conference. Each topic was represented by invited papers, workshops, an oral session, and a poster session. The conference layout enabled each attendee to build his or her optimal schedule by topic or by specific interest without overlaps.

On the first day of the symposium, two tutorials enabled attendees to refresh and expand their knowledge on the following topics:

- "Simulation of Packaging under Harsh Environment Conditions: Temperature, Pressure, Corrosion and Radiation" by Kirsten Weide-Zaage (RESRI Group, Institute of Microelectronic Systems, University of Hannover, Germany)
- "The Impacts of EMC/ESD on Embedded Systems: A Challenge for Safe Systems Achievement" by Geneviève Duchamp (IMS Lab, University of Bordeaux, Fabrice Caignet, LAAS-CNRS Toulouse)



Poster session draws heavy traffic.

Plenary session at ESREF 2017 featuring invited speakers.

Seven invited speakers, who are recognized experts in their field, gave an overview of the state of the art and special focus on advanced research work. The keynote speech by Vincent Huard et al. (STMicroelectronics, France) opened the conference on September 25.

Invited talks focused on leading work in the areas of:

- "Enabling Robust Automotive Electronic Components in Advanced CMOS Nodes" by Vincent Huard[a,b], S. Mhira[a,b], F. Cachoa[a], A. Bravaix[b] ([a] STMicroelectronics, France; [b]REER, IM2NP-ISEN, CNRS, France)
- "Review of the Impact of Microstructure of Lead-Free Solder Joints on Assessment of Fatigue Lives of the Solder Joints by Simulations and Thermal Cycling Tests" by Per-Erik Tegehall (Swerea IVF, Sweden)
- "Aerospace Trends are Moving Fast Towards No More Custom ICs to High Reliability Automotive Solutions" by R. Enrici Vaion[a], M. Medda[a], A. Pintus[a], A. Mancaleoni[a], and G. Mura[b] ([a]STMicroelectronics, Agrate Brianza; [b]University of Cagliari, Italy)
- "Reconsideration of TDDB Reliability of Gate Dielectrics: Mechanisms and Statistics" by Kenji Okada, (TowerJazz Panasonic Semiconductor, Japan)
- "Technologies of IoT: Challenges and Chances for Fault Isolation" by Christian Boit, (Technical University of Berlin, Germany)
- "Reliability and Qualification of Microphotonics for Space Applications: A New Challenge" by Iain McKenzie (ESTEC-European Space Agency, Noordwijck, the Netherlands)
- "A Review of Vth Instabilities in GaN MISHEMTs" by Clemens Ostermaier (Infineon Villach, Germany)

Based on an exchange agreement with the committees of the International Symposium on the Physical & Failure Analysis of Integrated Circuits Conference (IPFA 2017) and the International Reliability Physics Symposium (IRPS 2017), the authors of outstanding papers were invited to present their work. The opening session concluded with the Best Papers from those sister conferences:

- IPFA 2017 Best Paper: "A Simple Method to Identify Metastable States in Random Telegraph Noise," Zhenghan Lin, Shaofeng Guo, Runsheng Wang, Dongyuan Mao, Ru Huang, (Peking University, China)
- IRPS 2017 Best Paper: "Robust Automotive Products in Advanced CMOS Nodes," Vincent Huard, Souhir Mhira, M. De Tomasi, E. Trabace, R.E. Vaion, and P. Zabberoni, (STMicroelectronics, France and Italy)

Workshop chairs provided attendees with multiple opportunities to hear about the vision and roadmap of several key industries handling high TRL products, challenged by research laboratories and academics proposing low TRL innovative technologies.

- The ESREF-ECPE annual workshop on Power Devices was organized by Eckard Wolfgang (ECPE-Germany) and Mauro Ciappa (ETH Zurich, Switzerland). This year's workshop focused on "Advanced Packaging and Reliability for Power Devices used in Automotive, Avionics, Traction, and Renewables."
- The workshop on "Emerging Challenges for a Built-In Reliability in Innovative Automotive ICs" was organized by Alberto Mancaleoni (STMicroelectronics, Agrate Brianza, Italy) and Massimo Vanzi (University of Cagliari, Italy).
- The workshop on "Photonic Devices and Systems: Up-to-Date Technologies, Challenges, Environment Risks and Reliability" was organized by Laurent Béchou (IMS Lab, University of Bordeaux, France) and Alain Bensoussan (IRT Saint Exupéry and Thales Alenia Space). It was co-organized with the French Photonics clusters, Route des Lasers, the Cluster for Aeronautics, Space and Embedded Systems, Aerospace Valley and the International Society on Reliability of Optoelectronic Systems.
- The workshop on "Wide Band Gap Components and Systems: Needs, Challenges, Environment Risks and Reliability" was organized by André Durier, (IRT Saint Exupéry and Continental, France); Matteo Meneghini, (University of Padova, Italy) and Loïc Théolier, (IMS, University of Bordeaux, France).
- The European Focused Ion Beam (FIB) Users Group meeting (EFUG workshop) was organized this year by Guillaume Audoit from CEA-France.

The exhibition featured 24 companies and opened on Monday afternoon with a cocktail reception. The exhibition area hosted coffee breaks and lunches, providing the opportunity for attendees to network with key vendors representing the fields of reliability and failure physics, and analysis of electron devices and systems. Exhibitor flash presentations were scheduled on Tuesday morning and afternoon to allow exhibitors to showcase their capabilities and know-how.

Exhibitors share their capabilities with attendees visiting the show floor.

A cocktail get-together during Tuesday's poster session and a gala dinner on Wednesday at the CAPC contemporary art museum provided additional networking opportunities.

Toasting during the gala dinner held inside the unique CAPC contemporary art museum.

With up to three parallel tracks, the conference was packed with rich content. Thanks to the large effort and efficient evaluation of scientific presentations by the Best Paper Award Committee chaired by Francesco Iannuzzo (University of Aalborg, Denmark), the following three

Bordeaux's Pont de pierre provides a picturesque backdrop for ESREF attendees. Courtesy of wikipedia.org/ Olivier Aumage.

papers were designated as outstanding. The authors received financial support to travel and an invitation to one of the sister conferences: IRPS 2018, IPFA 2018, or ISTFA 2018.

- "Protective Nanometer Films for Reliable Cu-Cu Connections," T. Berthold[a,b], G. Benstetter[a], W. Frammelsberger[a], M. Bogner[a], R. Rodríguez[b], and M. Nafría[b], ([a]Deggendorf Institute of Technology, Germany; [b]Autonomous University of Barcelona, Spain)
- "Capacitive Effects in IGBTs Limiting Their Reliability under Short Circuit," P.D. Reigosa, F. Iannuzzo, M. Rahimo, and F. Blaabjerg, (Aalborg University, Denmark and ABB Switzerland Ltd. Semiconductors)
- "Temperature Accelerated Discharging Processes through the Bulk of PECVD Silicon Nitride Films for MEMS Capacitive Switches," M. Koutsoureli, N. Siannas, and G. Papaioannou, (University of Athens, Greece)

A very warm thank you goes to all the volunteers, the IMS lab team, the local support of the University of Bordeaux and the IDEX program, the ADERA Congrès team, and the speakers, attendees, and industrial exhibitors who created this memorable event.

Do not miss the 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2018, on October 1-5, in Aalborg, Denmark. Mark your calendar for this event, and visit the ESREF website at esref.org for updated information. ■

NOTEWORTHY NEWS

MICROSCOPY & MICROANALYSIS 2018 MEETING

The Microscopy & Microanalysis (M&M) 2018 meeting will be held **August 5-9** in Baltimore. The scientific program features the latest advances in biological, physical, and analytical sciences as well as techniques and instrumentation. Complementing the program is one of the largest exhibitions of microscopy and microanalysis instrumentation and resources in the world. Educational opportunities include a variety of Sunday short courses, tutorials, workshops, and pre-meeting congresses for early-career scientists. The opening reception offers a networking venue for meeting new people in the field and renewing old acquaintances, while the Monday morning plenary session showcases talks from outstanding researchers and recognizes major Society and meeting award winners. In addition, daily poster awards will highlight the best student posters in instrumentation and techniques as well as biological and physical applications of microscopy and microanalysis.

M&M is sponsored by the Microscopy Society of America, the Microanalysis Society, and the Microscopical Society of Canada. For more information, visit microscopy.org/MandM/2018. ■

EDFAS 2018 PHOTO CONTEST

OPEN TO ALL MEMBERS OF THE FAILURE ANALYSIS COMMUNITY!

SHARE YOUR BEST IMAGES WITH THE FAILURE ANALYSIS COMMUNITY AND BE RECOGNIZED FOR CREATING THEM!

SPONSORED BY THE MEMBERSHIP COMMITTEE OF THE ELECTRONIC DEVICE FAILURE ANALYSIS SOCIETY

Where: Selected entries will be displayed and prizes awarded October 28 - November 1 at the 44th International Symposium for Testing and Failure Analysis (ISTFA) Conference and Exposition in Phoenix.

Categories: No more than one image per person allowed in each category

I. *Color Images Only* (*Optical Microscopy*)

II. *Black & White Images Only* (*Optical Microscopy/SEM/TEM/X-Ray/UV Micrographs/Other*)

III. *False Color Images Only* (*SPM/SAM/Photon Emission/Other*)

Images will be judged on failure analysis relevance (35%), aesthetics (35%), and novelty of the technique or mechanism (30%).

Deadline: Entries must be submitted by September 1.

Entries: Submit by email to **photocontest@edfas.org** (subject line: EDFAS Photo Contest).

Format: Submissions should be made through email only, with one picture attached. Each submission must be in a standard format (PNG, JPEG, TIFF, BMP, etc.). Please provide your highest-resolution image. The preferred submission is a .jpg or .tif, five inches wide at 300 dpi resolution.

Along with the picture, the email should include the name of the submitter, category of submission, mailing address, phone, fax, email address, and a description of the micrograph (not exceeding 50 words). The picture should not have any contact information embedded.

Copyright & Permissions: Entrants are responsible for obtaining any releases or any other permission or license necessary for the submission of their work for this contest and future publication. EDFAS and ASM International will have the right to exhibit, reproduce, and distribute in any manner any or all of the entries. The entries will not be returned to the submitters.

Prizes: **1st place** in each category receives a wall plaque and one-year complimentary ASM/EDFAS membership.

2nd and 3rd places in each category receive award certificates and one-year complimentary ASM/EDFAS memberships.

The top 10 entries in each category will be displayed at ISTFA 2018 in Phoenix.

edfas.org

EDFAS 2018 VIDEO CONTEST

ARE YOU THE NEXT SCORSESE OF FAILURE ANALYSIS? WE HOPE SO!

Submit your 3 minute (or less) video about an exciting result or a scintillating artifact—anything goes as long as it relates to failure analysis! Your FA community will judge them and recognize winners at this year's ISTFA. Show off your filmmaking skills and FA prowess. **Upload your video today!**

Format:	MPEG or AVI format with a maximum size of 50 MB. The video should be 3 minutes or less. Audio and subtitles are allowed. A short description should also be submitted along with all of your complete contact information.
Categories:	**Failure Analysts:** Anyone working in the failure analysis field **Students:** Students currently studying in fields related to failure analysis (physics/electrical engineering/chemistry/materials science, etc.) **Exhibitors**
Deadline:	October 1
Entries:	Go to https://asm.confex.com/asm/istfa18/cfp.cgi
Copyright & Permissions:	Entrants are responsible for obtaining any releases or any other permission or license necessary for the submission of their work for this contest and future publication. EDFAS and ASM International will have the right to exhibit, reproduce, and distribute any or all of the entries. The entries will not be returned to the submitters. You will be asked to accept the copyright and permissions before you upload your video.
Prizes:	**1st place** receives a $50 gift card, a complimentary registration to a future ISTFA conference, and a 1st place winner plaque. **2nd place** receives a $25 gift card and award certificate. **3rd place** receives an award certificate. (Note: 2nd place will be awarded if total submissions are more than 10; 3rd place will be awarded if total submissions are more than 15.) The top 10 entries in each category will be displayed at ISTFA 2018 in Phoenix.

WIN ESTEEM AND RESPECT FOR YOURSELF AND YOUR COMPANY BY SUBMITTING THE WINNING VIDEO. LIGHTS, CAMERA...ANALYSIS!

edfas.org

SEMICAPS

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- Laser Timing Probe (LTP)
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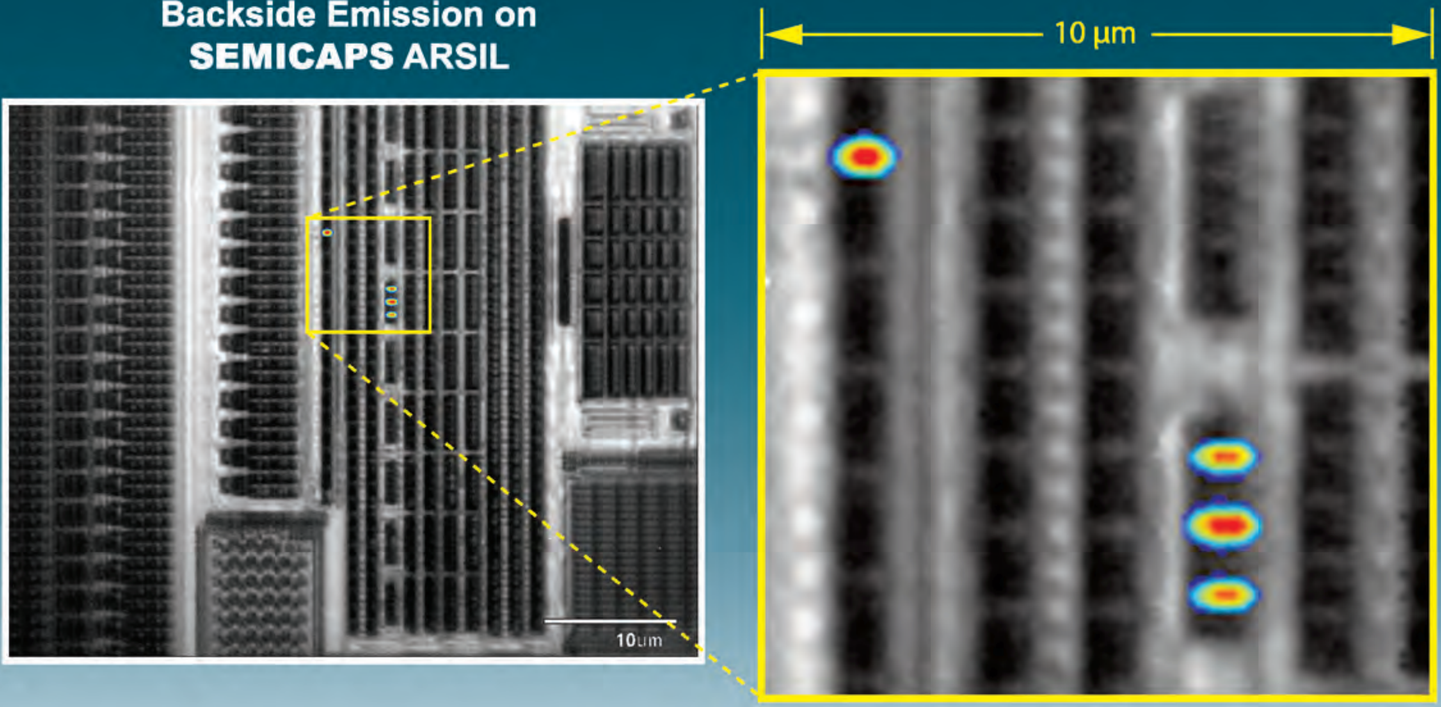
Backside Emission on SEMICAPS ARSIL



SEMICAPS

Excellence In Innovation

DIRECTORY OF INDEPENDENT FA PROVIDERS

Rosalinda M. Ring, Kionix
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Electronic companies of all types and sizes require failure analysis (FA) services. Our goal is to supply a resource of FA service providers for your reference files. The directory lists independent providers and their contact information, expertise, and types of technical services offered.

ACCOLADE ENGINEERING SOLUTIONS

15520 Rockfield Blvd., Suite H
Irvine, CA 92618
949.597.TEST or 949.597.8378
info@accoladeeng.com
accoladeeng.com
Services: Reliability assessment, failure analysis, and analytical, chemical, and material characterization, etc.
Tools/Techniques: DSC, DMA, TMA, TGA, TGA-MS, micro-sectional analysis, electron microscopy (FE-SEM) with EDS, CSAM, microhardness testing, electromechanical universal tester, bondtester, XRF, GC-MS, Py-GCMS, microhardness testing, E, ion chromatography, FTIR, ICP-MS, LA-ICP-MS, temperature/humidity testing, thermal shock, impact shock, drop shock, HALT, HASS, flying probe in-circuit testing, etc.

FIB SERVICES

1400 S Sherman St., Suite 212
Richardson, TX 75081
972.470.9290 or
972.470.1688
fibservices.com
Services: FIB frontside and backside circuit edit, TEM cross-sections, etc.
Tools/Techniques: FEI V600 FIB, decapsulation, glob after edit, prototype packaging, etc.

FIB-X

538 Haggard St., Suite 409A
Plano, TX 75074
214.473.6764
fib@fibx.com
fibx.com
Services: Oil & gas, shale SEM maps imaging, IC design verification, debug, cross-sections, decapsulation/encapsulation
Tools/Techniques: FEI Teneo SEM, FEI DB235 dual beam FIB/SEM, DCG P3X circuit mod tool, Fischione model 1060 SEM mill for geological samples, etc.

IC FAILURE ANALYSIS LAB

1719 S. Grand Ave.
Santa Ana, CA 92705-4808
949.329.0340
info@icfailureanalysis.com
icfailureanalysis.com
Services: IC/package/PCB cost and failure analysis, IC/package/PCB reverse engineering, microsurgery, reliability testing services, counterfeit component authenticity, etc.
Tools/Techniques: Chemical/laser decapsulation, cross-sectioning, delayering/parallel lapping, dye and pry analysis, EDX, PEM (EMMI), OBIRCH, FIB precision cutting, I-V (curve trace) measurement, optical microscope, optical profiler, SAM or SAT, scanning capacitance microscopy, SEM, SIMS, TEM, x-ray (2D and 3D) examination, autoclave or pressure cooker test, bias life test, die shear test, ESD (CDM, HBM, MM), HAST, HTSL, HTOL/THB, latch-up test, lead integrity test, mark permanency test, moisture/reflow sensitivity classification, physical dimension measurement, reconditioning Test (PC), real-time thermal profiling, solderability, solder ball shear test (BGA), temperature cycling air-to-air, temperature humidity bias testing, thermal shock, wire bond pull test, wire bond shear test, etc.

MATERIALS RESEARCH LABORATORIES INC.

290 North Bridge St.
Struthers, OH 44471
800.424.1776 or
330.750.0778
info@mrllab.com
mrllab.com
Services: Physical and chemical analysis of solid materials and surfaces; failure analysis
Tools/Techniques: XPS/ESCA, ISS, high-resolution SAM, SEM, TEM, SAED, EDS, infrared spectroscopy/microscopy (FTIR/microFTIR), laser Raman spectroscopy/microscopy, UV/VIS/NIR spectroscopy, RGA, metallography, light microscopy, gas/liquid/ion chromatography, physical testing (tensile, shear, etc.) XRD, WDS, STEM, AFM, STM, emission spectroscopy (DCP/ICP), XRF, atomic absorption and mass spectroscopy, thermal analysis (DSC/DTA/TGA), NMR, SIMS/LIMS, ToF-SIMS, etc.

NANOPHYSICS B.V.

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+3153 711 3618 or +31(0)53 489 1087
info@nanophysics.nl
nanophysics.nl
Services: Failure analysis, quality control, and materials characterization
Tools/Techniques: CSAM, x-ray inspection (2D and 3D), dual beam FIB cross-sectioning, conventional cross-sectioning, optical and electron microscopy, SEM/EDX, decapsulation of integrated circuits, FIB chip modification/probe pad deposition, OBIRCH fault localization, photon emission fault localization, advanced TEM sample preparation and imaging, STEM-HAADF, etc.

NANOSCOPE SERVICES

No. 30, Station Road Workshops
Station Road, Kingswood
Bristol, BS15 4PJ, UK
+44 (0)117 957 6225
contact@nanoscopeservices.com
nanoscopeservices.com
Services: IC nanosurgery, failure analysis, reliability testing, fabrication process qualifications, and nanofabrication for the nanotech community
Tools/Techniques: SEM-EDS analysis, FIB x-sections (site specific), FIB sections for FA, QA, and metrology, (S)TEM foil prep, customized TEM foils, (S)TEM analysis, deep (S)TEM foils, cryo-DualBeam, nanoprototyping, x-ray imaging, CSAM, etc. ■

INTERNET RESOURCES FOR ENGINEERING

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NATIONAL RENEWABLE ENERGY LABORATORY (NREL)

WWW **nrel.gov**

The NREL is located in Colorado. It advances the science and engineering of energy efficiency, sustainable transportation, and renewable power technologies and provides the knowledge to integrate and optimize energy systems. The NREL is the only federal laboratory dedicated to the research, development, commercialization, and deployment of renewable energy and energy efficiency technologies.

OAK RIDGE NATIONAL LABORATORY (ORNL)

WWW **ornl.gov**

ORNL is recognized as the largest U.S. Department of Energy science and energy laboratory. Its missions consist of scientific discovery, clean energy, and security. ORNL has added new research missions in the areas of national security and high-performance computing to its historic competencies in energy, life sciences, neutron sciences, and advanced materials.

USA.GOV

WWW **usa.gov**

USA.gov is an online guide to government information and services. It searches federal, state, and local government websites (most ending in .gov or .mil) to provide official information.

HOW-TO GEEK

WWW **howtogeek.com/120865**

How-To Geek provides websites for expanding scientific knowledge. From news about scientific discoveries to resources for teaching science, a wealth of scientific information can be found on the web.

SCIENCE.GOV

WWW **science.gov**

Fourteen scientific and technical information organizations from ten major science agencies have collaborated to create science.gov, the "FirstGov for Science" website. This site is the gateway to reliable information about science and technology from across federal government organizations. Users can find over 1000 government information resources about science, including technical reports, journal citations, databases, federal websites, and fact sheets.

AIR FORCE RESEARCH LABORATORY SCHOLARS PROGRAM

WWW **afrlscholars.usra.edu**

This program is dedicated to preparing students for leadership positions in the science, technology, engineering, and mathematics fields through the integration of education and experience in research and development. ■

PRODUCT NEWS

PRESS RELEASE SUBMISSIONS:
MAGAZINES@ASMINTERNATIONAL.ORG

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PHENOM-WORLD LAUNCHES NEW DESKTOP SEMS

Phenom-World, the Netherlands, a leading supplier of desktop scanning electron microscopes (SEMs), introduces its fifth-generation Phenom Pro and ProX SEMs. The systems' enhanced imaging performance, 20% resolution improvement, larger choice of detectors, and new software significantly widen their application range while still maintaining ease of use. Their excellent performance offers a serious alternative to floor-model SEMs in applications that include materials science, industrial manufacturing, electronics, earth science, life sciences, education, and more.

"Desktop SEMs have matured and are providing valuable and reliable results," explains Emile Asselbergs, chief executive officer. "Increasingly, SEM users are realizing that they do not need a full-sized floor-model SEM for many SEM jobs. In fact, most of our currently installed desktop SEM systems are being used in applications that previously used floor-model systems. Our Generation 5 SEMs will only accelerate this trend."

"Generation 5 is a big step forward and adds a number of advanced features," says Jos Maas, director of product marketing. "Imaging is improved, thanks to new electronics and an improved lens. Resolution is at least 20% better. In addition, an optional, high-end secondary electron detector is now available, extending their application to situations that require more sensitivity to surface information. The Generation 5 SEMs also allow the user to image materials that are very sensitive to beam damage. Glove box compatibility allows imaging of highly reactive materials that need to be manipulated in an inert gas environment, such as argon or nitrogen."

Phenom
ProX

The Phenom ProX SEM from Phenom-World.

The Phenom Pro and ProX Generation 5 SEMs are robust, vibration-insensitive SEMs that allow easy sample handling and deliver an image in approximately 30 s. A long-lifetime, high-brightness CeB_6 source provides excellent image quality, even in low-vacuum conditions when analyzing nonconductive samples. A powerful and transparent application programming interface makes it easy for users to optimize imaging and image processing for their own dedicated workflows. Additionally, on the Phenom ProX, a fully integrated energy-dispersive x-ray spectroscopy detector allows users to analyze elemental composition and distribution at the microscopic scale.

For more information, visit phenom-world.com.

KEYSIGHT LAUNCHES AUTOMOTIVE ETHERNET SOLUTIONS

Keysight Technologies Inc., Santa Rosa, Calif., recently unveiled five new automotive Ethernet solutions to help automotive design and test engineers bring their products to market faster with easy-to-use conformance testing.

Among the innovations is the suite of BroadR-Reach, 100Base-T1, and 1000Base-T1 compatible automotive Ethernet bundles, providing automated setup and testing for Tx, link segment, as well as Rx connectivity and protocol decoding.

Automotive Ethernet is increasingly more important as a backbone to a car's communication network. Safety standards and increased consumer communication demands require the automotive industry to add more applications with ever increasing complexity for connectivity to networks. Faster data-transfer times and more reliable networks demand that the backplane is lighter, faster, and more robust than before. Car manufacturers, original equipment manufacturers, and chipset vendors in the automotive industry are looking to automotive Ethernet as a replacement for the aging media-oriented systems transport bus.

Keysight's solutions simplify the test setup and interpretation of results to validate BroadR-Reach, 100Base-T1,

Keysight's automotive Ethernet receiver compliance test solution.

and 1000Base-T1 specifications for physical media attachment, physical layer solutions, and physical coding sublayer. All four software options automate compliance with 100% test coverage for all tests in the automotive physical layer BroadR-Reach, 100Base-T1, and 1000Base-T1 specifications, respectively.

These automotive Ethernet test software packages automatically execute tests and display results in a flexible report format. In addition to measurement data, the report provides a margin analysis that shows how closely the devices passed or failed each test. The automotive Ethernet electrical compliance solutions perform a complete set of electrical tests to meet the BroadR-Reach, 100Base-T1, and/or 1000Base-T1 specifications:

- Transceiver testing for BroadR-Reach V3.2 and 100Base-T1 (IEEE 802.3bw) specifications
- Receiver testing for BroadR-Reach V3.2 and 100Base-T1 (IEEE 802.3bw) specifications
- Transceiver testing for 1000Base-T1 (IEEE 802.3bp) specifications
- Protocol trigger and decode for BroadR-Reach V3.2 and 100Base-T1 (IEEE 802.3bw) specifications
- Link testing for BroadR-Reach V3.2 and 100Base-T1 (IEEE 802.3bw) specifications

For more information, visit keysight.com.

INOVENSO INTRODUCES IEM DESKTOP SEM

Inovenso, Istanbul, introduces its IEM Series of desktop scanning electron microscopes. The biggest advantages of Inovenso's benchtop SEMs over conventional SEMs is process rapidity. With Inovenso's SEMs, results can be obtained within four minutes, compared with 30 minutes for conventional SEMs. The price difference is also considerable, as the benchtop SEMs enable users to achieve 5 nm resolution results (similar to a full-sized SEM) with a price that is three times more affordable. Another advantage is that the benchtop SEM doesn't require any infrastructure—just a table and a plug.

The SEMoscope tabletop SEM combines imaging power up to 150,000× magnification rate and outstanding technical performance with better depth of focus and chemical contrast:

Integrated EDS analysis. The SEMoscope + Series high level tabletop SEMs offer integrated, powerful EDS microanalysis with NORAN System 7 specialized for SEMoscope spectral imaging. Further, the UltraDry Compact EDS detector provides outstanding elemental mapping within a few minutes. With spectral imaging, where a full EDS spectrum is stored at every pixel, samples can be analyzed after they have been removed from the microscope. NORAN System 7 tools provide several analytical methods for best results. Both Oxford and EDAX brands of EDS detectors can be integrated into the SEMoscope dekstop SEM models depending on user needs.

Removable BSE detector. By applying the 4-channel BSE detector, composition and topography functions are available. These functions are optional and can be opted out.

ION coater and cool stage. During SEM analysis, the specimen is irradiated with an electron beam, which causes an accumulation of electric charges on the specimen surface and decreasing image quality. In order to obtain high quality images of nonconductive samples via SEM, it is necessary to create a conductive layer on the surface. The conductive coating shields the sample from the surface charge and provides a ground-potential surface, eliminating electric fields outside the sample.

For more information, visit semoscope.com.

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Inovenso's benchtop SEM.

BRUKER DEBUTS NANOMECHANICS LAB

Bruker Corp., Billerica, Mass., announces the NanoMechanics Lab, a suite of force-mapping modes that enable Dimension FastScan and Icon AFM systems to perform quantitative nanoscale characterization, extending from soft hydrogels and polymers to stiff metals and ceramics. The NanoMechanics Lab encompasses a broad range of nanoscale AFM measurement techniques, including the well-established force volume mode, as well as the new high-accuracy PeakForce QNM, FASTForce volume, and FASTForce volume contact resonance modes. Using advanced algorithms and AFM probe manufacturing methods, these modes deliver repeatable and accurate high-volume quantitative measurements, with the addition of data cubes for multidimensional nanoscale analysis of materials.

For more information, visit bruker.com.

HORIBA SCIENTIFIC INTRODUCES UVISEL PLUS

Horiba Scientific, Japan, a global leader in spectroscopic ellipsometry for over 25 years, announces the launch of Uvisel Plus, a modular ellipsometer that includes acquisition technology designed to measure thin-film samples faster and more accurately than ever.

FastAcq, the company's newest acquisition technology, is based on double modulation designed for real-world thin-film characterization. Based on a new electronic data-processing and high-speed monochromator, the FastAcq technology enables a sample measurement from 190 to 2100 nm to be completed within three minutes at high resolution. The ability to continuously adjust the spectral resolution along the measurement range enables smarter and faster sample scanning. The Uvisel Plus also introduces a new calibration procedure, delivering faster performance and accuracy.

HORIBA
UVISEL

Horiba's Uvisel Plus.

Due to its design, which has no rotating elements and no additional components in the optical path, the Uvisel series phase-modulation technology delivers pure and efficient polarization modulation for accurate ellipsometric parameter measurements. The superior polarization modulation capabilities of the photoelastic modulator deliver the highest sensitivity for measurement of critical thin, transparent layers deposited onto glass substrates.

Designed for enhanced flexibility for thin-film measurements, the Uvisel Plus offers microspots for patterned samples down to 50 µm, variable angles from 40° to 90°, an automatic horizontal mapping stage, and a variety of accessories, making it scalable to meet numerous application and budget needs. The spectral range from 190 to 2100 nm is covered by two Uvisel Plus configurations: 190 to 920 nm and a near-infrared extension to 2100 nm. The easy upgradability is a hallmark of the Uvisel Plus to meet ongoing demanding applications. Driven by an advanced DeltaPsi2 software platform, as well as the Auto-Soft interface featuring an intuitive workflow to speed up data collection and analysis, the Uvisel Plus allows users from novice to expert to perform thin-film measurements with extremely high accuracy and sensitivity.

For more information, visit horiba.com/uviselplus.

NEW MICROSCOPY TECHNIQUE REPORTED FOR NANOMECHANICAL SUBSURFACE IMAGING

Northwestern University, Evanston, Ill., reports the development of scanning near-field thickness resonance acoustic microscopy (SNTRAM), an imaging technology with sharp phase contrast and mechanical sensitivity that suits a wide range of applications in nanomechanical imaging of semiconductor structures and other materials.

Acoustic waves can be used to measure several properties, such as thickness, sound speed, acoustic impedance, density, bulk modulus, and attenuation for numerous materials, both soft and hard. Because these are elastic strain waves that can travel through different materials without causing any damage, they can be used for imaging subsurface structures noninvasively, a concept widely used in medical imaging. Nanoscale spatial resolution can be achieved by combining atomic force microscopy (AFM) and ultrasonic microscopy, using an AFM probe as a local mechanical detector of elastic waves. However, the combination of ultrasonics with an AFM platform is still a developing area of research, where understanding the physics of the mechanism of detection and determining the sensitivity of detection of surface or subsurface properties are still in progress.

Despite progress in ultrasonic-based methods, major challenges persist. For example, one question is how to generate better image contrast in spite of high signal-to-noise of the transmitted ultrasound wave to the other side of the sample. Another challenge involves achieving sensitive detection of local variation in material properties at much better resolution when facing a sharp change in phase (especially when two materials have similar mechanical properties).

In the newly developed SNTRAM technique, the sample is actuated at a frequency corresponding to the lowest longitudinal thickness resonance mode(s) in the actuating transducer, and the AFM cantilever is operated in contact mode. The sample resonates at its natural resonance frequency via the piezotransducer underneath it.

The authors demonstrated the versatility of this technique by imaging buried conical holes created by focused ion beam (FIB) and low-k dielectrics patterned trenches. They believe this development will fill a critical void in the subnanometer spatial range for nondestructive subsurface imaging in physical sciences.

For more information, see the article “Thickness Resonance Acoustic Microscopy for Nanomechanical Subsurface Imaging” by G.S. Shekhawat et al. in *ACS Nano*, 2017, *11*(6), pp. 6139–45, DOI: 10.1021/acsnano.7b02170.

ZEISS ENTERS SEMICONDUCTOR PROCESS CONTROL MARKET

Zeiss, Germany, is expanding into a new market in the semiconductor industry. Through its new Process Control Solutions (PCS) business unit, the company will leverage its core technology solutions and partnerships to address a range of special needs for semiconductor customers. This business unit will be part of the Zeiss Semiconductor Manufacturing Technology (SMT) business group.

“We see a strong trend in semiconductors toward complex 3D chip structures and new materials,” explains Karl Lamprecht, head of the SMT business group. “As development cycles lengthen and R&D costs climb, the role of metrology changes. Our customers need effective process control solutions delivering integrated, actionable information that speeds time to problem resolution and time to production.”

With shrinking structure sizes, ever more sophisticated designs, and hundreds of individual working steps, the semiconductor manufacturing workflow has become increasingly challenging. Fast and cost-effective process control solutions play a key role in ensuring the functioning of semiconductor devices. Zeiss is now bringing its semiconductor equipment experience into the market for semiconductor process control solutions.

The PCS business unit will expand on Zeiss’s existing product portfolio including its core proprietary microscopy technologies to penetrate the semiconductor lab and fab space. Key products to be deployed include Zeiss’s electron microscopes Zeiss Crossbeam and Zeiss MultiSEM (the latter incorporates the company’s unique multi-electron-beam technology), the ion beam microscope Zeiss Orion NanoFab, as well as the Zeiss Xradia Versa and Zeiss Xradia Ultra nondestructive 3D x-ray microscope systems. Process control solutions will be offered across the spectrum of semiconductor manufacturing process steps, including front end of line, back end of line, packaging, and assembly.

To aid in this effort, the new Zeiss Customer Center Bay Area was opened in Pleasanton, Calif., on June 15, 2017. Located near the heart of Silicon Valley, this facility joins the company’s global network of customer centers in making the company’s portfolio of optical, ion, electron, and x-ray microscopy offerings available for demonstrations, application development, and training.

For more information, visit zeiss.com/semiconductor-process-control.

AEROTECH’S HEXAPOD ADVANCES POSITIONING PERFORMANCE

HexGen hexapods from Aerotech, Pittsburgh, represent a significant advance in six-degree-of-freedom positioning performance. The newest member of the HexGen family, the HEX300-230HL, is targeted at medium-load, ultraprecision applications ranging from sensor testing to synchrotron sample manipulation. HexGen hexapods are reportedly the only hexapods on the market that provide guaranteed positioning accuracy specifications below 5 μm.

The HEX300-230HL is actuated with six high-accuracy struts built with precision preloaded bearings, ball screws, and drive components. Unlike competitive hexapods driven by DC brush servomotors, the HEX300-230HL is

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TRAINING CALENDAR

Rose M. Ring, Kionix
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LIFELONG LEARNING

EDFAS believes in lifelong learning and supporting our members and customers in that endeavor. Our goal is to provide a list of educational resources in failure analysis and related topics in each issue of *EDFA* magazine. In addition, explore all EDFAS has to offer from regional events, chapter courses, and tutorials and courses during ISTFA. Find out more by visiting edfas.org.

May 2018

EVENT	DATE	LOCATION
Southeast Asia Technical Conference on Electronics Assembly Expo	5/8-10	Kuala Lumpur, Malaysia
Medical Electronics Symposium	5/16-17	Dallas, TX
Contact: SMTA		
Metallographic Techniques	5/7-10	Novelty, OH
Principles of Failure Analysis	5/21-24	Novelty, OH
Practical Fractography	5/23-24	Novelty, OH
Contact: ASM International		

June 2018

EVENT	DATE	LOCATION
International Conference for Electronics Enabling Technologies	6/5-7	Markham, Canada
Symposium on Counterfeit Parts and Materials	6/26-28	Hyattsville, MD
Contact: SMTA		
Atom Probe Tomography and Microscopy 2018	6/10-15	Gaithersburg, MD
Contact: NIST		
Introduction to SEM and EDS for the New Operator	6/3	Bethlehem, PA
Focused Ion Beam (FIB): Instrumentation and Applications	6/3-8	Bethlehem, PA
Scanning Electron Microscopy and X-ray Microanalysis	6/4-8	Bethlehem, PA
Problem Solving: Interpretation and Analysis of SEM/EDS/EBSD Data	6/4-8	Bethlehem, PA

June 2018 (cont'd)

EVENT	DATE	LOCATION
Quantitative X-ray Microanalysis: Problem Solving using EDS and WDS Techniques	6/4-8	Bethlehem, PA
Scanning Transmission Electron Microscopy: From Fundamentals to Advanced Applications	6/4-8	Bethlehem, PA
Contact: Lehigh Microscopy School		
Metallurgy for the Non-Metallurgist	6/4-7	Novelty, OH
Fractography	6/11-14	Novelty, OH
Elements of Metallurgy	6/11-14	Novelty, OH
Contact: ASM International		

July 2018

EVENT	DATE	LOCATION
Introduction to Metallurgical Lab Practices	7/9-12	Novelty, OH
Metallurgy for the Non-Metallurgist	7/10-12	Novelty, OH
Metallurgy for the Non-Metallurgist: Midlands Technical College	7/23-26	Columbia, SC
Advanced Metallographic Techniques	7/30-8/2	Novelty, OH
Contact: ASM International		

August 2018

EVENT	DATE	LOCATION
Microscopy & Microanalysis 2018	8/5-9	Baltimore, MD
Contact: M&M 2018		
Practical Interpretation of Microstructures	8/6-9	Novelty, OH
Contact: ASM International		

Contact Information

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M&M 2018
Microscopy Society of America
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microscopy.org/MandM/2018

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SMTA
952.920.7682
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PRODUCT NEWS

CONTINUED FROM PAGE 47

driven by Aerotech's AC brushless, slotless servomotors that maximize its performance and longevity. Directly coupling the AC brushless servomotors to the ball screw results in increased drive stiffness, higher positioning accuracy, and better minimum incremental motion (20 nm in *XYZ* and 0.2 µrad for θxθyθz) compared to competitive designs using belts, gearheads, or compliant couplings. Specially engineered strut pivot joints provide low friction and high stiffness, enhancing the hexapod's overall performance. The HEX300-230HL's structural design offers the user a generous load capacity of up to 45 kg.

AEROTECH
HEXGEN

Aerotech's HexGen hexapod positioning system.

The HEX300-230HL's platform and base can be easily modified with user-specific features or mounting patterns. It features a 100-mm-diameter clear aperture in the platform, while a 60-mm-diameter clear aperture in the base allows workpiece access from the bottom. The base mounting holes adapt directly to English and metric optical tables.

Aerotech hexapods can be vacuum prepared for demanding applications such as synchrotron sample or optics manipulation, semiconductor manufacturing and inspection, or satellite sensor testing.

Driving the HEX300-230HL is Aerotech's award-winning A3200 motion control software. Built on years of experience with difficult kinematics applications, the A3200 controller allows easy programming and control of the hexapod in any user-defined coordinate system.

Aerotech's HexSim software gives users the ability to easily visualize and simulate the available workspace. Tight integration between HexSim and the A3200 motion controller provides real-time motion visualization in any user-defined coordinate system. An intuitive graphical interface permits selection of the active coordinate system for easy virtual pivot-point programming and motion.

For more information, visit aerotech.com.

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LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Reverse Engineering, Counterfeit Electronics, Case Studies, System Level, and Packaging

Michael R. Bruce, Consultant
mike.bruce@earthlink.net

The current column covers peer-reviewed articles published since 2015 on reverse engineering, counterfeit electronics, case studies, system level, and packaging. All of these fields are dependent on failure analysis for their success. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the email address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

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GUEST COLUMNIST

EVOLUTION OR REVOLUTION? HOW MOBILE PHONES CHANGED THE CHIP BUSINESS

Dick James, TechSearch International
dickjames@ieee.org

I've been in the business of taking things apart for a living for the last 20-plus years, and aside from the technological changes brought on by Moore's Law, the products we pull apart in order to see the latest technology have changed through those years.

Back in the '90s we were mainly taking apart PCs and laptops to get the leading-edge chips. That morphed into gaming systems, such as the Xbox or Sony PlayStation. After the iPhone launch, it started to be mobile phones. However, Intel has always ploughed its own furrow. So to get their latest chip, it has always been—and still is—a PC to get the CPU. In parallel, we have seen the growth of the memory business, both DRAM and NAND flash.

Alongside all of this is the consolidation of the chip manufacturing industry. Now we are down to four players producing the latest generations of logic process technology: TSMC, Samsung, GlobalFoundries, and Intel. Similarly, we have four memory companies: Samsung, SK Hynix, Toshiba/Western Digital (or whatever the newly separated company will be called), and Micron/Intel.

Of course, in terms of chip technology, we have to get back to Moore's Law and rewind to the 90 nm node, circa 2004. Leading-edge phone manufacturers such as Nokia and Motorola were using 90 nm chips in common with the PC and gaming companies.

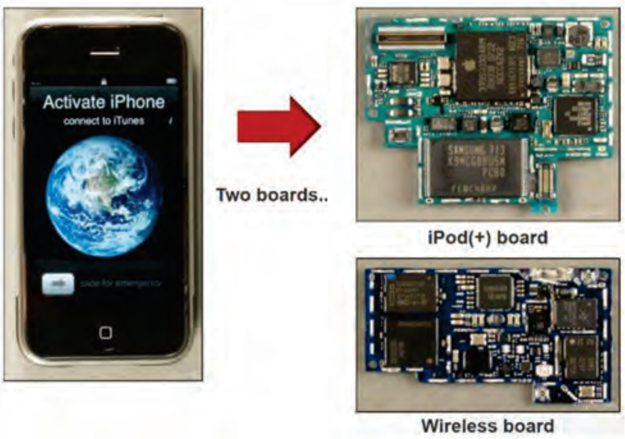
Then came the iPhone. It contained no individual leading-edge chips and didn't have outstanding performance as a phone. Rather, it was the integration of the innovative touchscreen, multiple applications, and sleek design that gave it a market edge.

In chip packaging terms, the iPhone followed the trend of other mobile phones and was fairly replete with condensed packaging for the time: two multi-chip packages, a dual-stacked Samsung NAND flash, and the Samsung app's processor + SDRAM package on package (PoP). There were also Marvell and CSR chips that were both flip-chip on board. I think this was the first use of a PoP in a phone, though the app's processor itself was 65 nm technology, like the competition.

Around that same time, Intel and Panasonic were just about to launch their 45-nm technologies, and everyone else was plugging away at 65 nm processes. The foundries tended to use field-programmable gate arrays from Altera or Xilinx to prove in their new processes, so for a generation or two we would hunt those down to get the first iteration.

That changed at the 40/45 nm generations, with the Apple A4 on Samsung's 45 nm process, and Qualcomm having a lot of trouble getting yield out of TSMC 40 nm. Then phones started to be the driver: the A5 was 32 nm, the A7 was 28 nm, both from Samsung, and the Snapdragon 800 was TSMC 28 nm. By this time, we're down to two main suppliers for app processors: TSMC and Samsung. Apple, Qualcomm, and Samsung pushed the chip designs for headline phones, while Huawei's HiSilicon tried to catch up.

Now examining the latest iterations, the iPhone 8 series and the X are almost unrecognizable when compared with the original. The application processors are made on the latest 10 nm process from TSMC, and they



The original iPhone from 2007. Source: TechInsights.

are now 4G LTE world phones capable of working with over 40 wireless bands, and equipped with carrier aggregation to improve signal sensitivity. The same can be said for the competitor phones from Samsung, Huawei, Xiaomi, et al.

In parallel with the logic evolution, we've had advances in flash memory, the demand for more and more data driving the maximum memory from 8 GB to 256 GB in 10 years, and DRAM from 128 MB to 6 GB in some products.

With the expanded wireless capability, the radio frequency (RF) end of the board is a lot more complex, and we can't ignore the sensors. Fingerprint sensors were introduced in the iPhone 5S. In addition to motion and direction sensors, there are now barometric, temperature, and humidity sensors, and heart rate monitors. Now we have face recognition too, with its complex set of optical sensing tools.

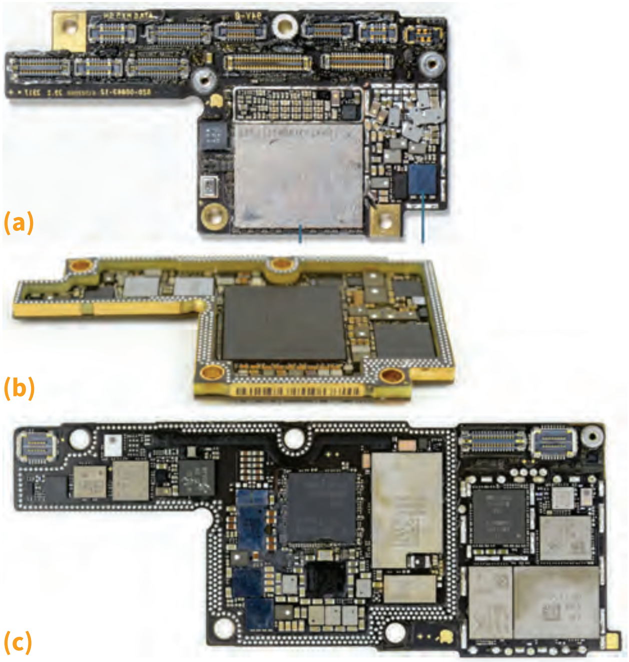
So while we all anticipate the latest phone from Apple or Samsung to see what the newest processor is at the latest process node, we have to recognize that all the added capabilities have propelled other segments of the industry. Image sensors are now a much bigger deal, and have likely dealt a death blow to the compact camera industry. RF-SOI is not the niche technology that it once was, BCD-MOS is thriving in the power-management area, and even GaAs is having its day.

The form factor has evolved too, from the flip-phone and candy-bar formats to the almost universal full-screen smartphone. There seems to be a competition to make the thinnest phone, as well as the highest performance device.

The original iPhone was 11.7 mm, and it bottomed out in the iPhone 6 at 6.9 mm. Now the iPhone X is up to 7.6 mm, with the camera bump increasing the thickness. (I'm using iPhones for comparison, simply because the data and teardowns are well tabulated, making research for this piece much easier.)

That, of course, has put pressure on the packaging segment of the business to innovate both dimensionally and cost-wise. Again looking at Apple, it is clear that wafer-level packaging (WLP) count has significantly increased—the iPhone 7 is up to 44, and the iPhone 8 and X models are in the 35-40 range. For a graphic, visit https://www.eetimes.com/document.asp?doc_id=1326998.

In addition to the WLPs, we have evolved from the dual-stacked flash packages and PoP of the first iPhone to 16 dies stacked in a flash package, and thinner PoPs incorporating TSMC's InFO fan-out wafer-level packaging (FOWLP), as well as other FOWLP usage in RF and PMIC chips. The latest innovation, seen in the iPhone X, is the use of substrate-like PCBs for the motherboards. We are back to two boards, linked with high-density PCB interconnect.



iPhone X motherboards. (a) Top view of top board. Source: TechInsights. (b) Tilt view of underside of top board, showing high-density interconnect stack. (c) Bottom board. Source: iFixit.

I think we can conclude that mobile phones are now the main driver for both the process and packaging technologies in the semiconductor business.

When it comes to failure analysis, the move to nanotechnology and vastly more complex systems create a real challenge. This especially applies to the materials analysis side, because in some cases we are now counting atoms. Tracking down an errant signal in something like the latest phone strikes me as much worse than a simple needle in a haystack. Kudos to the designers and manufacturers who manage to weed out almost all of these potential problems before the phone gets to market!

ABOUT THE AUTHOR

Dick James is a 45-year veteran of the semiconductor industry and senior analyst for TechSearch International, based in Austin, Texas, a leading consulting company in the field of advanced semiconductor packaging technology. In addition, he is fellow emeritus for TechInsights, a Canada-based specialty, reverse engineering company, and a contributing editor for *Solid State Technology* magazine.

NOTEWORTHY NEWS

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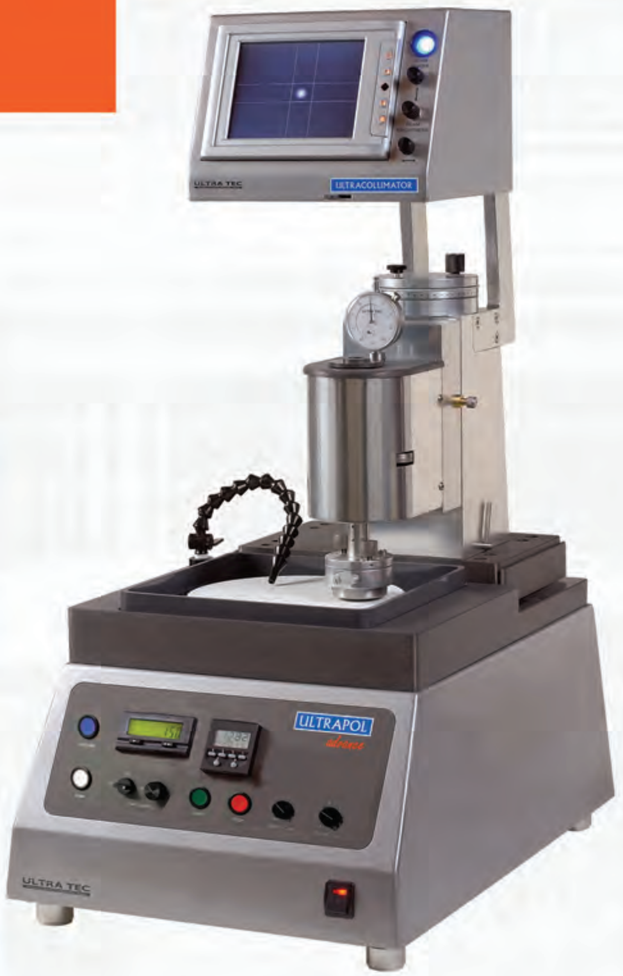
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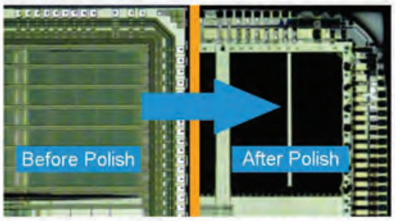
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After Polish

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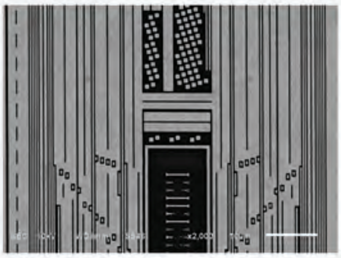

Copper layer after de-processing Magnification = 2000X

Small encapsulated packages after x-sectioning

Better sample alignment produces better polishing results

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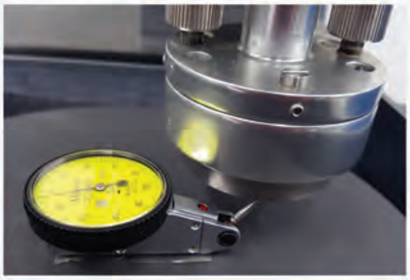
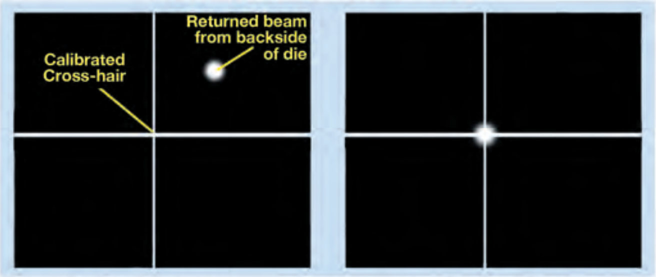


OPTICAL ALIGNMENT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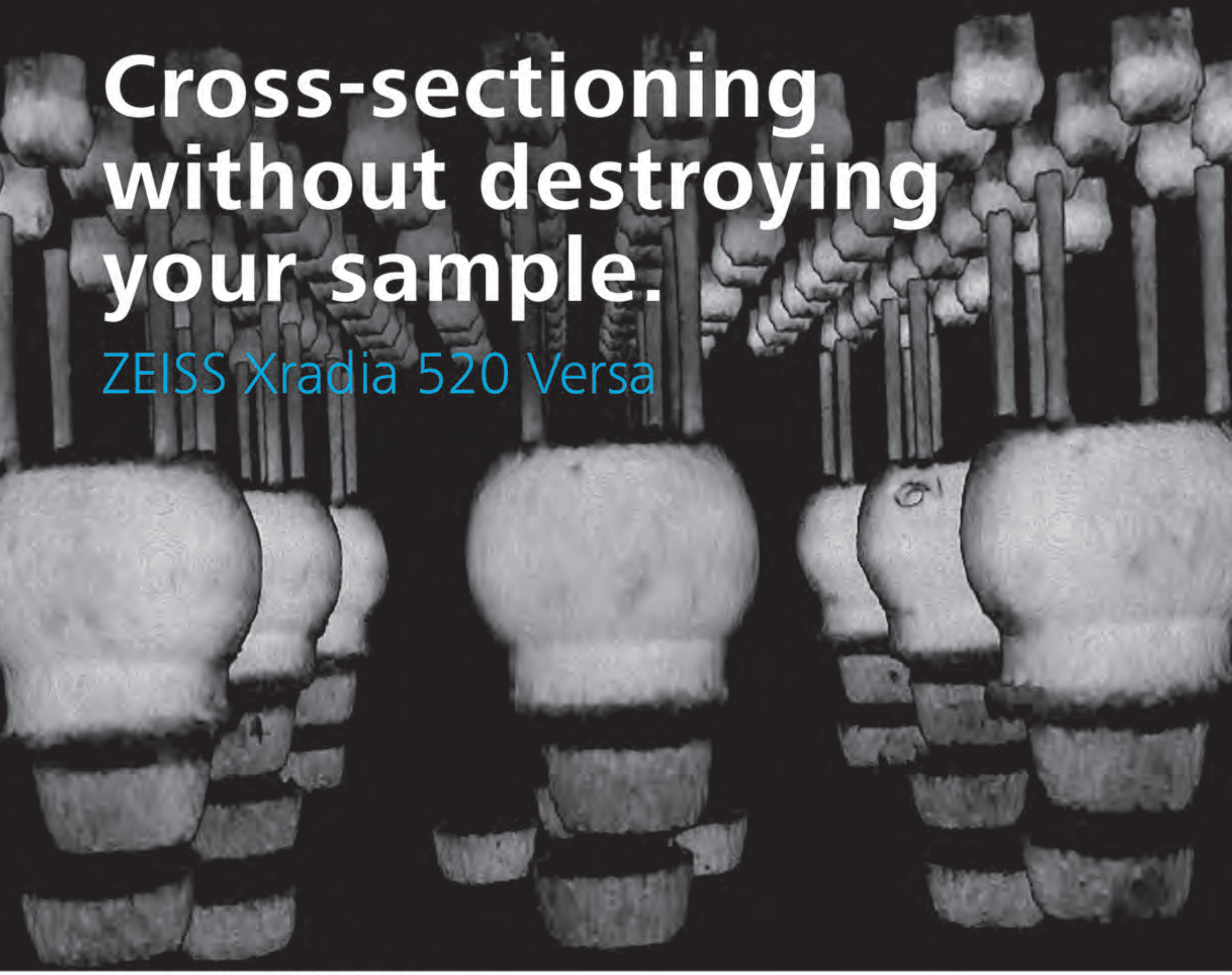
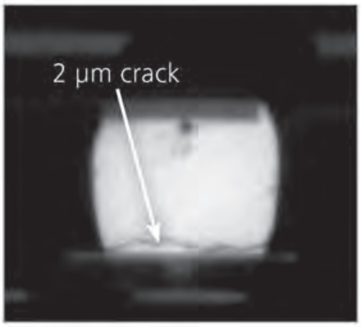
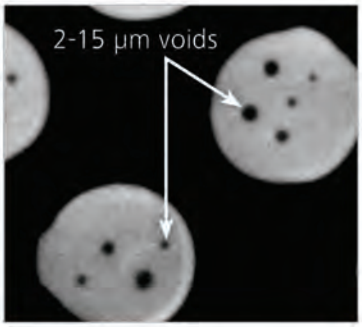


Image courtesy of AMD Failure Analysis Lab, Singapore



Virtual cross section



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