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MONOGRAIN DEFECT IN POLYSILICON GATES

DC/DC CONVERTER FAILS TO START UP WITHOUT OVERSHOOT DUE TO INTERACTION WITH INRUSH CURRENT SUPPRESSION CIRCUITRY

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THE GIFT OF TIME

Liz Marquard, EDFA Managing Editor
LZMarquard@aol.com

Fifteen years ago, while working as a copyeditor for ASM International, I was presented the opportunity to become Managing Editor of EDFA magazine. A brief outline of my new duties included the following directive: “Go out to California and attend ISTFA.” My response was, “What is ISTFA?” As you can see, my on-the-job learning curve was not just steep, it was absolutely vertical!

With the patience and guidance of then-Editor Chuck Hawkins, my education began. Chuck graciously answered my numerous questions, even though they must have been extremely elementary to him, such as, “What are MEMS?” I quickly discovered that I needed to learn a foreign language—“acronym-speak”—to decode cryptic manuscript sentences similar to: “The team performed a PFA on the DUT using SEM, FIB, AFM, EMMI, and IREM to search for EOS/ESD in the MOSFET at the FEOL.” Huh?

No one was prouder (or more relieved!) than me when the November 2003 issue—my first as Managing Editor—arrived looking great and containing all the necessary components. Each subsequent issue offered more opportunities for growth and learning. It has been a privilege to help guide the magazine to its current status as a full-color 56+ page quarterly packed with relevant information for a very responsive EDFAS constituency.

The best part of the learning curve has been my working relationship with the backbone of EDFA magazine: the Editorial Board and its outstanding former Editors, Larry Wagner, Chuck Hawkins, Ed Cole, Rose Ring, Mike Bruce, and current Editor, Felix Beaudoin. EDFA magazine is a success because of this incredibly dedicated group of professionals. I thank them for their insight, guidance, and humor as well as their tolerance of my well-known “nag-o-grams.” It has been an honor to work with such a fine and talented Board, who are not only my colleagues but also my friends.

After 15 years at EDFA’s helm, I have come to a pivot point in my life. What I want the most is not new professional challenges but rather the gift of time—time to travel, to play with my grandchildren, to finish writing my second novel, to read recreationally, and to wander away from my desk for long, leisurely spans.

My farewell ends with a favorite line, often attributed to Dr. Seuss (Theodor Geisel): “Don’t cry because it’s over. Smile because it happened.”

I leave you with a smile and a deep sense of gratitude for all that we have experienced and accomplished together.
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FAILURE MECHANISMS OF ELECTROMECHANICAL RELAYS ON PCBAS: PART I

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INTRODUCTION

Many printed circuit board assemblies (PCBAs) have relays that are soldered to the PCB. If such an electromechanical component fails, it can cause the whole device to fail, just like any other electronic component. The spectrum of root causes that lead to an increased contact resistance or a complete contact failure is totally different from what usually occurs in the electronics domain. This article provides a detailed analysis of these failures and the corresponding root causes, many of them self-centering.

In this overview about failure mechanisms of electromechanical relays, the failure analysis discussed and the corresponding root causes are limited to contact failures between two contacts in relays that are used to switch small loads (Fig. 1). The relay has five terminals. The two terminals on the left in Fig. 1 are wired to a coil that creates a magnetic field when a current is applied. The magnetic field moves the middle contact of the three terminals on the right in Fig. 1, which connects or disconnects to the left and right contact. Nickel/silver or silver/tin oxide is used as the contact material. Sometimes they are gold plated, but the failure mechanisms are incidental in the cases shown.

Fig. 1  X-ray of a common electromechanical relay. If an electric current is passed through the coil, it generates a magnetic field that activates the hinged armature on the left. The movement is transferred to a plastic slider, and the movable contact—here in the middle of the three contacts—either opens (normally closed) or closes (normally open) a connection with the fixed contacts left and right. The pins are soldered to the PCB.

Fig. 2  (a) Plastic chip from an edge of the plastic part. (b) Flux particle from a remote solder joint. (c) Solid plastic chip from a plastic part. (d) Flattened plastic particle exactly in the middle of the contact point
CONTACT FAILURE CAUSED BY NONCONDUCTIVE PARTICLES AND FILMS BETWEEN THE CONTACTS

The most common failure type for an electromechanical relay is a nonconductive particle lodged between two switching contacts. Frequently, the particle is a chip from a plastic part. Particles are also formed if metal parts scrape against plastic surfaces. This results in oxidized metal wear as well as plastic wear (Fig. 2a,c,d) and glass fiber fragments from the glass-fiber-reinforced plastic (Fig. 3, 4). Further, solid flux residues from soldering the copper wires of the coil to the pins can be found on the contacts (Fig. 2b).

It has been observed that nonconductive particles between two contacts do not appear by chance, but this is a self-centering failure mechanism.

The mechanical shock caused when two relay contacts open causes particles in the relay to bounce. An inhomogeneous electrical field is simultaneously built up, which exerts a force on the particles. They are pulled in the direction of the force. It may take tens of thousands of switching operations, but, at some point, the particle finally reaches the center of the force. A very thin film of oil is often used in relays to prevent this type of failure. These particles adhere to this thin film of oil and do not move, due to inhomogeneous electrical fields.

CONTACT FAILURE CAUSED BY CONTACT OIL

If contact oil is used in electromechanical relays, the type of oil used and the quantity applied are very important factors. Perfluoroether is common and a good choice; however, the quantity is critical. If the oil is applied undiluted in a layer more than a few micrometers thick, then another self-centered failure mechanism can occur. Particles stick on the oily surface (Fig. 5a). If the oil film is too thick, it acts as a liquid, and the fluid coalesces in the capillary around the contact point (Fig. 5b). When the contacts separate, the surface of the oil is pulled into the direction of the contact point, as are the particles that have attached themselves to the fluid (Fig. 5c). After a number of switching operations, the particle reaches the contact point (Fig. 5d) and causes the failure. Figures 6 and 7 show examples of a glass fiber and a plastic particle that have been pulled to the contact point.

ELECTRICAL ARCING DUE TO LARGE PARTICLES BETWEEN THE CONTACTS

If a large particle prevents the contacts from being tightly closed, an electrical arc may build up, depending on the diameter of the particle and the applied voltage. In air, there is a basic rule that an electric field of 1000 Volts/mm distance (1 V/µm) is required for an electric arc. This means that 24 V can arc over a distance of 24 µm. Oil between the contacts usually overrides this rule. An arc
is nearly impossible. However, if an arc does form, the oil will evaporate, catapulting the contact open. A sizzling sound can be heard, because this effect may be repeated several times.

If the particle is located somewhat away from the shortest distance between the contacts, it will not burn or sink into the molten contact surface. The arc can continue to burn for a long time. If direct current is involved, then material can also be transported, forming a tip and a hole. The failure manifests itself in such a way that a higher contact resistance is measured (Fig. 8, 9).

**SILICONE OIL OR SILICONE VAPOR IN AN ELECTRIC ARC IS TRANSFORMED INTO SILICON DIOXIDE**

Contact failure is not caused just by solid particles. If electric arcs occur and silicone oil or silicone vapor is present, the silicone is oxidized to silicon dioxide (SiO$_2$), in the solid form commonly known as quartz or glass. This nonconductive silicon dioxide condenses as an insulating layer in just the contact region. The process is again self-centering because the highest fields occur at the shortest distance, which is the contact region (Fig. 10).

Part II of this article, which will appear in the May issue of *EDFA*, will discuss the formation of nitrous gases caused by arcing and the formation of phosphoric acid crystals on contacts, resulting from the addition of red phosphorus as a flame retardant to certain plastic materials. It also will discuss why sealed relays, which pop open during soldering, are prone to precisely this type of failure. Finally, a failure mechanism due to wax, which is used as a lubricant for the enameled copper wire of the relay coils, will be discussed.
Fig. 8  Contact failure caused by metal wear. Arcing occurs and burns the contact surfaces.

Fig. 9  If a particle blocks the contact, and if the distance between the contact surfaces is not too large, arcing can occur (basic rule: 1 V/µm in air). The arc burns at the point, which represents the closest distance between the contacts. If the particle (see arrows for the mark) is located somewhat away, it will not burn or sink into the molten contact surface. Material can be transported if direct current is involved, forming a tip and a hole.

Fig. 10  The black regions in the scanning electron microscopy image of the contact point of a failed relay contact indicate nonconductive layers. They consist of silicon dioxide, shown in the energy-dispersive x-ray spectrograph. The SiO₂ is produced in the electrical arc from silicone vapor and condenses in the contact region.
ABOUT THE AUTHOR

Gert Vogel studied physics in Stuttgart. He has been with Siemens for more than 32 years. Dr. Vogel was a semiconductor technologist in Siemens’ DRAM production in Munich and Regensburg for seven years. He then moved to Siemens Amberg, where one of his specialties is the failure analysis of electronic components on printed circuit board assemblies. He led a tutorial, “Avoiding Flex Cracks in Ceramic Capacitors,” at ESREF 2015. This was followed by a tutorial, “Creeping Corrosion of Copper on Printed Circuit Board Assemblies,” at ESREF 2016.

EDFAS BOARD OF DIRECTORS

2018 CALL FOR NOMINATIONS

Cheryl Hartfield, Chair, EDFAS Awards and Nominations Committee
Past President, EDFAS
Cheryl.hartfield@zeiss.com

EDFAS is soliciting nominations for candidates for the EDFAS Board of Directors. Nominations are for member-at-large Board positions for three-year terms beginning October 1, 2018, through September 30, 2021. There are expected to be up to three positions open for nomination, and any members of EDFAS in good standing are encouraged to nominate themselves or another member for one of these positions. The incumbents may also seek re-appointment by notifying the Awards and Nominations Committee Chair, Cheryl Hartfield (Cheryl.hartfield@zeiss.com).

Nominations are due March 1, 2018. Candidates who initiate or accept nomination will be asked to provide a three-page nomination package that includes the candidate’s:

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- Photograph and contact information

Nomination packages should be sent to Mary Anne Jerson at 9639 Kinsman Rd., Materials Park, OH 44073-0002 or maryanne.jerson@asminternational.org. For more information or questions, call 440.338.5151, ext. 5539.

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INTRODUCTION

There is a tricky soft electrical failure that is hard to identify in electrical test validation and, if undetected, could generate fails in products delivered to customers. Such failure occurs more often at high $V_{DD}$ and high frequency, limiting the maximum reachable frequency. It happens only at very low levels—2 or 3 ppm—but impacts critical paths, clock trees, scan chains, or memory cells, which can lead to zero yields. The tricky failure, exacerbated by transistor scaling, is observable mostly on technology nodes below 40 nm. The failure is caused by a defect that gives very few signatures during failure analysis localization because of its dynamic failure mode with a test sequence that is hard to set up. It does not show abnormality in parametric measurements when probing isolated transistors, because of its transient electrical activation. Finally, it does not show visible and morphological defects in physical analysis using classical techniques such as transmission electron microscopy (TEM) lamellae, and it requires advanced techniques such as nanobeam diffraction\[1\] to be observed. However, after many failure analysis cases and using some experimental techniques, the authors are now able to recognize the symptoms of this failure, observe the defect, and limit the impact on electrical timing margins with both design and process corrections. The defect has been identified as a monograin defect in the polysilicon gate of the transistor.

ELECTRICAL BEHAVIOR

What is the common electrical failing factor between a scan chain working in scan mode but failing in capture mode and a memory cell failing at high voltage? In the case of the monograin issue, both are related to the clock frequency. The defect directly impacts the signals gated by the clock pulse width, leading to a delay increase.

For circuits with cores running at high frequency, it is difficult to check the value of internal logic states at speed directly at the chip interfaces. The I/O at the interfaces of the integrated circuit has too much capacitive load and self-inductance to properly output high-frequency signals. Therefore, validating the logic states can be done only at low frequency. A scan chain is used to cover this test. It takes a picture of the logic state at a given moment using the same high-frequency clock that is running the core of the circuit; this is the “capture” sequence. The data are memorized into the flip-flop registers of the scan chain, as shown in Fig. 1. The data are serially shifted out of the circuit using a low-frequency clock and can be read by automatic tester equipment; this is the “scan” or “shift” sequence. To summarize, the capture sequence uses an internal clock with a small pulse width, resulting in a capture fail if there is a monograin defect, and the shift sequence uses an external clock with a large pulse width to allow external observation without any additional failures. A complete scan chain test sequence is alternating scan and capture modes.

In the case of a memory cell failure, it is more or less the same approach. The external clock driving a memory block is self-formatted by the memory into a small clock pulse width; this is referred to as self-timing. It allows high-speed operations by shrinking the clock period to the maximum frequency allowed by the memory. It also saves dynamic consumption by reducing the memory bitline time to discharge. Like the scan chain, memories are also sensitive to the monograin defect when it affects signals gated by short clock pulse widths.

FAILURE ANALYSIS AND DEFECT LOCALIZATION

The failure mode of the monograin defect is very specific. It is visible with transient, dynamic test sequences and only with the clock “at speed.” It is identified as a transition fault by scan diagnosis systems; static failure analysis techniques such as photoemission and static
laser stimulation cannot be used. Candidate circuits for failure analysis are chosen because their boundary failing conditions show soft fail behavior versus supply voltage. Only two techniques provide usable results: dynamic laser soft defect localization (SDL)\(^2\) and laser voltage probing (LVP).\(^3\) No signatures were obtained with other techniques (emission microscopy, laser frequency imaging).

Using a \(220\times\) (2.45 NA) solid immersion lens with an 8\(\times\) laser scan magnification through the backside of the silicon, the SDL signature provides very accurate localization of the failure, highlighting the PMOS of a gate controlled by the internal clock. Figure 2 shows the location in a flip-flop for the scan chain failure case, and a similar result is found in the memory failure case.

**Fig. 1** (a) Schematic of a scan chain used to capture values in the high-speed core logic using the high-frequency internal clock (capture mode) and then shifting the data out of the circuit in serial through the flip-flops using an external low-frequency clock (scan or shift mode). (b) Timing diagram of Ck_FF for several scan/capture sequences

**Fig. 2** (a) Shmoo plot showing electrical test setup configuration of the test sequence for a scan chain failure leading to SDL in (b). A PMOS gated by the clock is highlighted in a flip-flop.
The LVP technique integrates voltage waveforms acquired on each transistor of the flip-flop. It requires a looping test sequence with all the measured signals synchronized with the trigger signal of the loop. Unfortunately, the scan chain failure is on the capture test sequence, which utilizes a high-speed clock generated by an internal phase-locked loop, not synchronized with the trigger signal. The failing test sequence is not visible using LVP.

To address the LVP limitations, the shift test sequence (showing no functional failures) is used because it operates with an external clock. Even if this sequence is always “pass,” the signals acquired on the clock-gated transistor highlighted in SDL show an abnormally slow transition on the rising edge (PMOS1), which generates delays after reformatting of the post-transistor stages (PMOS2 and PMOS3), as shown in Fig. 3.

(continued on page 14)
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With the “passing” shift test sequence, the delay generated by the failing flip-flop is "caught up" by the next flip-flop, due to the DATA-to-CK setup time, and is invisible. With the capture test sequence, the output signal of the failing flip-flop is stuck and propagates along the scan chain. The same behavior is observed on a failing memory with a self-timed test sequence using the internal clock and a non-self-timed sequence.

**ELECTRICAL FAILURE MECHANISM**

When the flip-flop fails, a test sequence with a short clock pulse width is involved. The transition at the output is not generated because the clock goes low before the critical PMOS1 has finished switching. Figure 4 shows that the falling edge of the clock is acting as a timing clamp. If the signal generated by the critical PMOS is affected by a monograin switch before this “timing limit,” there is no fail and it is not possible to detect the monograin even if it is present. If the signal is too slow and switches after this limit, the transition is clamped before the signal reaches a high level, and a fail is generated. The monograin defect is sensitive to the supply voltage and is detected here by clock pulse width variations.

**PHYSICAL ANALYSIS**

In the case of the scan chain, PMOS1 is clearly

![Fig. 4](image-url)  
**Fig. 4**  
Signal rising edge of a failing transistor impacted by a monograin defect. Failure is strongly linked to the pulse width of the clock.

![Fig. 5](image-url)  
**Fig. 5**  
(a) Layout including the fail and a reference PMOS for TEM lamella observation along the width of the transistor.  
(b, c) No morphological difference is observed in TEM and STEM.  
(d) One main orientation (one color only) of the polysilicon grain is revealed on the failing transistor in dark-field imaging.
identified as the failing location. After deprocessing of several failing dice down to the contact level, the static parametric characteristics of that PMOS are measured and compared with a good reference transistor in nano-probing. The measurements show a perfectly working transistor. This result proves that the defect has pure dynamic and transient effects. Observing the defect with TEM was very costly in terms of used candidates until a good orientation was finally found for lamella extraction: lengthwise of the polysilicon gate, along the width of the transistor. Nevertheless, the defect is still invisible in classical TEM or scanning-TEM (STEM). Figures 5(b) and (c) do not show any difference between the failing transistor and a reference one. Before concluding that the failing transistor has no anomalies, TEM dark-field imaging (Fig. 5d) provides qualitative results on the microstructure: one main orientation difference is observed through the polytungsten of the failing PMOS.

Due to artifacts in the diffraction contrast leading to shadow areas, dark-field imaging always leaves some doubts in the interpretation of the polysilicon gate grain orientation. The nanobeam electron diffraction (NBD) technique is used for quantitative measurement of the grain orientation, providing more reliable results. The principle of NBD is rather simple. As shown in Fig. 6, a parallel electron beam with small diameter is formed in the TEM and scanned across the sample. The resulting diffraction patterns are recorded and analyzed for each location with a high-speed, high-resolution charge-coupled device (CCD) camera. Local orientation and phase information on polycrystalline materials can be extracted from diffraction spot positions.

Approximately 50 NBD patterns are acquired over a line profile in the polysilicon of the reference and failing PMOS transistor using an electron probe size of 5 nm. Figure 7 shows different diffraction patterns along the gate, revealing multiple grains through the polysilicon. On the failing PMOS, the same lattice plane is systematically present through the polysilicon; one main diffraction pattern is observed, revealing only one grain in the gate of this transistor.

The synchronization between e-beam scanning and the fast-acquisition CCD camera (up to 200 patterns/second) with postprocessing computation of the data allows the transposition of line profiles into automatic crystal orientation/phase mapping (ACOM). It produces an orientation map similar to electron backscatter diffraction in scanning electron microscopy based on the collection of electron diffraction patterns and cross-correlation comparison with simulated ones. The acquisition time is limited by the capture rate of the CCD camera; a mapping of 200 × 200 pixels using a probe size of 10 nm with a step...
size of 10 nm takes approximately 7 min. Figure 8 shows a grain orientation map acquired with this technique on a good and a bad NMOS memory bitcell in a 28 nm fully depleted silicon-on-insulator (FD-SOI) technology. Several polysilicon grains with multiple orientations are visible on the reference transistor, whereas only one major big monograin (colored blue and green) is observed on the bad NMOS.

**FAILURE ROOT CAUSE**

Obviously, control of the grain size during the polysilicon gate process is one of the key factors to reducing the occurrence of this failure. However, the monograin itself cannot explain the electrical behavior of the failing transistors. An energy-dispersive x-ray (EDX) chemical analysis comparison conducted on two NMOS transistors (one is reference, one is fail) of a monograin failure in a memory bitcell permits a deeper explanation of the mechanism and the consequences of the failure. In Fig. 9, the reference transistor shows a good arsenic dopant diffusion along the grain boundaries of the polysilicon toward the TiN surface. On the bad NMOS, no arsenic diffusion is visible through the monosilicon grain, because there are no grain boundaries. The arsenic is blocked at the polysilicon/NiSi interface. This comparative EDX study is still ineffective on PMOS because it is very hard to acquire the boron x-ray signature.

The lack of dopants at the poly/TiN interface due to a monograin (no diffusion path) in the polysilicon gate leads to degradation of the transistor electrical dynamic performance. The gate is not more metallic and acts as a semiconductor; this leads to an extra delay due to excessive added capacitance and generates a triggering threshold that acts as a Schottky diode. The observation of missing dopants allowed a technology computer-aided design (TCAD) model to be built based on a Schottky diode on the gate, simulating the electrical behavior of

![Fig. 8](image)

**Fig. 8** Orientation map acquired using ACOM on a reference and a failing NMOS from a memory bitcell in a 28 nm FD-SOI technology. Multiple polysilicon grains and orientations are visible on the reference transistor, but only one big monograin is observed on the failing MOS.

![Fig. 9](image)

**Fig. 9** TEM EDX chemical analysis on an NMOS transistor in a 28 nm memory bitcell. Arsenic diffusion through grain boundaries is visible on the reference transistor, while it is blocked at the polysilicon/NiSi interface due to the monograin on the bad transistor.
a monograin-affected transistor. It allowed the development of a dedicated simulation program with an integrated circuit emphasis (SPICE) model that was used to reproduce, at the design level, observations (signal slope/delay) acquired with LVP.

**CONTAINMENT AND CORRECTIVE ACTIONS**

The monograin issue is closely linked to both process and design factors. Several containments have been applied at the process level, such as doping of transistors, control of grain growth, optimization of the polysilicon height, and so on. At the design level, because the monograin strongly depends on scaling, critical transistors have been redesigned to avoid or minimize the occurrence and impact of gate monograin issues. High-speed clock-driven gates with small poly areas have been replaced with a longer poly shape, review of some regular poly layout, automatic detection algorithms included in the verification flow, margin simulations using the dedicated SPICE model developed for the monograin issue, and so on. All of these “robustization” actions concerning the monograin issue affecting just a few parts per million of transistors led to a significant gain in yield and better margins in maximum frequencies.

**CONCLUSION**

Finding the monograin failure mechanism required a high number of failing parts and was time-consuming. Even though failure localization was quite “classical” in the failure analysis flow using SDL and LVP, the difficulties occurred at parametric verification during nanoprobng and TEM analysis. Electrical measurements showed proper transistors, and physical observation in the TEM showed a proper morphological device. It was difficult to be convinced that the located failing transistor was the correct one until the monograin failure hypothesis was tested using TEM observation along the gate instead of across the gate of the transistor. Failure analysis of the monograin required the use of techniques from material crystallography analysis, such as nanobeam diffraction with automatic crystal orientation/phase mapping, to prove the single orientation of the grain compounding the gate. With the support of TCAD and design, test, and process teams, the root cause and failure mechanism has been clearly explained, leading to the production of dedicated physical and electrical simulation tools to resolve the failure mode. Transistor gates have now been “robustized” by design and optimized in process to limit the effect of this specific defect that impacts integrated circuits of nanoscale technology nodes.

**REFERENCES**


**ABOUT THE AUTHORS**

**Thierry Parrassin** obtained a Master’s degree in microelectronics from the Institut National Polytechnique de Grenoble in 2010. He joined STMicroelectronics as a failure analysis technician in 1999, where he is currently a failure analysis engineer. His mission is to support both manufacturing and research and development activities on site through basic and advanced failure analysis. Thierry is a specialist in test engineering, design debug, defect-localization techniques, photoemission (emission microscopy), laser stimulation mapping (OBIRCH, TIVA, laser-assisted device alteration, soft defect localization, fault injection mapping), laser mapping (laser voltage imaging, variation mapping, thermal frequency imaging, second-harmonic degradation mapping), and contactless
ABOUT THE AUTHORS (cont’d)

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ERRATUM FOR NOVEMBER ISSUE’S sMIM ARTICLE

In the November ’17 issue of EDFA magazine, an incorrect image was inadvertently inserted in Fig. 2 on p. 13 of “Nanoscale Capacitance and Capacitance-Voltage Curves for Advanced Characterization of Electrical Properties of Silicon and GaN Structures Using Scanning Microwave Impedance Microscopy (sMIM)” by Oskar Amster, Stuart Friedman, Yongliang Yang, and Fred Stanke. Here are the correct image and caption as well as the corresponding text from the article.

The staff of EDFA magazine regrets any confusion caused by this error.

“The sMIM-C measured on various bulk dielectrics shows a clear linear relationship between sMIM-C and the log of the permittivity. The red squares shown in Fig. 2 are from a model that originates with a finite-element calculation of the tip-sample admittance for the conical geometry of the sMIM probe. The origins of the log(ε) dependence can be seen in analytical models for spherically terminated conical tips above and in contact with linear materials, documenting the origin of the log dependence published by other researchers.”
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The desire for smaller, lighter, and faster products drives the development of 2.5-D/3-D integration technologies that can use tens of thousands of connections per die. Micro-copper pillar geometries have been widely adopted because their small size and fine pitch provide high thermal conductivity, higher input/output (I/O) density, and resistance to deleterious electromigration effects. In micro-copper pillars, SnAg solder is electroplated on top of a copper pillar. Because of the small volume of solder employed, intermetallic compounds (IMCs) comprise a significant fraction of the resulting solder joint, and very fine Ag$_3$Sn precipitate morphologies can occur. Thus, the microstructure of SnAg solder/copper pillar microstructures varies significantly from that of larger solder joints, such as flip-chip solder joints. Furthermore, 2.5-D applications include interposers of distinctly different materials, such as silicon or glass. The different properties of these materials, such as coefficient of thermal expansion (CTE), affect the thermomechanical response of the package to temperature excursions and the lifetime of the package. Thus, behaviors of copper pillar packages during accelerated thermal cycling (ATC) were examined. Correlations between the shear strength and microstructure of copper pillars were examined for different solder compositions and for different aging times. Microstructure analysis (e.g., Ag$_3$Sn precipitate morphology) was performed with both optical and scanning electron microscopy (SEM). The effects of thermal aging on the growth of intermetallic compounds, the Ag$_3$Sn precipitate morphology, and the mechanical properties of micro-copper pillar bumps were examined. The shear strength performance of micro-copper pillars with three different bump diameters (30, 50, and 100 µm) was also evaluated. Results were considered in terms of variations in the precipitate morphology and in terms of increases in the thicknesses of intermetallic layers at micro-solder/substrate interfaces. The ATC test results for two different interposers (silicon and glass with high CTE) are discussed.

INTRODUCTION

Varying the processing of lead-free solder joints affects their microstructure and their reliability. Important examples are changes in geometry, solder composition, or thermal history. Each factor can significantly affect solder joint microstructure and mechanical behavior. The Ag$_3$Sn precipitates coarsen during aging and lose their effectiveness in hindering the motion of dislocations, particularly aging at elevated temperatures. Geometry is also an important factor. Smaller solder joints undergo more after reflow and solidify at lower temperatures, generally resulting in a more refined microstructure. Thermal history, most importantly aging time, can also significantly affect lead-free solder joint microstructure and mechanical behavior. The Ag$_3$Sn precipitates coarsen during aging and lose their effectiveness in hindering the motion of dislocations, particularly aging at elevated temperatures.

The present study seeks to better characterize and understand interactions among processing, microstructure, and the properties of lead-free solder joints in copper.
pillar geometries. The very large decreases in solder volume realized in copper pillar solder joint geometries (Fig. 1) would be expected to affect initial microstructures. Changes in solder joint composition and thermal history are correlated with the microstructure, shear strength, and ATC lifetimes of solder joints. The precipitate morphology is compared with changes in solder composition and aging time at elevated temperature. All of these values were correlated to solder joint mechanical properties in an effort to better understand and control copper pillar solder joint reliability. Copper pillars are much stiffer than lead-free solder, resulting in higher stress during assembly processes and in use, with the possibility of reduced reliability because fracture or delamination may occur. Therefore, studies of the mechanical and reliability properties of packaging interconnect copper pillar joint structures are critical.

The present investigation was focused on the reliability of silicon/micro-copper pillar/solder/glass assemblies and silicon/micro-copper pillar/solder/silicon assemblies—fundamental building blocks of 2.5-D packaging. These studies should also be relevant to 3-D packaging, where copper pillars are also used. The inclusion of glass interposers in this study is important, because these materials are important new alternatives to through-silicon interposers; glass interposers are relatively stable, low cost, and afford great flexibility in manufacturing arbitrary sizes.[7-9] The investigation used shear strength measurements and ATC tests to characterize the reliability of silicon/micro-copper pillar/solder/glass assemblies with a wide range of parameter values, including a varied range of pitches. Previous investigations of the shear strength of copper pillar solder joints have revealed sensitivities to the thickness of intermetallic compounds in the joint, shear speed, and shear height.[11-30] This study incorporates these variables and extends such investigations to include careful correlations with solder composition, substrate chemistry, solder joint microstructure, and the results of ATC tests with assemblies with the same copper pillar solder joints.

**EXPERIMENTAL PROCEDURES**

**FABRICATION OF SUBSTRATE AND CHIP (TOP DIE)**

The substrates were metallized to allow continuous monitoring of the electrical resistivity of most of the solder joints. The substrate wiring extended beyond the chip area to an array of test probe pads. For both glass and silicon interposer substrates, a 0.8 µm SiO₂/0.8 µm SiN bilayer was deposited prior to the wiring deposition. A serpentine line was created by alternating lines between the chips and the substrates. The thin-film structure consisted of two levels of wiring. The first level, on top of the SiN layer, was fabricated by electroplating 3- to 4-µm-thick copper lines, either 15 or 20 µm wide, depending on the copper pillar pitch. This was followed by a dual dielectric layer of 0.6 µm of SiN and 3 µm of photosensitive polybenzoxazole (PBO) dielectric. Then, the top layer was deposited as either 7 µm of copper or 2 µm of nickel/0.08 µm gold on the substrate or copper pillar structures on the chips.

Silicon wafers with copper pillar structures, and both glass and silicon interposer substrate, were fabricated at IBM. Three different interposer materials were metallized at IBM: two Corning glass interposer substrates (one with a CTE of 3 ppm/K and one with a CTE of 8 ppm/K) and a silicon interposer substrate (wafer). Separate silicon wafers were fabricated with copper pillars and solder cap at IBM in a proven, standard lithography process. The pad diameters were 30, 50, or 100 µm, while the pitch was 90, 140, or 190 µm, respectively. Three different copper pillar heights were produced for each pad diameter (15, 25, or 35 µm). Solder compositions of Sn, Sn0.9%Ag, Sn1.8%Ag, and Sn2.4%Ag were deposited at layers of 10 or 20 µm thick (Table 1).

Results were correlated with careful characterizations of microstructure and a wide range of parameter values, including copper pillar height, aging time, solder and metallization compositions, and number of reflows. Different assemblies were fabricated, allowing variation of a number of different parameters, including interposer
substrate material, copper pillar and solder heights and diameters, underbump metallization, and solder composition (Table 1).

**FABRICATION OF TEST ASSEMBLIES**

Copper pillar assemblies were fabricated at Universal Instruments Corporation, which included a 60 × 60 mm interposer substrate metallized with a single pad diameter and associated pad pitch in a pattern that accommodated four similar silicon “chips” (each bumped with copper pillars) (Fig. 2, 3). Copper pillars were dipped in flux and placed on the glass or silicon substrate using an automated pick-and-place machine. Soldering was performed in a forced convection reflow oven with a nitrogen atmosphere. Peak solder joint temperature during the reflow process was measured on a setup board to be between 240 and 245 °C, and the time above liquidus was 64 s. After reflow, all assemblies were inspected electrically using an ohm-meter and through x-ray imaging. (X-ray imaging itself was not sufficient to reveal an acceptable solder joint formation during the assembly process, due to the small size of the joints.) The design allowed the electrical continuity of most of the solder joints (including the corner joints) to be continuously monitored during the ATC test. As seen in Fig. 2, the substrates were designed to be tested in multiples of four testable units.

**MICROSTRUCTURE CHARACTERIZATION**

Samples were mounted in epoxy for metallographic sectioning after reflow and after reliability testing. Also, copper pillar samples (chip) and substrate (both glass and silicon) were analyzed. All the samples were ground in a series of steps with abrasive paper, polishing cloths with diamond suspension, and finally with a 0.02 µm colloidal silica suspension. Great care was used with each polishing step to remove as much damage as possible from the substrate material, copper pillar and solder heights and diameters, underbump metallization, and solder composition (Table 1).

### Table 1  Tests parameters in the current study

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interposer substrate material</td>
<td>Low-CTE glass (≈3 ppm/K)</td>
</tr>
<tr>
<td></td>
<td>High-CTE glass (≈8 ppm/K)</td>
</tr>
<tr>
<td></td>
<td>Silicon</td>
</tr>
<tr>
<td>Copper pillar and solder cap heights</td>
<td>25 µm Cu + 10 µm solder</td>
</tr>
<tr>
<td></td>
<td>15 µm Cu + 20 µm solder</td>
</tr>
<tr>
<td></td>
<td>15 µm Cu + 10 µm solder</td>
</tr>
<tr>
<td></td>
<td>35 µm Cu + 10 µm solder</td>
</tr>
<tr>
<td>Solder cap composition</td>
<td>Sn, Sn0.9%Ag, Sn1.8%Ag, Sn2.4%Ag</td>
</tr>
<tr>
<td>Copper pillar pad diameter</td>
<td>30, 50, and 100 µm</td>
</tr>
<tr>
<td>Metallization layer, component side</td>
<td>Nickel, copper</td>
</tr>
<tr>
<td>Metallization layer, substrate side</td>
<td>Electrolytic nickel/gold, copper</td>
</tr>
</tbody>
</table>

![Fig. 2](image2.png)  Test assemblies were built using the surface-mount technology process, with four similar silicon 12 × 12 mm “chips” (with copper pillars) placed on silicon or glass substrates (60 × 60 mm).

![Fig. 3](image3.png)  Detail of assembly at the corner of the package (“chip” with copper pillars) from Fig. 2. The design allowed the electrical continuity of most of the solder joints (including the corner joints) to be continuously monitored during the ATC test.
previous polishing step. With the final polishing step, the goal was to have no polishing damage (neither scratches nor crystal deformation) left in the tin as a result of specimen preparation.

The specimens were imaged using optical metallography in both bright-field imaging and polarized light, with the polarizers nearly crossed (cross polarizer, or XP, imaging). The XP imaging contrast in tin arose from the birefringent properties of tin, leading to different colors for different crystal orientations of tin under XP imaging.\[31\] Selected specimens were imaged using SEM. Images were taken using backscatter electron (BSE) imaging. In BSE composition mode images, contrast is proportional to the average atomic number of the material.

MEASUREMENTS OF SHEAR STRENGTH

The shear strength tests were conducted using a DAGE Series 4000 Plus bond tester. The shear loading speed was 700 µm/s (with a maximum test load of 400 g) (Fig. 4), in accordance with the JEDEC JESD22-B117A standard.\[32,33\] Measurements done at room temperature were repeated on multiple nominally identical samples. The dependence of shear strength on system parameters (e.g., solder composition, size, and aging time) and on shear strength measurement parameters, such as shear height, was examined. Shear test was performed on both copper pillar and solder cap.

ACCELERATED THERMAL CYCLING TEST

An ATC test was performed at Universal Instruments Corporation. A –40/125 °C ATC test was used with 15 min dwell times at the temperature extremes and 9 °C/min transition rates between the extremes, consistent with IPC-9701 criteria.\[34\] A solder joint failure was defined when the resistance of the joint exceeded 900 Ω. Generally, after failure was detected, samples were removed from the chamber for microstructural characterization.

RESULTS

The effect of composition and aging on the microstructure and shear strength of copper pillar solder joints was examined. The microstructure of the solder joint was evaluated in the as-fabricated configuration and after aging. Varying the solder composition or the thermal history of SnAg or SnAgCu solder joints affects their microstructure and their mechanical response.\[1-6\] The number, size, and arrangement of Ag3Sn precipitates affect the mechanical response of Sn-Ag-Cu near-eutectic solder joints and their reliability.\[1–8\] A large number of fine Ag3Sn precipitates (Fig. 5) would be expected to be much stronger than one with a few large Ag3Sn precipitates (Fig. 6, micrographs for aged samples). A number of different thermal history parameters influence the Sn-Ag-Cu microstructure, including aging time. A fine Ag3Sn precipitate morphology in Sn-Ag-Cu solder (such as that of Fig. 5) will coarsen over time, particularly at elevated temperatures, and the mechanical properties of the solder would be expected to change. These effects were examined for copper pillar solder joints before and after aging.

The effect of silver concentration on the microstructure of copper pillar/SnAg solder joints is illustrated in Fig. 5. A number of Ag3Sn precipitates are seen in all of the joints containing silver, even for the solder joint with solder containing 0.9% Ag. The spacing between precipitates ranged from 0.1 µm to approximately 2 µm, with more submicron spacings for the solder joint containing 2.4% Ag.
(Fig. 5). Such fine spacings between Ag$_3$Sn precipitates were observed at essentially all points in the tin matrix of the copper pillar solder joints. In contrast to larger lead-free solder joints (see, for example, Fig. 1), where recalescence causes much of the joint to solidify at or near the melting temperature of the alloy, these much smaller copper pillar solder joints would not increase in temperature as much after initial solidification. Thus, a more homogeneous distribution of fine precipitates would be expected to be observed (Fig. 5, 6).

Aging these copper pillar solder joints resulted in a dramatic decrease in the number of Ag$_3$Sn precipitates in the solder joint. Aging was conducted at a temperature of 125 °C for a period of 1000 h, resulting in significant coarsening of the precipitates (Fig. 6). The number of precipitates in a cross section of a typical solder joint decreased from several hundred to less than ten for all silver concentrations (Fig. 7).

Measurements of shear strength were conducted on copper pillar/SnAg solder joints to examine separately

![Fig. 5](image1.jpg) SEM micrographs of copper pillar pad diameters of 100 µm with different solder compositions, as noted in the figure on the silicon chip. The Ag$_3$Sn precipitate morphology was observed to change with silver composition in the solder.

![Fig. 6](image2.jpg) Backscattered SEM images of two category copper pillars on the left after reflow. The right is after 1000 h (6 weeks) of aging at 125 °C. The number of Ag$_3$Sn precipitates has decreased, while their size is increased. Pad diameter of pillars is 30 µm on the silicon chip.

![Fig. 7](image3.jpg) Quantitative analysis for the number of Ag$_3$Sn precipitates as a function of aging time for pad diameters of (a) 100 µm and (b) 30 µm.
precipitates was approximately 10 µm, so the precipitates no longer significantly hindered dislocation movement.

In 30-µm-diameter copper pillars, the shear strength of the copper pillar and the solder. Scanning electron microscopy examination of the metal remaining on the pad after shearing (Fig. 8a) and energy-dispersive analysis (Fig. 8b), along with plots of the force versus displacement (Fig. 8c), provided insight on the nature of the failure in the solder joint. If the force-versus-displacement plot indicated ductile failure (Fig. 8c), and the majority of the remaining metal on the pad was tin (Fig. 8b), then the indication was ductile failure in the solder. This was confirmed in the present case by SEM micrograph of a cross section of the shear solder joint (Fig. 8d), which revealed a significant amount of solder remaining on the pad. Solder failure was observed to be ductile for all samples tested, including all compositions, as-reflowed and aged samples, for both pad diameters.

Measurements of shear strength were conducted for a variety of copper pillar/solder joints, both as-reflowed and after 1000 h of aging at a temperature of 125 °C (Fig. 9). Three different solder compositions were studied, with different silver concentrations, and two different copper pillar diameters were examined: 30 and 100 µm. After aging, the values for shear strength were essentially the same for all samples, with values near 23 MPa. This correlated with the observation that the Ag₃Sn precipitates had coarsened significantly in all of the samples after aging, leaving few (less than ten) precipitates in a given cross section. The spacing between precipitates was approximately 10 µm, so the precipitates no longer significantly hindered dislocation movement. In 30-µm-diameter copper pillars, the shear strength of

Fig. 8 Shear strength of solder cap after 1000 h aging. (a) Top view for failure of sample with pad diameter of 30 µm. (b) Energy-dispersive x-ray analysis to prove the failure type. (c) Force vs. displacement plot for pad diameter of 100 µm. (d) Cross section after failure for sample with pad diameter of 100 µm on silicon chip

Fig. 9 Shear strength of solder cap depending on solder composition and pad diameter (solder volume) for pad diameters of (a) 30 µm and (b) 100 µm
as-received samples was generally significantly higher than that for aged samples, with Sn1.8Ag samples exhibiting values above 50 MPa compared to approximately 38 MPa for Sn0.9Ag samples. Lower values of shear strength for Sn2.4Ag samples may reflect the possibility of formation of primary Ag3Sn precipitates in these samples, thus decreasing the silver available for the fine secondary Ag3Sn precipitates (Fig. 5, 6). However, counts of numbers of secondary Ag3Sn precipitates in these samples were similar to those for Sn1.8Ag solder joints (Fig. 7). Values of the shear strength of as-reflowed, 100-µm-diameter copper pillar solder joints were distinctly lower than for the 30-µm-diameter copper pillar solder joints (Fig. 9); values were close to those of the aged solder joints. This was despite a similar spacing between Ag3Sn precipitates in both as-received 100 µm and 30 µm copper pillar SnAg solder joints.

Shear strength measurements were conducted for the copper pillars themselves (Fig. 4b), in an effort to examine the relative strength of the copper pillar and the aluminum pad/pillar bond. The results revealed the strength of the copper pillar/aluminum pad bond, because all failures were observed to be in the copper pillars (Fig. 10b). Values for the shear strength of copper pillars themselves were all similar in the as-fabricated state; shear strengths of 130 MPa were observed (Fig. 10a).

Accelerated thermal cycling between −40 and 125 °C was conducted to characterize the interconnect reliability of the copper pillar non-underfilled assemblies. Comparisons were made between the performance of silicon/high-CTE glass interposer assemblies and silicon/silicon interposer assemblies. These copper pillar assemblies had 50-µm-diameter copper pillars and Sn1.8Ag solder.

Failure of the copper pillar solder joints was observed to occur via crack propagation through a relatively thin solder layer remaining between intermetallic compounds after assembly and ATC testing (Fig. 11). Such a failure was similar to those observed in more conventional surface-mount geometries, such as chip-scale packages.[24] Similar results were found for both corner and chained end joints (Fig. 12).

These ATC results are presented in Fig. 12 in the form of two-parameter Weibull plots of cumulative percentage of failures (percent) versus number of cycles before failure. Fits to these datasets provided estimates of the shape parameter (slope), $\beta$ and characteristic lifetime (scale), and $\eta$ for each dataset. Lifetimes were more than an order of magnitude larger for the silicon/silicon assemblies than for the silicon/high-CTE interposer assemblies (Fig. 12).

**CONCLUSIONS**

In the current study, relations between processing,
microstructure, and reliability of assemblies enabled through copper pillar/interposer technology were examined. Both silicon/micro-copper pillar/solder cap/glass and silicon/micro-copper pillar/solder cap/silicon assemblies with a large number of I/Os were examined in a configuration that allowed monitoring of electrical continuity during test. Significant variation in Ag₃Sn precipitate morphology was observed under nominally identical fabrication conditions. These were correlated with relatively large variations in mechanical behavior, for example, in measured values of shear strength. Large variations in Ag₃Sn precipitate size and number were also observed with changes in composition and upon aging, as would be expected. Copper pillar assemblies revealed small but continuous solder layers. After failure during ATC, cracks were found to have propagated through these continuous solder layers. Even though the silicon-to-silicon joints had no CTE mismatch, there were still solder fails. Thus, underfill is recommended for all structures; both silicon-silicon and silicon-glass will benefit.

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REFERENCES

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NOTEWORTHY NEWS

2018 IRPS CONFERENCE

The IEEE International Reliability Physics Symposium’s (IRPS) annual conference will be held March 11 to 15, 2018, at the Hyatt Regency Airport in South San Francisco, Calif.

The IRPS technical program includes technical sessions, keynote and invited talks on emerging issues, tutorials, workshops, an evening poster session, a year-in-review seminar, panel discussions, and equipment demonstrations. Special attention is given to the reliability of advanced CMOS scaling, new materials introduction, new processes or integration strategies, and/or fundamentally new device architectures. Attendees returning from the IRPS will be better equipped to solve critical reliability problems and develop effective qualification procedures that affect their companies’ bottom line.

The IRPS Conference is sponsored by the IEEE Reliability Society and IEEE Electron Device Society. For more information, visit the IRPS website at irps.org.
**DC/DC CONVERTER FAILS TO START UP WITHOUT OVERSHOOT DUE TO INTERACTION WITH INRUSH CURRENT SUPPRESSION CIRCUITRY**

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**INTRODUCTION**

A chip may suffer failure due to voltage stress, current stress, temperature stress, mechanical stress, and so on. DC/DC converters work in a control loop to convert the output error signal into a variable duty cycle of the driving signal for the switching element. At start-up, the error amplifier works in an unbalanced state and the pulse width modulation works at 100% duty cycle, thus causing an output overshoot voltage and high input inrush current.[1] The DC/DC converter’s start-up overshoot voltage will impose a voltage stress on its load chip through the chip’s supply voltage pin and is handled by the power supply designer. So far, a great deal of attention has been given to suppressing start-up overshoot voltage. To achieve this, a soft-start circuit is required. The two most common methods are to adopt an external soft-start capacitor or soft-start capacitor-based circuit and an on-chip digital soft-start circuit.[2-4] Generally, there is no start-up overshoot in a DC/DC converter.

However, there is an amazingly high input inrush current when an electromagnetic interference (EMI) filter is applied. This high inrush current mainly involves charging of input capacitors. As shown by the literature,[5] if the power is applied as a step with a rise time of 1 µs or less, the initial inrush current can be 50 A or more on an unlimited power bus. This could occur if power is applied with a switch, such as a relay, on the power bus, leading to possible damage to the power bus and the switch. In a high-reliability space application, inrush current suppression circuitry (ICSC) is important and necessary to suppress the inrush current to a reasonable limit at start-up. The inrush current decreases as the working time of the ICSC increases. The typical specification for ICSC’s working time is not more than 5 ms. The start-up delay time of some DC/DC converters plus the start-up time is generally less than 2 ms, shorter than the working time of the ICSC. The transient response performance of DC/DC converters is limited, with transient response recovery time generally 300 µs.

There may still be a start-up overshoot voltage when a DC/DC converter without start-up overshoot itself is applied with ICSC, if the converter does not match its ICSC. The amplitude and duration of the overshoot voltage varies significantly with the respective performance of the DC/DC converter and ICSC. This start-up overshoot voltage also imposes a voltage stress to the DC/DC converter’s load chip and even causes chip failure, which was confirmed by a professional reliability research and analysis institute, thus degrading or damaging the entire electronic system.

This article explores why a DC/DC converter without start-up overshoot itself fails to work normally, how the start-up overshoot voltage occurs, but not how the start-up overshoot voltage stress leads to chip failure. Solutions are also given in this article.

**INTERACTION OF DC/DC CONVERTER WITH ICSC**

In Chinese space electronic systems, ICSC is required to suppress the input inrush current. ICSC is used as a series-limiting resistive element in either the positive or return supply line between the input point and the capacitors, through which the input capacitors are charged when the power bus is applied to the converter. Thus, the input inrush current is limited to a reasonable value. ICSC is always conducted in one of three methods: resistor, negative temperature coefficient thermistor, and active circuit. Active ICSC is based on either an n-channel MOSFET in the return supply line or a p-channel MOSFET.
in the positive supply line. The most common and basic ICSC in Chinese space electronic systems is shown in Fig. 1. It is an n-channel enhancement MOSFET-based ICSC and is used as an illustration to simplify the analysis. MOSFET Q1’s DC input resistance is extremely high. When the power bus $V_{in}$ is applied through a switch S1, due to C1, $V_1$ increases from 0 V to $R_2 V_{in}$, with a duration $T_{tr}$ of several milliseconds. The relationship of $V_1$, $t$, and $V_{in}$ can be written as $V_1 = \frac{R_2}{R_1+R_2} V_{in} + \frac{1}{C_1} R_1 R_2^2 V_{in} + \frac{R_2}{R_1+R_2} R_2 V_{in}$ is more than the gate threshold voltage of MOSFET Q1. R3 is low, aimed to damp the ringing of C1 and the gate inductance. $V_2$ is almost equal to $V_1$, and thus $V_2$ increases from 0 V to $R_2 V_{in}$, which is more than the gate threshold voltage of Q1, within this duration $T_{tr}$. Q1 turns on as $V_2$ increases to more than the gate threshold voltage. The equivalent circuit of drain-to-source for MOSFET Q1 is similar to a varistor. Drain-to-source resistance decreases from a million ohms to on-state resistance. Therefore, the input line voltage to the EMI filter and hybrid DC/DC converter $V_{inf}$ is ramped to almost $V_{in}$. $V_{inf}$ can be approximately calculated as $V_{inf} = k t$, where k is the ramp rate, and $t$ is time. Typical input line voltage rise time is 5 ms. With input line voltage ramped, the in-rush current is reduced to several amps, which is acceptable for spacecraft power bus.

However, some converters start up in a short time. The start-up delaying time, $T_d$, plus the start-up time, $T_s$, is on the order of milliseconds. The overall time is less than the working time, $T_{op(ICSC)}$, of the ICSC. That is:

$$T_d + T_s < T_{op(ICSC)}$$  (Eq 1)

Because all DC/DC converters can operate in a wide range of input voltage, when DC/DC converters are applied in the power system with an EMI filter and ICSC, they begin to work in their input line voltage ramp. At this time, a DC/DC converter’s input voltage is lower than the final input voltage. The DC/DC converter’s start-up delaying time plus start-up time is less than the working time, $T_{op(ICSC)}$, of the ICSC. After the DC/DC converter’s start-up, the DC/DC converter’s internal soft-start circuit will not limit its duty cycle, and its duty cycle is determined only by its internal control loop. Because the DC/DC converter’s input voltage is lower than the final in the input line voltage ramp, it works with the duty cycle more than the normal, perhaps maximum duty cycle. This working state will go on until the internal controlled closed loop regulates the output voltage again. The normal bandwidth of the controlled closed loop is several kilohertz, with regulating time on the order of milliseconds. During the input voltage ramp, the DC/DC converter’s duty cycle should decrease to the corresponding value in time. However, under the milliseconds regulating time limit, the closed loop cannot decrease the duty cycle in time, and thus the overshoot occurs.

In a switching DC/DC converter, neglecting the switch device’s on-state voltage drop and the rectifier’s forward voltage drop, the relationship of input voltage ($V_{in}$), primary winding turns ($N_p$), secondary winding turns ($N_s$), duty cycle (D), and output voltage ($V_o$) is:

$$V_o = V_{in} \times \frac{N_s}{N_p} \times D$$  (Eq 2)

From Eq 2, if the duty cycle, D, cannot decrease in time as the input voltage, $V_{in}$, increases, the output voltage, $V_o$, will increase. If it occurs at start-up, it is just start-up overshoot. If the controlled loop’s regulating time, $T_{reg}$, is lower than the ICSC’s working time, $T_{op(ICSC)}$, minus the DC/DC converter’s start-up delaying time, $T_d$, and start-up time, $T_s$, the overshoot voltage, OV(%), can be approximately calculated as:

$$T_{reg} < T_{op(ICSC)} - T_d - T_s$$  (Eq 3)

$$OV(\%) = \frac{T_{reg}}{T_{op(ICSC)}} \times 100\%$$  (Eq 4)
SOLUTIONS

From the analysis above, to cope with start-up overshoot, many techniques can be adopted, such as shortening the working time of the ICSC, increasing the start-up delay time, increasing the start-up time, and improving the transient response performance. Shortening the working time of the ICSC will lead to high input inrush current. Limited by the DC/DC converter’s output LC filter and error amplifier, the bandwidth of the controlled closed loop cannot be improved significantly, meaning that the transient response performance cannot be improved sharply. This article advises increasing the start-up delay time, \( T_d \), and increasing the start-up time, \( T_s \), to solve start-up overshoot. For packed hybrid DC/DC converters, increasing the start-up time cannot be done except by decapsulating the converter to revise the internal circuit. Adding an external start-up delay circuitry is one of the choices. Figure 2 shows one circuit design. It applies to the converter that cannot work if its inhibit pin is connected to the input return line. It sacrifices input voltage range to increase start-up delay time. Without this circuit, the DC/DC converter starts up at \( V_{in1} \). With this circuit, it starts...
up at $V_{in2}^*$ and $V_{in1} < V_{in2}$. The external start-up delay time consists of input ramp line voltage time from $V_{in1}$ to $V_{in2}$ and charging time of the capacitor C4. Parameters of this circuitry vary significantly for different manufacturers’ DC/DC converters.

**EXPERIMENTAL RESULTS**

This start-up overshoot is verified in a 5 V rated output hybrid DC/DC converter application circuit. The hybrid DC/DC converter’s start-up waveform without EMI filter or ICSC is shown in Fig. 3. There is no start-up overshoot voltage for the DC/DC converter alone, as stated before. The start-up delay time, $T_d$, is approximately 220 µs, and the start-up time, $T_s$, is approximately 300 µs. Start-up delay time, $T_d$, plus start-up time, $T_s$, is 520 µs. As Fig. 4 shows, however, there is a start-up overshoot when this DC/DC converter is applied in the power system with an EMI filter and ICSC. The overshoot is 3.28 V, which is 65.6% of the rated output voltage. The converter’s load chip failed after start-up for more than 100 times. The working time of ICSC is approximately 3 ms, longer than time $T_d$ plus $T_s$. This article adopts the start-up overshoot suppression circuitry shown in Fig. 2. This start-up overshoot, which is shown in Fig. 5, is suppressed from 3.28 V to 87.5 mV, from 65.6 to 1.75%. Start-up delay time is increased to approximately 4 ms.

**SUMMARY**

When the external ICSC’s working time is longer than the DC/DC converters’ start-up delay time plus start-up time, a start-up overshoot is induced. This is because the DC/DC converter cannot decrease its duty cycle as the ramp input line voltage increases in time. By increasing the DC/DC converter’s start-up delay time, overshoot can be suppressed. A start-up delay circuit is proposed. Experimental results verified its feasibility for suppressing this start-up overshoot voltage.

**ACKNOWLEDGMENTS**

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**ABOUT THE AUTHOR**

Guo Xianxin is an electrical engineer for Chinese spacecraft. He has more than 6 years of switching power supply research and development experience. His research interests include low-voltage high-current DC/DC converters, pulse power supply, high-voltage low-current power supplies, and adjustable switching power supplies. Mr. Guo received a B.S. degree in electronic engineering from the China University of Mining and Technology in 2007 and an M.S. degree in power electronics from the China Academy of Space Technology in 2010. He is currently pursuing a Ph.D. degree in power electronics at the China Academy of Space Technology.
The International Symposium for Testing and Failure Analysis (ISTFA) concluded on November 9, 2017, in Pasadena, Calif. Thanks to the booming semiconductor industry and the value that failure analysis brings to the industry’s growth, ISTFA 2017 set records for attendance in recent years and the revenue generated for the Society. Including the Tutorials, Symposium, and Expo, there were a total of 859 attendees, which is an 8% growth over ISTFA 2016.

**ISTFA EXPO**

The ISTFA Expo has always been the exceptional venue for FA professionals to learn about the latest FA tools and services. The number of companies displaying their products and services at the Expo increased by 16% from 2016, to a total of 87 this year. Such double-digit growth suggests that the IC manufacturers are investing in new FA equipment, and the future of the FA industry is bright. Approximately 80% of the exhibitors who completed the survey also indicated that they are highly likely to return to the ISTFA 2018 Expo. Such commitment demonstrates the success of the 2017 Expo and the value that ISTFA brings to our suppliers.

**TECHNICAL PROGRAM**

The ISTFA Technical Program kicked off on Saturday, November 4, with two excellent perennial short courses, “Fault Isolation Techniques for Failure Analysis” and “Beam-Based Defect Localization,” taught by David Vallett (PeakSource Analytical) and Ed Cole (Sandia National Laboratories), respectively. The Tutorial Program on Sunday and Tuesday featured 5 new and 18 returning tutorials. The short courses and tutorials were organized by the Tutorial Committee, led by Mayue Xie (Intel) and Randal Mulder (Silicon Laboratories).

The ISTFA Keynote Presentation was given by Dr. Adam Steltzner (NASA’s Jet Propulsion Laboratories). In his captivating presentation, Dr. Steltzner discussed his inspiring story of leading the team that invented the “sky crane” landing system that landed the Mars Rover Curiosity on Mars in 2012, and NASA’s future plans for exploration of Mars. He also highlighted the importance of human curiosity, which drives all of us to innovate and explore.

Thanks to the hard work by Technical Program Chair Felix Beaudoin (GLOBALFOUNDRIES) and a team of 50 session chairs and 114 reviewers, the ISTFA 2017 Symposium featured 117 high-quality oral and poster presentations and three invited talks in two tracks. A new industry-specific session, titled “Space Application FA,” was introduced.

Patrick Pardy (Intel) and Baohua Niu (TSMC) organized three User Groups. One User Group was held on Wednesday evening, and two User Groups were held during the long lunch break on Thursday. The lunchtime User Groups were well attended, which is also consistent with 75% of ISTFA survey respondents’ preference for scheduling User Groups during lunch rather than at the end of the day. An outstanding Panel Discussion on the conference theme “Striving for 100% Success Rate” was organized by Panel Chairs Susan Li (Cypress Semiconductors) and Renee Parente (AMD). Don’t miss the ISTFA User Group and Panel Discussion summaries, which can be found online at asminternational.org/web/edfas/news/edfa under the link “Supplemental Reading 2017.”

**STUDENT PARTICIPATION**

Today’s students are the next generation of FA engineers. This year, the ISTFA 2017 Organizing Committee made a concerted effort to attract abstracts for Symposium
sessions from student authors. The abstracts were then subjected to the same rigorous blind review as any other abstract submitted to the conference. In the end, nine student papers were accepted to the conference Symposium and Poster sessions, which is a significant growth from previous years. For the first time, in recognition of their contributions, all student authors were awarded full conference registrations as scholarships.

THANKS TO VOLUNTEERS

ISFTA is made possible by numerous volunteers. In addition to the various chairs mentioned in previous sections, I would also like to thank Vice General Chair Efrat Moyal (LatticeGear), Past General Chair Martin Keim (Mentor, A Siemens Business), Expo Chair Becki Watt (Mentor, A Siemens Business), Audio/Visual Chairs David Grosjean (Butterfly Network) and Zhigang Song (GLOBALFOUNDRIES), Local Arrangements Chair Ryan Ross (Jet Propulsion Laboratories), Video Contest Chair Rose Ring (Kionix), Publicity Chair (Academia) Navid Asadi (University of Florida), and International Chairs Frank Altmann (Fraunhofer CAM) and Vinod Narang (AMD). Last but not least, a big thanks to ASM International staff Kathy Murray and Lindy Good for attending to numerous requests from the ISTFA volunteers, attendees, and vendors.

STRIVING FOR 100% SUCCESS

Based on the verbal and survey feedback received, I believe ISTFA 2017 met or exceeded the expectations of most attendees. Of course, there are also things that can be improved. The ISTFA 2018 Organizing Committee has received your conference survey feedback and is reviewing it carefully. If you have additional comments, please feel free to contact me. We can work with the ISTFA 2018 Organizing Committee to achieve 100% success in every aspect of the conference.

JOIN US AT ISTFA 2018

ISTFA 2018 will be co-located with the International Test Conference on October 28 to November 1, 2018, in Phoenix, Ariz. Planning for the conference has already begun. The deadline for abstract submission is April 21, 2018. For more information, visit the ISTFA 2018 website at asminternational.org/web/istfa-2018.

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Ed Principe, Synchrotron Research Inc.

**ISTFA 2017 ATTENDEES’ BEST PAPER:**
“Characterization of Gate Oxide Pinhole Defect in NMOS FinFET Devices”
Liangshan Chen, GLOBALFOUNDRIES

**ISTFA 2017 BEST STUDENT PAPER:**
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Alexandra Fraczkiewicz, University Grenoble Alpes; CEA, LETI, MINATEC Campus

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Elham Amini, Technical University of Berlin

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**EDFAS 2017 PHOTO CONTEST WINNERS**

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3rd  Tammy Berger, Naval Surface Warfare Center

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2nd  Bence Hevesi, Robert Bosch Kft.
3rd  Nathan Wang, Maxim Integrated

**Category III: False Color Images**
1st  Wentao Qin, ON Semiconductor
2nd  Ian Kearney, Mark Dipsey, and Bruce Gillette, Texas Instruments

All winners received a recognition plaque or certificate and a one-year EDFAS membership. The winning entries will be featured on the cover of this magazine during 2018. They also may be viewed on the EDFAS website.

**EDFAS 2017 VIDEO CONTEST WINNERS**

**Congratulations to the following winners:**

First Place: “Electromigration Station” by Stephen T. Fasolino, Raytheon
Second Place: “A Foil Odyssey” by Terry Stark, Qorvo

The first-place winner received a $150 gift card and an award certificate. The second-place winner received a $100 gift card and an award certificate. The winning entries may be viewed on the ISTFA 2018 website.

**ISTFA 2017 PANEL DISCUSSION AND USER GROUPS SUMMARIES**

Summaries of the ISTFA 2017 Panel Discussion and the User Groups can be found online at asminternational.org/web/edfas/news/edfa. These reports are included in the digital edition of the magazine and can also be accessed by clicking on the link shown under the portal “Supplemental Reading 2017” on the EDFA webpage.
CALL FOR PAPERS

SUBMIT AT ISTFA.ORG
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Share your experiences and advance the industry and your career at the 44th International Symposium for Testing and Failure Analysis, the premier event for the microelectronics failure analysis community. We invite you to submit your work for publication and to present to the industry in Phoenix, Arizona, for the 44th year of ISTFA.

TOPICS INCLUDE:

- Emerging FA Techniques and Concepts
- Future Challenges of FA
- Fault Isolation (Thermal, Lock-in thermography, static and dynamic laser stimulation, static and dynamic emission microscopy, Laser Voltage Probing and imaging ...)
- 3D devices Failure Analysis (stacked dies, TSV ...)
- FA Techniques Addressing the Challenges of Heterogeneous Systems in Package
- Organic Electronic (OLED ...)
- Wireless, Self-Powered, Sensors, MEMS Failure Analysis
- Detecting Counterfeit Microelectronics
- Alternative Energy (Photovoltaics, Solid State Lighting, etc ...)
- FA Process
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- Diagnostic Testing, Scanning and Debug
- Board and System Level FA
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- Electronic Device Materials Characterization (SIMS, RBS, XPS, Auger, etc ...)
- Microscopy (SEM, TEM, FIB, etc.)
- Circuit Edit (Laser, FIB, etc.)
- Sample Preparation and Device Deprocessing
- Scanning Probe Analysis
- Yield and Reliability Enhancement
- Nanoprobing, Electrical Characterization
- Competitive Analysis and Reverse Engineering
- FA use cases
A SUMMARY OF THE ISTFA 2017 PANEL DISCUSSION: STRIVING FOR 100% SUCCESS RATE

Susan X. Li* and Renee Parente,** ISTFA 2017 Panel Discussion Organizers
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** Advanced Micro Devices, Austin, Texas — renee.parente@amd.com

D uring ISTFA 2017, we successfully hosted a Panel Discussion on the topic of “Striving for 100% Success Rate.” The failure analysis (FA) community knows that achieving 100% success rate is the ultimate goal for FA operations, and it holds particular importance for industries, such as automotive, aerospace, and oil companies, beyond the traditional semiconductor chipmakers. Five area experts among these industries shared their views on our panel regarding what “100% success rate” means to their organization, what challenges they encounter when working toward this goal, and the experiences they have in their daily work when operating toward this goal.

Dr. David Su, a director of the FA group at TSMC, Taiwan, began the Panel Discussion. David shared with the audience his belief that every sample is important, because finding the cause for failures is critical for fab process improvement. In the wafer fab foundry, a challenge can be the lack of sufficient product knowledge; therefore, it is particularly important to have strong partnerships with requesters in order to make the FA successful for root-cause finding. David emphasized the importance of a strong, experienced, expert team that is disciplined yet thinks outside the box and is fast but meticulous. He also cautioned that quickly finding a physical defect could lead to early, misguided satisfaction in the FA process, so be sure the analysis continues until the true root cause of the issue is found.

Our second presenter, Mr. Dan Bodoh, a technical director in the Product Diagnostic Center at NXP, focused mainly on electrical FA and fault isolation for new product introduction (NPI). Dan indicated the importance of having a definition of “failure analysis success.” NXP uses three criteria for successful FA: (1) conclusive evidence that connects electrical behaviors to a physical defect, or (2) a fingerprint or a signature is already agreed upon, or (3), for early NPI debug, significant contribution to the product and design team’s understanding of an issue. Dan shared the belief that FA leadership has a responsibility to keep an eye on the processes in the lab, because it is okay to make a mistake, but patterns of mistakes must be investigated, as it is critical to learn from them. He also encouraged holding “challenging analysis meetings” to brainstorm with the team, and building a team led by experienced people not bound by the daily cycle-time pressure but empowered to help the team have better productivity and quality daily analysis work.

Unlike the first two speakers from the traditional semiconductor wafer fab and chipmakers, our next three invited speakers were from companies in special application areas.

Dr. Oliver Senftleben, a senior technical expert from Audi Semiconductor Lab in Germany, shined light on the automakers’ perspective of 100% FA success rate. For automakers, 100% success rate is a requirement, not a strategic goal. On average, there are 6000 to 8000 semiconductors in each car; therefore, a 1 ppm random failure rate means 10,000 to 15,000 defects in car components, based on yearly production volume for Audi. A 100% success rate is imperative for qualification failures, because findings impact new vehicle project releases. A typical qualification sample size is six devices; thus, failures could likely imply systematic issues. Rapid determination of countermeasures, even based just on the failure symptoms, is critical for 0 km failures, because potential systematic failures are pushed into the field every 80 s per production line. Quick root-cause identification of field failures is a priority, because systematic and epidemic failures lead to high warranty costs and
This year we had six presentations that covered a wide range of topics, including:

- Three papers that featured alternate (non-gallium) ion beams
- A methodology for evaluating the relative merits of competing FIB platforms
- A guide for deciding which backside edit sample-preparation method to select
- Planar FIB deprocessing from the backside and frontside
- A sub-pico-amp FinFET edit example using the latest gallium circuit edit platform

In one room to work through issues. This good team work and broad knowledge base, along with strictly following process flows, improves the success rate and preserves the integrity of aerospace industry investigations.

After looking up to the sky, we finalized our Panel Discussion with a look at what 100% success rate means to the oil industry. Mr. John Bescup, an electrical engineer with Weatherford in Houston, Texas, spoke about electronic devices used for “logging while drilling” that collect useful real-time data to assist the drilling engineers in finding oil reservoirs. The printed circuit boards and components used must meet high reliability standards and function at high-temperature conditions in harsh vibration environments. Failures on electronic components can cause costly downtime during the drilling operation, so a high success rate on FA is vital for the success of drilling service companies in the oil industry. Commonly seen failures are often related to package issues exacerbated by the harsh underground environment, so a broad knowledge base of metallurgy, chemistry, mechanical engineering, and electrical engineering is vital for FA success.

Throughout the Panel Discussion, the audience engaged with each panelist by asking numerous questions, and the discussion was a pronounced learning opportunity for those involved. We all are striving toward 100% success rate in our daily lives, and this Panel Discussion provided a little more knowledge and advice on how we can achieve it.
Demonstrated tests included 1.8 nm resolution at 10 kV/1 pA, low invasiveness in a chip edit simulation, excellent imaging and nanomachining control, and ultrafast secondary ion mass spectrometry (SIMS) acquisition.

Sharang, from Tescan Orsay, presented the second talk, “Delaying Capabilities Using Xe Plasma FIB and Associated In Situ Nanoprobing Operations.” He began by showing impressive delayering results from the M4 metal layer down to gates over a 40 × 40 µm area on a popular 14 nm FinFET processor product. The resulting surface roughness, as measured by atomic force microscopy technology, was very low, which enabled easy in situ nanoprobing at the individual FinFET transistor level. Results were shown from an eight-tip stage-mounted prober assembly and even an in situ atomic force probe.

However, being able to plasma-FIB deprocess the upper levels (thick, wide, and not necessarily fully planarized) would normally require starting with highly inexact mechanical parallel polishing. The trick shown was to begin the process on flip-chip module-mounted dice, as though it was the start of an FIB chip edit. Sharang began with ultrathin CNC contour milling followed by XeF₂ clearing of all remaining silicon to the underside of the fin mandrel and shallow trench isolation regions. Planar deprocessing then proceeded, using a proprietary gas and Xe⁺ beam process through the thin lower interconnects and into the thicker layers from the bottom side upward.

Michael DiBattista from Varioscale presented “A Decision Tree for FIB Sample-Preparation Strategy.” The idea for this talk came from a lunchtime discussion some months ago about all the possible options available to those engaged in FIB chip circuit edit. Depending on the tools at one’s disposal, time issues, edit-site peculiarities or the need to do multiple edits, and customer requirements (system use or test with or without probing), one may have either a clear choice or multiple possible paths. These include, but are not limited to, localized or wide-area partial or full-thickness silicon trenching (laser chemical etching, plasma FIB, or FIB XeF₂) or mechanical prethinning (localized pocket, moderate thickness remaining with or without contour following, or ultrathin silicon remaining). The need for good end-pointing and various methods were explored. From the “nuclear option” to ultrathinning, Mike stepped through each scenario and suggested the best toolset to use to achieve individual sample-prep needs.

Valery Ray of PBS&T, MEO Engineering/University of Connecticut, presented the fourth paper, “Quantifiable Comparative Evaluation of FIB/SEM Instruments.” Valery discussed the need to design quantifiable evaluation tests for FIB systems, noting that “canned” demos are designed to exploit the best features of a given tool but not necessarily show the full picture of the tool. He showed examples of standardized samples and a number of qualification tests, including beam burns, current versus dose, drift tests, patterning performance tests, and imaging tests. He also suggested some customized combination tests that will emulate specific-use cases. Being prepared with one’s own evaluation suite that can be performed on all FIB platforms under consideration will help end-users make the best tool-purchasing decision.

The fifth paper, “Sub-Pico-Amp Focused Ion Beam (FIB) for Circuit Edit on FinFET Technology,” was given by Hideo Tanaka from FEI/Thermo Fisher Scientific. Hideo’s talk explored the challenges that are arising from shrinking process nodes that accompany the adoption of FinFET technology. He stressed that a circuit edit solution which includes sub-pA beam currents, precision milling, and optimized gas and recipes must be precise. Critical for meeting today’s chip edit challenges is an improved secondary-electron detector to be able to image the scant amount of signal for end-pointing and so on. He showed a case study of circuit edit work with emphasis on the key elements required to enable a successful, functional modification.

The sixth and final paper of the workshop session, “Neon GFIS-Induced Chemical-Assisted Etch and Beam-Induced Deposition Characterization,” was presented by Rick Livengood of Intel. The first part of Rick’s talk included a review of neon gas field ion source (GFIS) technology and how it has been used for nanopatterning, surface analysis, transmission electron microscopy prep, and early circuit edit attempts. He noted that some of the key attributes to GFIS technology are that neon generates two to three times the secondary electron yield relative to gallium, and also, the sputter yield is half of gallium. That provides more reaction time along with better visual and instrumentation end-pointing.

The second segment included an update of recent experimental results comparing neon via sputtering versus gas-assisted neon etching, and deposition of oxides and metals using neon as the primary beam. Much of the work was done using a new gas system from Xidex that features dual opposing XeF₂ gas nozzles along with nozzles for an oxide source (PMCTS and oxygen). Overall, neon appears to address some of the limitations presented by gallium for chip edit and will be a good complement as a dual-column system for use on sub-10-nm process nodes.
In a marked change from previous ISTFA events, the FIB User Group meeting was held concurrently with the Contactless and Nanoprobing User Group during the two-hour lunch break on Thursday, November 9. Despite some concern, the “lunch and learn” experiment seemed to work. Overall attendance was up from last year, and audience participation was strong after each paper and during the panel discussion at the end. A peak attendance of 97 was recorded just before 1 p.m. The organizers also wish to thank Thermo Fisher Scientific for their sponsorship of the event.

ISTFA 2017 CONTACTLESS OPTICAL/NANOPROBING
EFA USER GROUP

Moderators: Dan Bockelman, Intel Corp.; Sweta Pendyala, GLOBALFOUNDRIES; and Nebojsa Jankovic, NXP Semiconductors
dan.bockelman@intel.com, sweta.pendyala@globalfoundries.com, nebojsa.jankovic@nxp.com

Dr. Daminda Dahanayaka (GLOBALFOUNDRIES, Essex Junction, Vt.) gave the first presentation, “Challenges of FEOL Sample Preparation for Nanoprobing of Advanced Nodes.” The goals in sample prep are good edge definition of conductors, protection of underlying structures, and good surface electrical conductivity for probe contacting. Because scaling reduces line widths as well as film thicknesses, specialized sample preparations for both scanning electron microscopy (SEM)- and atomic force microscopy (AFM)-based probes are required. First, the IC is delayered down to the layer of interest. Next, topographical relief of the contacts is performed 2 nm below the surface with a diamond slurry. Colloid slurry relief is not sufficient for AFM probes but is sufficient for SEM nanoprobing. An alternative to diamond slurry is HF reactive ion etch (CF4, CHF3, CH2F2, etc.). The HF yields poor images, and CF4 etches SiN faster than SiO2, but C-F leaves polymer deposits. Finally, a third alternative is ion milling (argon, N2, O2). The N2 etches a little faster than argon or O2. Overall, this presentation emphasized how important sample prep has become as devices have continued to scale aggressively.

The second presentation, “Recent Advances in Nanoprobing,” was given by Dr. Martin Von Hartman (Intel, Hillsboro, Ore.). The presentation discussed nPIII upgrades compared with the nPII system. The xProber using the Zeiss SEM is the precursor to the nPIII, which uses a substage. Faster nanoprobing is needed, especially for future technologies. Intel has seen increased demand for nanoprobing year after year, which is more than was anticipated. Essential capabilities of a nanoprober are minimal drift; maximum time on contact; SEM image quality; quality probe tips; good sample prep; automation; capability to detect opens, shorts, resistive shorts, and so on; and minimal e-beam invasiveness. Primary benefits of the nPIII system are 50% reduced beam current from nPII, a lower working distance of less than 4 mm, and greater than 10 min time on contact. Pulse probing was aimed at finding resistive gate failures, but it is too slow and not done routinely in the Intel labs. There is need for an alternating current test to investigate gate resistance, but it must be fast. It can take hours to set up for pulse probing.

The third presentation, “Advantages of Electrical Optical Voltage Probing (EOP) Using a Digitizer,” was given by Brett Adler (Hamamatsu, San Jose, Calif.). Sampling long-duration test loops enables detectability of timing behavior not possible with an oscilloscope. The technique uses a continuous-wave laser. Carrier concentrations under the transistor gate result in reflection changes as the transistor switches, and the changes are felt in the reflected beam. The reflected beam is sampled through the use of a detector, and the waveform information is derived. It allows zooming into any fast glitch in a waveform. The EOP mapping combined with a digitizer works well for SRAMs. These enable new analysis with 31.25 ps resolution. The technique uses up to four Giga-samples per second, and 500,000 points can be sampled at 250 ps resolution.

The fourth presentation, “Fault Localization—LTP Technique Using High-Speed Digitizer versus Oscilloscope,” was presented by Dr. Mike Bruce (Semicaps). Laser timing probe (LTP) measurements have been limited by the acquisition speed of oscilloscopes. Three spectrum analyzers have been used in parallel, due to the triggers in short test loops.
This is overcome with a high-speed digitizer capturing all the triggers for a short-loop acquisition time improvement of more than 50×, even up to 500× faster than a LeCroy oscilloscope. A 2 GHz bandwidth digitizer is 12 bits. For slow loops, high-bandwidth oscilloscopes are noisy. The digitizer allows for logic analysis in real-time, and binary searches are supported.

The fifth presentation, “Visible versus IR for Laser Probing,” was given by Neel Leslie (Thermo Fisher Scientific, Fremont, Calif.). Laser voltage probing and laser voltage imaging directly expose electrical functionality of an IC or cell. The interplay between optical spatial resolution (inversely proportional to wavelength) and transmission through the silicon has necessitated near-infrared wavelengths (1064 to 1340 nm). Visible light probing has shown improved resolution (1320 to 785 nm, resolution improves 40%); however, trade-offs exist with laser invasiveness and silicon thinning. To use the technique, silicon must be thinned below 10 µm. However, the impact of laser invasiveness on the measurements is still a question, but it can be reduced by lower laser power, less than 2 mW. At 5 µm silicon thickness, the transmission is 60%.

The final presentation, “Techniques for Successful Backend-of-Line Nanoprobing,” was given by Weston Hearne (Thermo Fisher Scientific, Richardson, Texas). Electron beam induced resistance change (EBIRCH) and electron beam absorbed current (EBAC) for back-end-of-line (BEOL) fault localization have become significant use cases for nanopробing. Fifty percent of nanopробing is for BEOL EBAC/EBIRCH, but frontside EBAC/EBIRCH accounts for 90% and backside EBAC/EBIRCH for 10%. With EBAC, nets remain intact.

This year the Contactless Fault Isolation and Nanoprobing User Groups were combined into a single User Group meeting. The User Group had six presentations focusing on topics in both contactless optical probing and nanopробing areas. All presentations were well received, with follow-on discussions and questions and answers during and after each presentation. Each of the presentations showcased innovations in the contactless probing and nanopробing areas and showed how the industry is moving forward to meet the challenges of semiconductor failure analysis today. More than 50 people attended the User Group meeting, and we look forward to a great 2018 User Group meeting as well. The organizers wish to thank Semicaps for their sponsorship of the session.

ISTFA 2017 SAMPLE-PREP/3-D PACKAGE-PREP USER GROUP

Moderators: Nathan Bakken, Intel Corp., and Tim Hazeldine, ULTRA TEC
nathan.j.bakken@intel.com, tim@ultratecusa.com

The Sample-Prep User Group, sponsored by Varioscale, Inc., hosted four technical presentations toward the development of new capabilities in the laboratory. The first presentation discussed ultra-flat repackaging as an alternative strategy to address the increasing complexity of coefficient of thermal expansion mismatch and other packaging-induced strains. The next two presentations addressed case studies where alternative deprocessing techniques were successful for particular current and proposed applications. The final presentation reviewed workflows to assemble or reassemble multiple chip packages to enable physical debug workflows. The session was concluded by an interactive discussion where the audience engaged to publish an answer to the question: “What are the greatest challenges facing 3-D IC package and sample-preparation technologists until 2022?”

“Rapid Repackaging of Die for Backside Physical Failure Analysis” was presented by Scott Silverman of Varioscale, Inc. The presentation noted the benefits of backside silicon deprocessing methodology that are becoming increasingly threatened by a packaging roadmap that continues to include thinner and less rigid substrate materials. In addition to more complex shapes caused by the package roadmap, the requirement for thinner silicon found in Z-height constrained applications or to reduce backside absorption also benefits from highly planar samples. A video was provided to show the implementation of an electrically or optically initiated foil soldering solution that has been successful in preventing thermal damage and was used to achieve surface flatness after mounting in the sub-100-nm range for an ~8 mm × 8 mm die. Also discussed was the selection of carrier materials to potentially
include depleted uranium in cases where ultimate stiffness is desired. The question-and-answer session addressed the minimum machining radii achievable for pocket mounting using milling tools, and an extension below 50 µm radii enabled with laser machining techniques.

“Thin, Smooth, and Curvy—The Confessions of a Sample-Prep Specialist” was presented by Jim Colvin of FA Instruments, Inc. Jim addressed the need for increasing controlled sample preparation across complex devices that is driven both by new failure analysis methodologies as well as increased tolerances for other testing requirements. He reviewed selected cases where successful processes occurred. Data showing the “orange-peel” effect as a function of temperature were reviewed, and it was demonstrated that mitigation could occur as the temperature was increased from 20 to 80 ºC within the detection limits of backside optical microscope inspection. The orange-peel effect was interpreted as the residual Z-strain resulting from the C4 attach process, which is particularly easily observed when remaining silicon thickness is below 5 µm. Some applications for capacitive and resistive endpointing mechanisms were highlighted, and the potential direction for in situ “probing while sample preparing” methodology was also shared. The audience initiated some discussion on the observable-by-eye color change that occurs when silicon is thinned to single-digit remaining thickness, with disagreement as to whether this observation could lead to development of simpler thickness metrology methodologies.

“Effective Microwave-Induced Plasma Decapsulation for Advanced IC Packages” was presented by Erik Jordan of Nisene Technology Group. The discussion focused on limitations due to extended throughput time or incompatibility with emerging materials systems facing traditional reactive ion etching processes. Also presented was the potential for application of microwave-induced plasma deprocessing to include oxygen, argon, carbon tetrafluoride, or other process gases as a solution to the decapsulation requirements roadmap. Examples from copper/palladium bonds that are highly reactive to wet deprocessing were reviewed in addition to examples demonstrating the deprocessing workflows for emerging silver bonding materials systems.

“Wire Bond Connected High-Bandwidth Memory Attatch on 3-D Stacked Die for Physical Debug Sample Prep” was presented by Nathan Bakken on behalf of Charles Ladwig, both of Intel Corporation. Heterogeneous integration of multiple dice at the package level was shown to be an increasingly common and threatening trend for physical debug techniques that traditionally rely on direct access to the backside silicon substrate. When dice are stacked or keep-out-zones required for physical debug techniques are otherwise infringed upon, it was proposed that an opportunity to reassemble die components in an orientation or workflow order suitable for debug could be pursued. Case studies were reviewed, including die reattach post-circuit-edit workflow as well as direct-to-die attach of LPDDR4 to enable optical probing of the base die in a package-on-package configuration where access to memory channels was a requirement for the fault isolation workflow.

Following the presenter topics, the moderators enabled a round-robin discussion of the five-year challenges forecasted for the sample-prep and 3-D package community. The audience participated by alternating between descriptions of future challenges and the relative magnitude of these challenges, with results tabulated and debated in real-time. As a result of a few dozen inputs from a variety of industry experts, seven challenges were identified for sample-prep and 3-D packaging technologists over the next five years:

- Absence of a roadmap consortium
- Proliferation of manufacturable processes out of the research and development lab
- Reduction of the quantity of and artistry required for process steps
- Attracting the next generation of engineering talent
- Getting support from design-for-test partners
- Reducing invasiveness
- Enabling budgets

The session successfully generated discussion and knowledge-sharing for over 75 people in attendance.
Driving activities in professional societies is not easy, given the frequent corporate mandate allowing society participation only if “it doesn’t interfere with your real work.” Nonetheless, some EDFAS members accept the challenge with a passion to learn, to contribute, and to make a difference for themselves as well as others. Former EDFAS President Jerry Walraven implemented the EDFAS awards to recognize these individuals, and, as Chair of the 2017-2018 EDFAS Awards and Nominations Committee, I am pleased to highlight our first award winners.

The **EDFAS Lifetime Achievement Award** recognizes those who have given their time, knowledge, and abilities toward the advancement of the electronic device failure analysis industry. Our first awardee, Dick Ross, a former IBM technical guru and manager, is a founding member and the second President of EDFAS. Dick wrote the operating procedures for ISTFA and EDFAS and provided insights into fundamental industry challenges, along with the necessary means/resources to implement their resolution.

Dick was the editor for the *Microelectronic Failure Analysis Desk Reference*, served in numerous EDFAS executive and ISTFA leadership positions for well over a decade, and delivered a highly popular tutorial on failure analysis lab management for many years. As ISTFA’s 2001 General Chair, Dick managed a deluge of last-minute speaker withdrawals and participant cancellations resulting from 9/11. He never imagined he would be compiling an opening speech that addressed a mass casualty. Dick adeptly faced the challenge in a way that is memorable to this day. In 2007, Dick stepped in to guide the recovery plan when both the EDFAS President and Vice President resigned simultaneously due to changes in professional and personal circumstances. Through the height and crash of the internet bubble and the failure analysis challenges introduced by copper low-k technology, Dick somehow...
managed consistent contributions to EDFAS and the industry while still getting his “real work” done at IBM. We all owe Dick a huge thank you for his lasting contributions.

The **EDFAS President’s Award** recognizes those who provided an exceptional amount of effort in their service to the Society. Our first recipient, Steve Herschbein, is a long-standing leader and technical contributor to the ISTFA FIB community, starting in 1998 when he received the Outstanding Paper Award for FIB chip edits of copper interconnects.

Steve chaired or co-chaired the FIB User Group meetings and Panel sessions for many years and also reviewed and mentored papers in the Technical Conference. Steve’s FIB tutorial at ISTFA has been presented annually and continuously since 2005. Steve is well recognized by his peers not only for his technical expertise but also his willingness to share his knowledge and opinion.

Please join me in thanking Dick and Steve for their significant contributions in driving industry advancements and enabling a strong conference and Society. To continue the recognition of worthy contributors, I urge you to send suggestions for the next award winners to cheryl.hartfield@zeiss.com. To learn more, visit asminternational.org/web/edfas/societyawards.

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**2018 EDFAS AWARDS**

**SEEKING NOMINATIONS FOR NEW EDFAS AWARDS**

EDFAS is seeking nominations for two awards to recognize the accomplishments of its members. The EDFAS Lifetime Achievement Award and the EDFAS President’s Award are given annually, with the first presentations made at ISTFA 2017. Nominate a worthy colleague today!

**EDFAS LIFETIME ACHIEVEMENT AWARD**

The EDFAS Lifetime Achievement Award was established by the EDFAS Board of Directors to recognize leaders in the EDFAS community who have devoted their time, knowledge, and abilities to the advancement of the electronic device failure analysis industry.

**EDFAS PRESIDENT’S AWARD**

The EDFAS President’s Award shall recognize exceptional service to EDFAS and the electronic device failure analysis community. Examples of such service include but are not limited to committee service, service on the Board of Directors, organization of conferences or symposia, development of education courses, and student and general public outreach. While any member of EDFAS is expected to further the Society’s goals through service, this award shall recognize those who provided an exceptional amount of effort in their service to the Society.

Nomination deadline for both awards is **March 1, 2018**. To learn more, visit asminternational.org/web/edfas/societyawards.
EDFAS MEMBER NAMED ASM FELLOW

The Electronic Device Failure Analysis Society (EDFAS) is proud to announce that member Cheryl Hartfield was named to ASM International’s 2017 Class of Fellows. In 1969, ASM established the Fellow of the Society honor to provide recognition to members for their distinguished contributions to materials science and engineering and to develop a broad-based forum of technical and professional leaders to serve as advisors to the Society. This year’s awards were presented at ASM’s annual Awards Dinner on October 10, 2017, in Pittsburgh, Pa., during Materials Science & Technology 2017.

Cheryl Hartfield, FASM, Solutions Manager, Zeiss, Pleasanton, Calif., was recognized “for sustained technical innovation and outstanding leadership in defect analysis and characterization methods that enabled the advancement of next-generation semiconductor devices with multiple industry applications.”


EDFAS MEMBER ON ASM BOARD OF TRUSTEES

Dr. Thomas M. Moore, FASM and President of Waviks, Inc., was elected to the ASM International Board of Trustees at ASM’s Annual Business Meeting on October 9, 2017, in Pittsburgh, Pa., during Materials Science & Technology 2017. His term runs from 2017 to 2020.

Tom has a long history of involvement with EDFAS and ISTFA, where he has published, presented, and served on various committees since 1989, including ISTFA General Chair in 2003. He co-authored a chapter on acoustic microscopy of semiconductor packages for the Microelectronics Failure Analysis Desk Reference, has published more than 90 technical papers and chapters, and holds over 20 patents. Tom served on the EDFAS Board of Directors from 2005 to 2014 and was EDFAS President from 2010 to 2011. He became an ASM Fellow in 2015.

EDFAS congratulates Tom on his election to the ASM Board of Trustees.
The EDFAS Board of Directors held its annual face-to-face meeting on Saturday, November 4, 2017, in Pasadena, Calif., preceding the ISTFA event. Board President Zhiyong Wang kicked off the meeting with the President’s report. Zhiyong discussed the path forward to better meet member needs, including innovative membership models, IT infrastructure for virtual content, an education certificate program, an on-line learning community, an FA technology roadmap, and global communications and collaboration.

ASM Senior Director for Sales and Marketing Ryan Milosh discussed the ASM Renewal, which has a focus on revitalizing membership and revenue growth, scaling up education, maintaining technical excellence, and implementing strategic collaboration and partnerships. The ASM Renewal is on track with lower costs and improving revenue. He also discussed ASM’s IT transformation, which is re-engineering content and has moved ASM’s data center to the cloud. You may notice that the website now works much better on mobile devices.

Starting in 2018, the on-line EDFAS Board elections will be replaced with a paper ballot conducted at ISTFA. ASM plus EDFAS membership will also be realigned to be consistent with other ASM Affiliate Societies and support the ASM Renewal.

Committee chairs shared year-to-date progress and 2018 plans for their respective areas, covering membership, EDFA magazine, education, ISTFA, and international growth. Lee Knauss is leading the effort to create a new edition of the Microelectronics Failure Analysis Desk Reference, while Ryan Ross is leading a new FA Technology Roadmap committee.

Felix Beaudoin, Editor of EDFA, reported that the magazine continues to have excellent technical content and strong advertising. Please contact Felix if you are interested in writing an article!

Looking forward to next year, General Chair Efrat Moyal provided a preview of ISTFA 2018 in Phoenix, Ariz., which will be themed “Failures Worth Analyzing.” David Grosjean was announced as Technical Program Chair for ISTFA 2018. For the first time, ISTFA will be co-located with the International Test Conference (ITC). The ITC 2018 theme is “AI Towards Autonomous Testing.” There will be a joint ISTFA/ITC Expo floor, and possibly joint discussion panels.

The Board of Directors strives to strengthen the visibility and credibility of our Society by providing value to EDFAS members and, through its volunteers, beneficial contributions to our industry. Your engagement in EDFAS is highly encouraged. Please feel free to connect with any Board member to discuss your ideas or interest in volunteering in the Society.
NEW ATOMIC FORCE MICROSCOPE STUDIES PIEZOELECTRICS AT THE NANOSCALE

Combining speed with incredible precision, a team of Molecular Foundry scientists and industry users developed a way to print extremely small devices on the tip of a glass fiber as thin as a human hair. These tiny devices precisely squeeze and manipulate light in ways that are unachievable by conventional optics. The team’s approach, called fiber nanoimprinting, builds tips 30 times faster than today’s sculpting approach. The scale-up path is to print many tips instead of sculpting individual tips.

Tiny optics could help improve the design of solar cells, pharmaceuticals, and semiconductors. Fiber nanoimprinting speeds the production of nano-optics from several per month to several per day. The technique opens the door to mass fabrication of nano-optical devices for widespread use.

Nano-optics have the potential to be used for imaging, sensing, and spectroscopy and could help scientists improve solar cells, design better drugs, and make faster semiconductors. A big obstacle to the technology’s commercial use, however, is its time-consuming production process. The new fabrication method could unplug this bottleneck. It was developed by scientists at the Molecular Foundry in partnership with users from Hayward, Calif.-based aBeam Technologies.

Their work builds on the campanile probe, which was developed by Molecular Foundry scientists four years ago and enables spectroscopic imaging at a resolution 100 times greater than conventional spectroscopy. Fabricating campanile probes has been part science and part art. The same applies to other nano-optical devices, such as microscopic lenses and beam splitters, which split one light beam into several. These devices require milling a 3-D shape with sub-100-nm-scale features on the tip of a wispy fiber, which is much trickier than fabricating a nanostructure on a flat surface such as a wafer.

That’s where fiber nanoimprinting comes in. Its first step is the most time-consuming: scientists create a mold with the precise dimensions of the nano-optical device they want to print. For the campanile probe, this means a mold of the probe’s nanoscale features, including the four sides and the light-emitting 70-nm-wide gap at the pyramid’s top. After the mold is created, it is filled with a special resin and then positioned atop an optical fiber. Infrared light is sent through the fiber, which enables scientists to measure the exact alignment of the mold in relation to the fiber. If everything checks out, ultraviolet light is sent through the fiber, which hardens the resin. A final metallization step coats the sides of the probe with gold layers. The result is a quickly printed—not meticulously sculpted—campanile probe. By doing this over and over, the team can make a probe every few minutes.


PIEZOELECTRIC FORCE MICROSCOPY REVEALS CHARGE MAPPING

In this research, the material was stressed by the atomic force microscope (AFM) tip with nanometric size. The tip applied a force in the range of hundreds of microNewtons and measured the generated charge that was created in the material. The new mode was proved by characterizing several common ferroelectric materials: a periodically poled lithium niobate, bismuth ferrite, and lead zirconate titanate. The mode was employed in...
a standard constant-force contact-mode AFM by using a solid platinum tip with part number RMN-25PT200H. Because the mapping was performed in constant mode, the amplifier gave zero signal while scanning a single domain; however, where the tip crossed a domain, a current was generated as a consequence of the inversion of the generated charge. The researchers were able to integrate the current obtained to estimate the generated charge by the material. The charges recorded were 5 fC for periodically poled lithium niobate, 25 fC for bismuth ferrite, and 90 fC for lead zirconate titanate. Few quantities are really quantitative in the AFM, one of them being the force applied by the tip. By knowing the force and integrating the current generated, researchers were able to estimate the d33 piezoelectric constant of the materials scanned. Force-versus-distance curves were generated, where the tip was placed in one spot and the force applied was changed through a constant force rate applied. By performing such experiments, researchers were able to distinguish between down and up domains, and it opened a window into making spectroscopy experiments quantitative.

The research focused on mapping the piezo-generated charge of a piezoelectric material. Piezoelectricity is a property whereby a charge is generated by a material as a consequence of a mechanical stress applied to the material. In this particular research, the material was stressed by a tiny needle, an AFM tip with nanometric size. The tip applied a force in the range of 100 µN and measured the generated charge that was created in the material. The total charge collected for each material was 5 fC for periodically poled lithium niobate, 25 fC for bismuth ferrite, and 90 fC for lead zirconate titanate. This new mode enhances AFM as a key future technique available for materials research and opens the future into counting electrons at the nanoscale.


OLYMPUS LAUNCHES LASER CONFOCAL SCANNING MICROSCOPE

The new OLYMPUS LEXT OLS5000 3-D laser confocal scanning microscope delivers precise imaging in a fast, easy-to-use system for research and development and quality-control inspection in the automotive, electronic component, and semiconductor industries.

The OLS5000 microscope was designed with the following new features and updated technology to enhance its performance and advance measurement outputs:

- The 4K scanning technology and optics designed specifically for the OLS5000 microscope provide improved measurement performance and reliability. This combination of technology and optics enables the detection of near-perpendicular features and small steps at close to nanoscale.
- It acquires data four times faster and improves the user experience with intuitive software designed to automate many common settings.
- An expansion frame and a dedicated, long-working-distance lens perform precise measurements on samples up to 210 mm in height and concavities up to 25 mm deep, even those with uneven surface cracks.

The result is simple, accurate, noncontact 3-D measurement of a wide variety of samples.

With the steady advancement of nanotechnology and the growing sophistication and miniaturization of electronic devices and car parts, quality management through the accurate measurement of components’ surface features is more important than ever. In the past, inspectors conducted surface shape and roughness measurements using direct-contact, stylus-based roughness instruments. However, an increasing number of samples, such as fragile films or samples with height variations less than the diameter of the stylus, gave rise to a need for more precise, nondestructive, noncontact measurement techniques.
A new 10× lens optimized for a 405-nm-wavelength light source and a long-working-distance lens was designed specifically for use with the LEXT microscope to reduce aberration and enable accurate measurements across the entire field of view. Meanwhile, 4K scanning technology with a resolution of 4096 pixels in the X-direction (four times that of the previous model) enhances resolution and improves the reliability of shape measurements (doubling improvement in the signal-to-noise ratio). These features enable the detection of near-vertical slopes and small steps without image correction.

The OLS5000 microscope uses the PEAK algorithm for fast, precise measurements at both low and high magnifications with four times the data-acquisition speed of the previous model. Smart Scan II and analysis template functions automate the sequence of steps from data acquisition to reporting.

An optional expansion frame enables the OLS5000 microscope to accommodate samples up to 210 mm in height. Observation and measurement can also be performed using a long-working-distance lens, which enables a separation of up to 25 mm between the lens and the sample.

For more information: web: olympus-ims.com.

MINILOCK-PHANTOM RIE FEATURES VACUUM LOADLOCK

Trion Technology’s compact MiniLock-Phantom reactive ion etcher (RIE) with vacuum loadlock is designed to supply research and failure analysis labs with state-of-the-art plasma etch capability. The bottom electrode is available in either 200 or 300 mm sizes and, depending on electrode configuration, can process single wafers or mounted parts (3 in. to 300 mm). It also has multiple-sized batch capability (4×3 in.; 3×4 in.; 7×2 in.).

Applications for corrosive chemistry etching (Cl₂, BCl₃, SiCl₄, HBr, NF₃, etc.) include AlGaAs, gold, carbon, chromium, copper, GaN, GaAs, InAlGaN, InGaAs, InP, light-emitting diode MQMs, polysilicon, platinum, silicon, SiC, titanium, praseodymium, and other organic materials.

Samples are loaded into the process chamber via the vacuum loadlock. This feature increases user safety by preventing contact with the process chamber and any residual etch by-products. The loadlock also allows the chamber to remain permanently under vacuum, thereby keeping out moisture and keeping the reaction chamber free of possible corrosion. Options include:

- An electrostatic chuck (E-chuck), to more effectively keep the wafer cool during the etch process, uses a helium pressure controller to build up a cooling layer of helium on the backside of the wafer.
- An inductively coupled option to create higher-density plasmas increases etch rates and anisotropy.

For more information: web: triontech.com.

OLYMPUS RELEASES NEW INVERTED METALLURGICAL MICROSCOPE

Designed for the observation and inspection of metal components, the new OLYMPUS GX53 inverted metallurgical microscope features a light-emitting diode (LED) light source for ultralong life and low power consumption. The GX53 microscope also incorporates the latest version of OLYMPUS Stream image analysis software (v. 2.3) for improved observation and reporting capabilities.

Inverted metallurgical microscopes observe samples from underneath, enabling the user to inspect thick or heavy samples without adjusting the orientation of the sample surface. This capability makes the GX53 microscope a practical tool for viewing the microstructure of metals used in automotive and other manufactured metal components.

The GX53 offers advanced functions that help inspectors do their jobs faster:

- **See fine details**: MIX observation contributes to clear imaging of microstructures and other surface features.
- **Coded hardware**: Save observation settings for faster inspections and improved productivity.
- **True-to-life images**: LED illumination offers a consistent color temperature.

With the incorporation of MIX observation technology—a first for the GX series—the GX53 microscope can obtain surface structure images with exceptional clarity. MIX technology produces unique observation images by combining darkfield with another observation method, such as brightfield, fluorescence, or polarization. MIX observation enables users to view samples that are difficult to see with conventional microscopes. The circular LED illuminator used for darkfield observation has a directional function whereby one or more quadrants are illuminated at a given time. This reduces a sample’s halation and is useful for visualizing its surface texture.

Meanwhile, the upgraded version of OLYMPUS Stream image analysis software uses image synthesis to provide clear images with minimal halation, even when viewing highly reflective samples.

When used with OLYMPUS Stream software, the GX53 inverted metallurgical microscope can save observation settings for easy recall. This improves user productivity and facilitates inspections by making it easy to replicate frequently used observation settings or the settings of other users.

OLYMPUS Stream image analysis software v. 2.3 supports every step of the inspection process, from preparing the microscope to observation, analysis, and reporting. The latest version includes an instant extended focal image function to bring the entire view field into focus. The software also incorporates improvements to the system’s spreadsheet-based reporting functions.

For more information: web: olympus-ims.com.

NEW TECHNIQUE IMPROVES RESOLUTION OF TERAHERTZ EMISSION SPECTROSCOPY

Researchers at Brown University in Providence, R.I., have improved the resolution of terahertz spectroscopy by 1000 times, making the technique useful at the nanoscale.

Laser terahertz emission microscopy (L TEM) is an expanding means of characterizing the performance of integrated circuits, solar cells, and various other materials and systems. Laser pulses illuminating a sample material result in the emission of terahertz radiation, which carries vital information about the sample’s electrical properties.

“This is a well-known tool for studying essentially any material that absorbs light, but it’s never been possible to use it at the nanoscale,” said Daniel Mittleman, a professor in Brown’s School of Engineering and corresponding author of a paper describing the work. “Our work has improved the resolution of the technique so it can be used to characterize individual nanostructures.”

LTEM measurements are typically performed with resolution of a few tens of microns; however, this new technique allows measurements down to a resolution of 20 nm, roughly 1000 times the resolution earlier possible using standard LTEM techniques.

The research, featured in the journal ACS Photonics, was headed by Pernille Klarskov, a postdoctoral researcher in Mittleman’s lab, along with Hyewon Kim and Vicki Colvin from Brown’s Department of Chemistry.

For their research, the team adapted for terahertz radiation a technique earlier used for improving the resolution of infrared microscopes. This technique uses a metal pin, tapered down to a sharpened tip a few tens of nanometers across, that hovers just above a sample to be imaged. After illuminating the sample, a small portion of the light is captured directly beneath the tip, which enables imaging resolution approximately equal to the size of the tip. It is possible to develop ultrahigh-resolution images of an entire sample by moving the tip around.

Klarskov succeeded in showing that the same technique could also be employed for increasing the resolution of terahertz emission. For their study, Klarskov and her colleagues were able to image a separate gold nanorod with 20 nm resolution using terahertz emission. The researchers are certain their new technique could be extensively used in characterizing the electrical properties of materials in exceptional detail.

“Terahertz emission has been used to study lots of different materials—semiconductors, superconductors, wide-bandgap insulators, integrated circuits, and others,” Mittleman said. “Being able to do this down to the level of individual nanostructures is a big deal.”

According to Mittleman, one example of a research area that could obtain benefits from the technique refers to the characterization of perovskite solar cells, a developing solar technology studied widely by Mittleman’s colleagues at Brown.

“One of the issues with perovskites is that they’re made of multicrystalline grains, and the grain boundaries are what limit the transport of charge across a cell,” Mittleman said. “With the resolution we can achieve, we can map out each grain to see if different arrangements or orientations have an influence on charge mobility, which could help in optimizing the cells.” That is one example of where this could be useful, Mittleman pointed out, but it is definitely not limited to that. “This could have fairly broad applications,” he noted.

The National Science Foundation, the Danish Council for Independent Research, and Honeywell Federal Manufacturing and Technologies supported the research.

For more information: web: www.brown.edu/academics/engineering.
### Training Calendar

**February 2018**

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<td>Pan Pacific Microelectronics Symposium</td>
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**Contact:** SMTA

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**Contact:** ASM International

### March 2018 (cont’d)

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<tbody>
<tr>
<td>19th International Symposium on Quality Electronic Design</td>
<td>3/13-14</td>
<td>Santa Clara, CA</td>
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**Contact:** ISQED 2018

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<tr>
<th>EVENT</th>
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<tr>
<td>IEEE 2nd Electron Devices Technology and Manufacturing Conference</td>
<td>3/13-16</td>
<td>Kobe, Japan</td>
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**Contact:** EDTM 2018

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<tr>
<th>EVENT</th>
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<tr>
<td>Failure and Yield Analysis</td>
<td>3/19-22</td>
<td>San Jose, CA</td>
</tr>
<tr>
<td>Semiconductor Reliability and Product Qualification</td>
<td>3/26-29</td>
<td>Portland, OR</td>
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**Contact:** Semitracks, Inc.

<table>
<thead>
<tr>
<th>EVENT</th>
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<tbody>
<tr>
<td>Intermountain Expo &amp; Tech Forum</td>
<td>3/20</td>
<td>Boise, ID</td>
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**Contact:** SMTA

### March 2018

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<thead>
<tr>
<th>EVENT</th>
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<tbody>
<tr>
<td>ESD Technician Training (in German)</td>
<td>3/5-7</td>
<td>Stuttgart, Germany</td>
</tr>
<tr>
<td>System ESD Protection Design Addressing PCB and IC Aspects</td>
<td>3/14-15</td>
<td>Munich, Germany</td>
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**Contact:** EOS/ESD Association

<table>
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<tr>
<th>EVENT</th>
<th>DATE</th>
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<tbody>
<tr>
<td>18th International Workshop on Junction Technology</td>
<td>3/8-9</td>
<td>Shanghai, China</td>
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**Contact:** IWJT 2018

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<tr>
<th>EVENT</th>
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<tr>
<td>IEEE International Reliability Physics Symposium</td>
<td>3/11-15</td>
<td>Burlingame, CA</td>
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**Contact:** IRPS 2018

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<tr>
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<tr>
<td>PCB Filters and Multiplexers Using Standard SMT Components</td>
<td>3/12-13</td>
<td>Barcelona, Spain</td>
</tr>
<tr>
<td>Grounding and Shielding: The Essence of EMC Design</td>
<td>3/12-15</td>
<td>Barcelona, Spain</td>
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**Contact:** CEI-Europe

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<tr>
<th>EVENT</th>
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<tbody>
<tr>
<td>metallurgical Techniques</td>
<td>3/12-15</td>
<td>Novelty, OH</td>
</tr>
<tr>
<td>Metallurgy for the Non-Metallurgist</td>
<td>3/13-15</td>
<td>Novelty, OH</td>
</tr>
<tr>
<td>Introduction to Metallurgical Laboratory Practices</td>
<td>3/20-22</td>
<td>Novelty, OH</td>
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**Contact:** ASM International

### April 2018

<table>
<thead>
<tr>
<th>EVENT</th>
<th>DATE</th>
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<tbody>
<tr>
<td>Wafer Fab Processing</td>
<td>4/9-12</td>
<td>Munich, Germany</td>
</tr>
<tr>
<td>Failure and Yield Analysis</td>
<td>4/9-12</td>
<td>Munich, Germany</td>
</tr>
<tr>
<td>Semiconductor Reliability and Product Qualification</td>
<td>4/16-19</td>
<td>Munich, Germany</td>
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**Contact:** Semitracks, Inc.

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<tr>
<th>EVENT</th>
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<th>LOCATION</th>
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</thead>
<tbody>
<tr>
<td>Dallas Expo &amp; Tech Forum</td>
<td>4/10</td>
<td>Plano, TX</td>
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<tr>
<td>Houston Expo &amp; Tech Forum</td>
<td>4/12</td>
<td>Houston, TX</td>
</tr>
<tr>
<td>Atlanta 22nd Annual Expo</td>
<td>4/18</td>
<td>Duluth, GA</td>
</tr>
<tr>
<td>Empire Expo &amp; Tech Forum</td>
<td>4/24</td>
<td>Liverpool, NY</td>
</tr>
<tr>
<td>Electronics in Harsh Environments Conference &amp; Expo</td>
<td>4/24-26</td>
<td>Amsterdam, The Netherlands</td>
</tr>
</tbody>
</table>

**Contact:** SMTA
2018 FIB/SEM WORKSHOP

The eleventh annual FIB/SEM Workshop will be held April 30 to May 2, 2018, at McMaster University in Hamilton, Canada. It will feature a workshop, tutorials, and an FIB User Group with demonstrations. The event offers plenty of technical content as well as opportunities for informal discussion with your FIB colleagues.

For more information, contact the following organizers: Nabil Bassim at bassimn@mcmaster.ca or Keana Scott at keana.scott@nist.gov.
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The current column covers a cornucopia of peer-reviewed articles published since 2015 on novel materials and structures, failure mechanics, and reliability. All of these fields are dependent on failure analysis for their success. Note that inclusion in the list does not vouch for the article’s quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.


### NOTEWORTHY NEWS

#### ANADEF 2018

The 16th ANADEF Workshop will be held **June 5 to 8, 2018**, at Belambra Business Club, Seignosse-Hossegur (Landes), France. The conference addresses new issues related to the latest technological developments in electronic component failure analysis, presented through tutorials, plenary sessions, micro-workshops, as well as participation by equipment manufacturers and suppliers.

ANADEF, a French nonprofit scientific society established in 2001, meets biennially to bring together industry experts and mechanism scientists concerned with the prevention, detection, and failure analysis of electronic components and assemblies.

For more information, visit anadef.org.
Electronic companies of all types and sizes require failure analysis (FA) services. Our goal is to supply a resource of FA service providers for your reference files. The directory lists independent providers and their contact information, expertise, and types of technical services offered.

<table>
<thead>
<tr>
<th>DIRECTORY OF INDEPENDENT FA PROVIDERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rosalinda M. Ring, Kionix</td>
</tr>
<tr>
<td><a href="mailto:rring@kionix.com">rring@kionix.com</a></td>
</tr>
</tbody>
</table>

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308 South Abbott Ave.  
Milpitas, CA 95035  
Tel: 408.719.1617  
e-mail: sales@advancedcircuitengineers.com  
Web: acellc.net  
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**ALTER TECHNOLOGY TÜV NORD**  
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41920 Sevilla, Spain  
Tel: +34 95 446 70 50  
Web: wpo-altertechnology.com  
**Services:** FA, electrical testing and characterization, counterfeit detection, etc.  
**Tools/Techniques:** SEM, EDS, FTIR, SIMS, XPS, cross sections, CSAM, bond pull test, die shear test, FIB, glassivation integrity test, PIND test, optical inspections, etc.

**EBATCO NANO ANALYTICAL AND TESTING LABORATORY SERVICES**  
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Eden Prairie, MN 55344  
Tel: 952.941.2199/844.332.2826  
e-mail: info@ebatco.com  
Ebatco Suzhou Office  
Guohua Building A303  
Chongwen Rd., 328 Xinghu St.  
Suzhou Industrial Park, Suzhou  
Jiangsu 215021, China  
Tel: +86 512 6258 0632  
e-mail: suzhouinfo@ebatco.com  
Web: ebatco.com  
**Services:** Analytical testing services, surface characterization, thin-film and contamination analyses, microscopy, etc.  
**Tools/Techniques:** SEM-EDS, FTIR, AFM, SPM, white light interferometry, nano- and microindentation, nano- and microscratch, friction, wear, DMA, TMA, DSC, TGA, particle and pore sizing, contact angle, surface/interface tension, etc.

**HI-REL LABORATORIES**  
6116 N. Freya  
Spokane, WA 99217  
Tel: 509.325.5800 / Web: hrlabs.com  
**Services:** FA, destructive physical and materials analyses, etc.  
**Tools/Techniques:** C-SAM, 2-D real-time/3-D computed tomography x-ray imaging, SEM imaging, EDS, FTIR, FIB cross sections, optical microscopy, external visual inspection, delid, PIND, bond pull, hermeticity, residual gas analysis, die shear, etc.

**INSIDIX**  
14 rue Henri Dunant  
38180 Seyssins, France  
Tel: +33 (0) 4 38 12 42 80  
e-mail: insidix@insidix.com  
Web: http://www.insidix.com  
**Services:** FA, training, sales, etc.  
**Tools/Techniques:** CSAM, 2-D real-time/3-D computed tomography x-ray imaging, lock-in and dynamic infrared thermography, topography and deformation measurements, etc.

**MASER ENGINEERING B.V.**  
Capitool 56  
7521 PL Enschede  
The Netherlands  
Tel: +31 53 480 26 80  
P.O. Box 1438  
7500 BK Enschede  
The Netherlands  
Tel: +31 53 480 26 70  
e-mail: info@maser.nl / Web: maser.nl  
**Services:** Nondestructive physical, construction, failure, and materials analyses; test and diagnostic services; qualification, mechanical, ESD, latch-up, and environmental tests; board-level reliability; consulting; training; etc.  
**Tools/Techniques:** SEM-FIB, scanning probe, SEM/EDX, and optical microscopies; TEM sample prep; 2-D real-time/3-D computed tomography x-ray imaging; CSAM; curve tracing; CCD/InGaAs PEM; absolute/lock-in thermography; AFM; EOTPR; FEG-STEM; STEM-HAADF; laser-assisted fault localization/OBIRCH; FTIR microscopy and analysis; SIMS; x-ray fluorescence and diffraction analysis; scanning ESCA microprobe; etc.
PORTAL TO THE WORLD OF FAILURE ANALYSIS

David Burgess, Accelerated Analysis
davidburgess@AcceleratedAnalysis.com

INTRODUCTION

It is no revelation that failure analysis today is drastically different from failure analysis 25 years ago. Not surprisingly, there is general agreement that failure analysis is tougher today. Problems presented by multi-die packaging, multilayer metallization, and mind-numbing complexity were not imagined. No one is complaining. Everyone is just plowing ahead undaunted, tackling each barrier as it arises. In a way, that attitude is one thing that has not changed. We always have attacked problems from all directions. We developed new imaging, measurement, and testing techniques as required. One major difference between then and now is EDFA magazine. Then, there was no EDFA magazine. How much difference does that make?

EDFA MAGAZINE

EDFA, more than any other magazine, introduces state-of-the-art research and new failure analysis techniques. It expands the horizons of analysts beyond their specific jobs to the limitless variation of failure analysis around the world. Many analysts read EDFA magazine as soon as it arrives. They read to better understand mechanisms and physics that might explain a perplexing failure. And, there is always hope that a case history will provide key insight for a current problem.

I am honored to be one of the nineteen people involved in producing and editing content for EDFA magazine. EDFA is intended to be authoritative, clear, and up to date. Without exception, I am pleased with the result that shows up in my mail box. State-of-the-art features are well written and successfully edited to present information logically and understandably. Case histories are summed up meaningfully, with clear and documented analysis steps. EDFA is a valuable resource for analysts.

EDFA also provides a way for analysts to share tricks for overcoming analysis barriers and tips for exploiting or extending the powers of failure analysis equipment. Analysts struggle with difficult tasks every day. Smart, clever innovations sometimes make awkward tasks easy. The “Master FA Technique” column is an EDFA feature that allows analysts to share such ideas in a short, concise note. EDFA is a tool that analysts can use to share best practices.

More than that, EDFA is a place to find references to failure analysis publications and failure analysis laboratories. All of this is good, but there is a danger.

The danger is that analysts underestimate their own work. Analysts, potential authors for EDFA, may dismiss the idea of writing because their own work is so familiar to them. Analysts are just doing their jobs today in the same way that they have for a long time. Many may assume they have nothing to write about. When this happens, we all lose. Potential authors lose because they don’t receive the benefits of being an EDFA author. (Authors do enjoy benefits to their careers.) The rest of us lose because a rich source of good ideas is blocked from us.

The irony is that, in fact, good ideas are everywhere. All failure analysts are faced with unique problems every day, and every day unique, clever solutions are found.

EDFA is not just a resource for failure analysts. More accurately, EDFA is a portal between each analyst and the world of failure analysis.
more difficult than ever. *EDFA* magazine is a great source of ideas and techniques, but that is just a start. Use and build on ideas you find, and, when you can, use *EDFA* to share innovative ideas that you develop. Call or e-mail *EDFA*’s Editor or any of the Associate Editors to discuss your idea. You will find someone eager to listen and ready to provide honest feedback. There is nothing to lose.

**ABOUT THE AUTHOR**

David Burgess is a failure analyst and reliability engineer. He developed techniques and taught in those areas at Fairchild Semiconductor and Hewlett-Packard. He is the founder of Accelerated Analysis, a manufacturer and distributor of specialty failure analysis tools. David is the co-author of *Wafer Failure Analysis for Yield Enhancement*. A graduate of Rensselaer Polytechnic Institute and San Jose State University, he is a member of EDFAS and has served on various ISTFA committees. David is a Senior Life Member of IEEE and was General Chairman of the 1983 International Reliability Physics Symposium (IRPS).
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