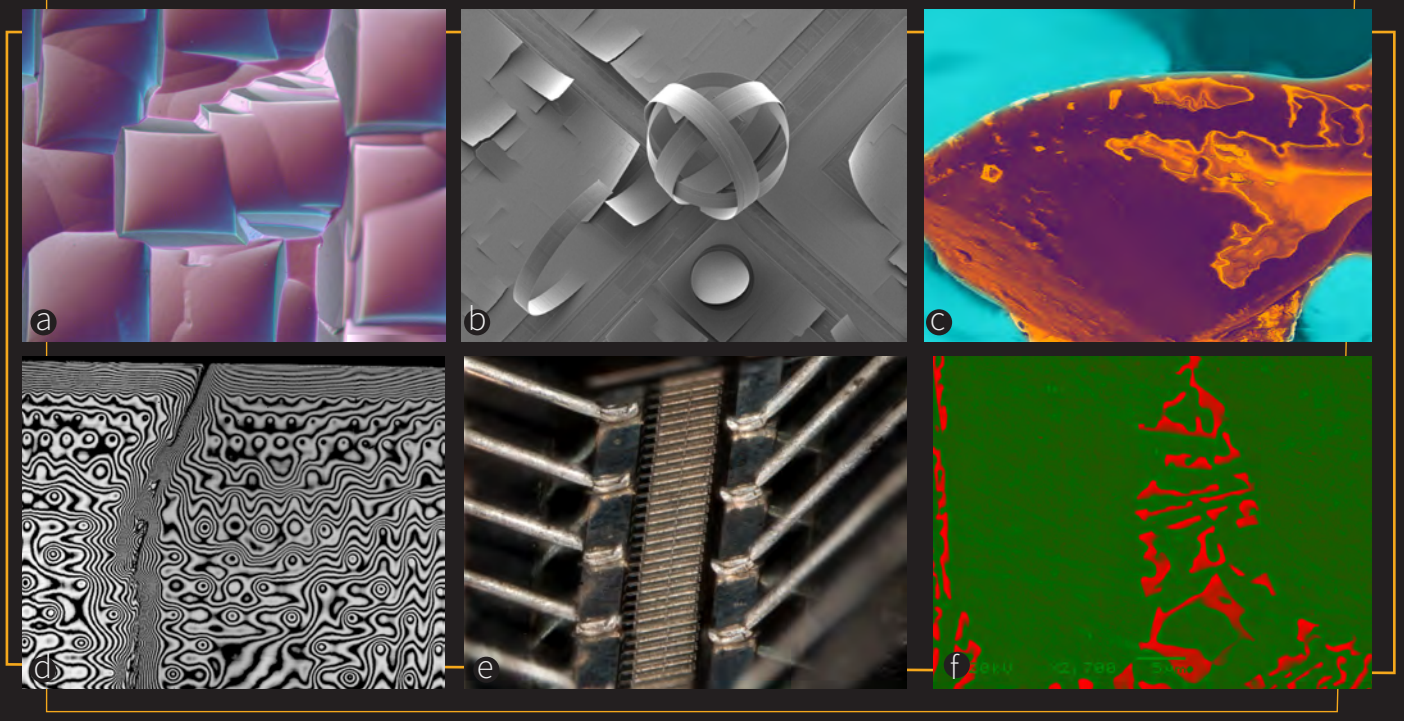
NOVEMBER 2017 | VOLUME 19 | ISSUE 4

edfas.org

ELECTRONIC DEVICE FAILURE ANALYSIS™

A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS

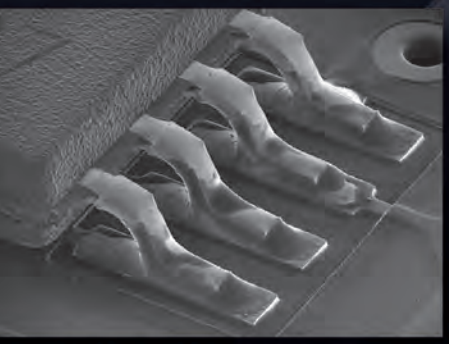
2016 WINNERS PAGE 64



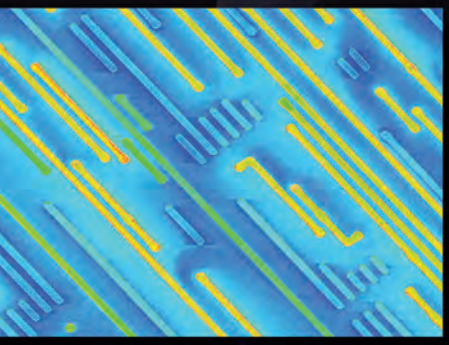
EDFAS
Electronic Device Failure Analysis Society
ASM INTERNATIONAL

UNLOCK THE ANSWERS

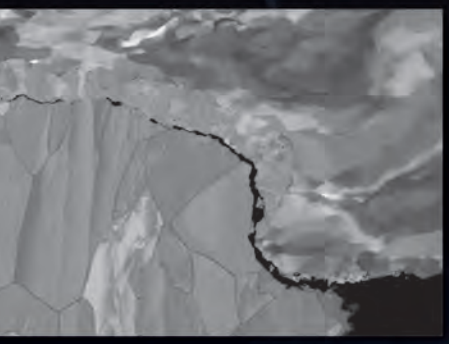
TO YOUR FAILURE ANALYSIS QUESTIONS WITH



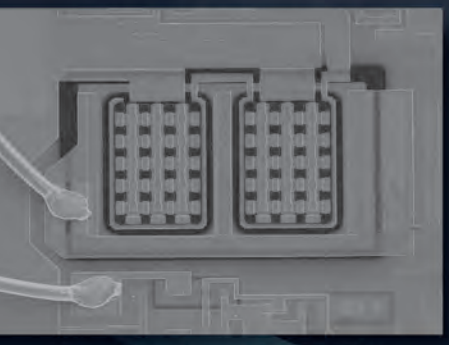
SEM Image of Semiconductor Device



Passive Voltage Contrast (PVC)
image of semiconductor device



Backscatter Electron (BSE)
image of Wire Bond Cross Section



Electron Beam Induced Current (EBIC)
Image of Semiconductor Device

SMART
FLEXIBLE
POWERFUL

SEM

Questions about...

- *Fatigue?*
- *Corrosion?*
- *Fracture?*
- *Delamination?*
- *Layer Integrity?*
- *Interfaces?*

Come see how JEOL high resolution, analytical Scanning Electron Microscopes and precision Cross Section Polishers help you get answers.

Visit jeolusa.com/jeolfa

JEOL
Solutions for Innovation

salesinfo@jeol.com

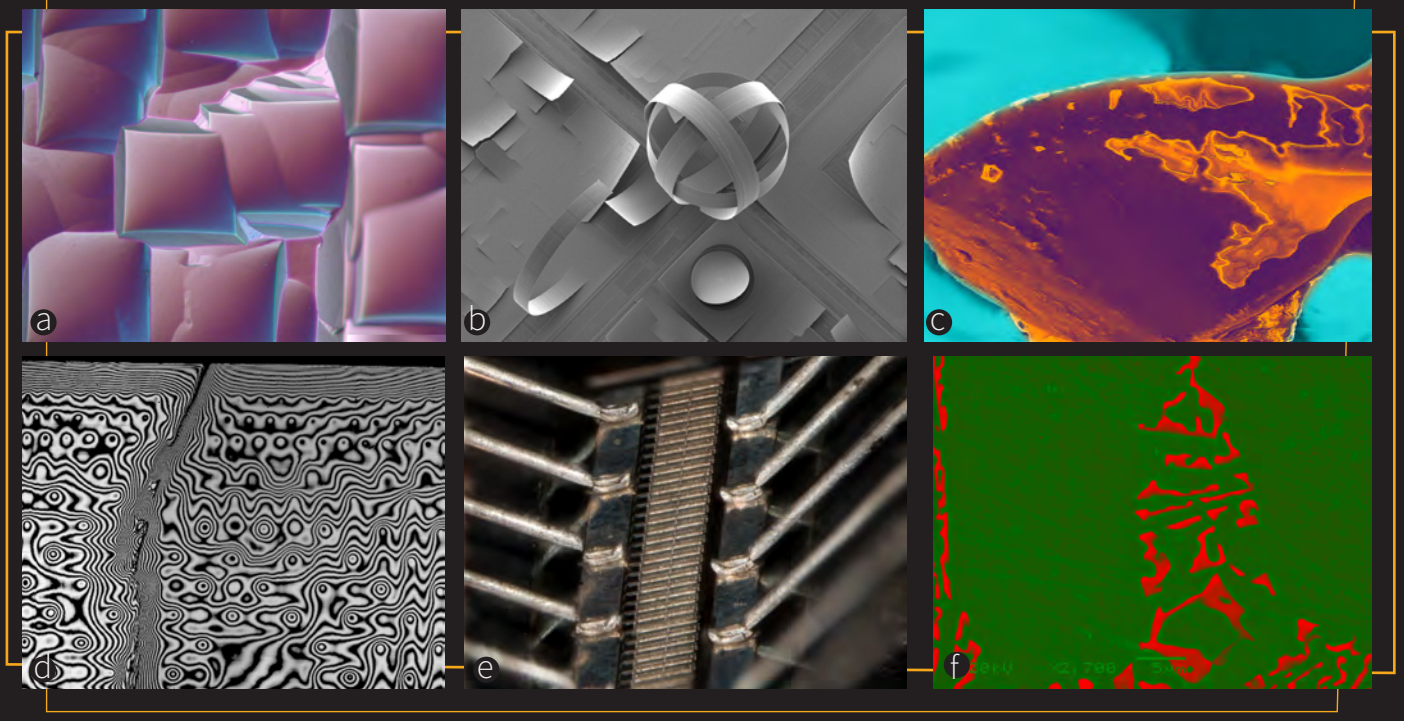
NOVEMBER 2017 | VOLUME 19 | ISSUE 4

edfas.org

ELECTRONIC DEVICE FAILURE ANALYSIS™

A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS

2016 WINNERS PAGE 64



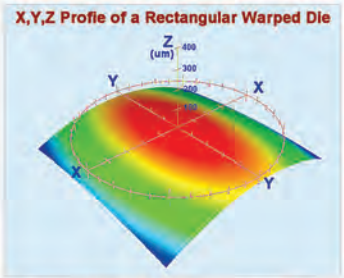
EDFAS
Electronic Device Failure Analysis Society
ASM INTERNATIONAL

ASAP-1® IPS

Interactive Preparation System

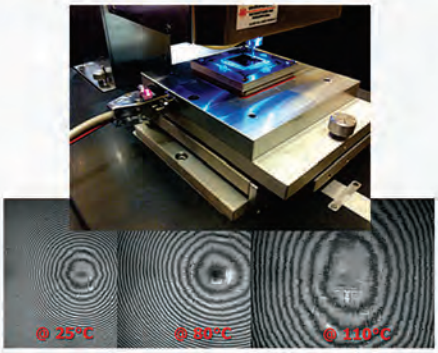
- Realtime Video Monitor with System Parameters
- **Huge Cavity Size Range - <0.25mm² to >1,600mm²**
- Automatic Endpoint option
- Full 5-Axis systems available
- **Open System Design** allows for fixturing all types and size of part – from surface-mount components, up to Motherboards and Wafers
- Touch-screen control with physical Joystick and Controls – **Best of Both Worlds**
- Meet Current SIL/LVP Requirements (demonstrated 50µm RST +/- 2µm on Flip Chip), and Single Digit RST

MEET 3D & CURVED/WARPED SURFACE CHALLENGES WITH ADVANCED TECHNIQUES



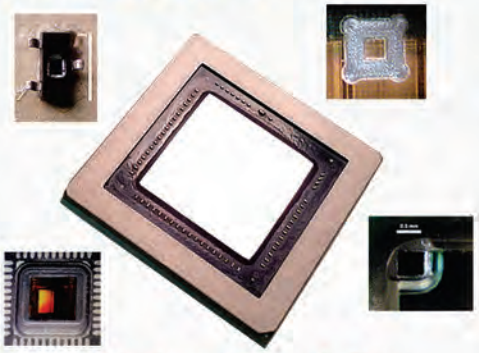
Curvature Compensation

- Auto-Curve and Auto-tilt Setup
- Independent X & Y Axes
- Convex & Concave Surfaces



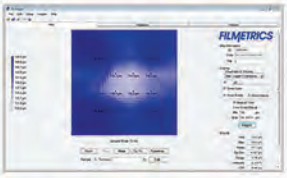
Thermal Relaxation

- Safe and Reliable method to turn complex 3D scenarios into simpler 2D ones
- Reduces dynamic flex of substrate during preparation
- In-situ Hotplate Mode for sample mounting



All Package Types & Sizes

- Parts can be decapped, thinned & polished in as little as 45 minutes



F-Series Wafer Thickness Measurement System

- Multiple or single-point measurements
- Both 2D and 3D data generated
- Provides Information for achieving final uniformity

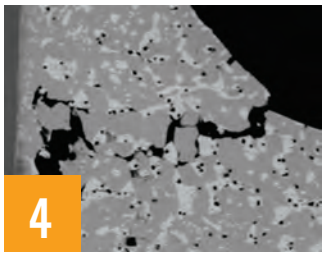
ULTRA TEC MANUFACTURING, INC.

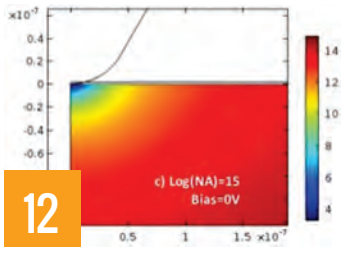
Toll Free (US) 1-877-542-0609
Tel: 1-714-542-0608 Fax: 1-714-542-0627
e-mail: info@ultratecusa.com
www.ultratecusa.com

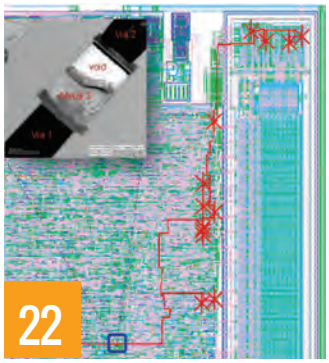
NOVEMBER 2017 | VOLUME 19 | ISSUE 4 edfas.org

ELECTRONIC DEVICE FAILURE ANALYSIS™

A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS







ABOUT THE COVER

See page 64 for a description of the contest winners' collage on the cover.

Author Guidelines

Author guidelines and a sample article are available at edfas.org. Potential authors should consult the guidelines for useful information prior to manuscript preparation.

For the digital edition, log in to edfas.org, click on the "News/Magazines" tab, and select "EDFA Magazine."

DEPARTMENTS

ELECTRONIC DEVICE FAILURE ANALYSIS™
A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS
NOVEMBER 2017 | VOLUME 19 | ISSUE 4

PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

Felix Beaudoin
Editor/GLOBALFOUNDRIES; felix.beaudoin@globalfoundries.com

Scott D. Henry
Publisher

Mary Anne Fleming
Manager, Technical Journals

Kelly Sukol
Production Supervisor

Liz Marquard
Managing Editor

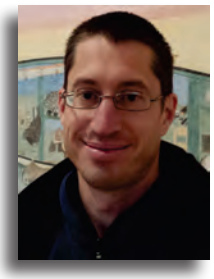
PRESS RELEASE SUBMISSIONS
magazines@asminternational.org
Electronic Device Failure Analysis™ (ISSN 1537-0755) is published quarterly by ASM International®, 9639 Kinsman Road, Materials Park, OH 44073; tel: 800.336.5152; website: edfas.org. Receive *Electronic Device Failure Analysis* as part of your EDFAS membership of $88 U.S. per year. Non-member subscription rate is $135 U.S. per year.

Electronic Device Failure Analysis is indexed or abstracted by Compendex, EBSCO, Gale, and ProQuest.

EDITORIAL

EDFAS SUCCESS THROUGH VOLUNTEERS!

Felix Beaudoin, Editor
GLOBALFOUNDRIES
felix.beaudoin@globalfoundries.com



"Striving for 100% Success Rate" is the theme of the 2017 International Symposium for Testing and Failure Analysis (ISTFA). If you attend the conference, you will certainly find the keys to success by joining the many planned technical sessions, users' groups, panel discussion, keynote presentation, and by exchanging with your peers. This year I have the privilege to act as the Technical Program Chair, and I assure you the conference will deliver on the technical quality, thanks to the dedication of all the volunteers on the ISTFA Organizing Committee. To the 100+ technical chairs, co-chairs, and reviewers who spent endless hours diligently mentoring oral and poster manuscripts, THANK YOU!

Success can be defined and measured in several ways. The panel discussion on the conference theme will surely debate questions such as: What does 100% success rate really mean to your organization? How best to overcome challenges in order to achieve success? As an individual contributor, I have the firm belief that success in our field of electronic device failure analysis can only be achieved by developing broad interdisciplinary scientific and technological knowledge. Peer mentoring, technical conferences, tutorials, short courses, and publications are all sources of information that are part of the EDFAS Society's mission to foster education and communication in the failure analysis community, which is, of course, powered by volunteers.

In particular, *EDFA* magazine relies on its volunteer Associate Editors, listed on page 2, to recruit and mentor technical contributions, write the various informative departments, and seek out guest editorials and columnists from experts worldwide. I would like to recognize James J. Demarest, who will be retiring from the *EDFA* Editorial Board. His main motive in stepping aside is to make way for new volunteers, fostering the growth of the magazine through fresh opportunities to serve. His expertise will be deeply missed.

EDFA magazine, and more generally our EDFAS Society, can only thrive with the help of volunteers like you. Please consider contributing technical articles to share your knowledge. New communication and social media tools now establish virtual content and help reach a broader audience who are dealing with failure of electronic devices in emerging application fields. We need help to create content for those new platforms. If you attend the conference, do not hesitate to stop me or any of the EDFAS Board members and Technical Session Chairs to introduce yourself and discuss your interests.

Ready to get involved? Please contact me or Sweta Pendyala, the Volunteer Committee Chair, at sweta.pendyala@globalfoundries.com. EDFAS can be "Striving for 100% Success Rate" only with volunteers like you!!!

Need higher resolution?

Use the Zurich Instruments UHFLI to generate and analyze your signal patterns up to 600 MHz

ISTFA/2017
booth #804

The Zurich Instruments UHFLI

- Lock-in amplifier measures amplitude and phase information with high signal-to-noise ratio and high precision
- AWG generates any waveform on the outputs
- Boxcar & Scope extract specific subsets from complex excitation patterns
- Imaging module converts your measurements directly into images
- APIs provide full control and integration through LabVIEW®, MATLAB®, C#, Phyton and .NET
- Analog Interfacing integrates easily with your existing Failure Analysis equipment

Get in touch
www.zhinst.com
info@zhinst.com
Intl. +41 44 515 0410
USA +1 617 765 7263

Your Application. Measured.

Zurich Instruments

EDFAAO (2017) 4:4-9 1537-0755/$19.00

FAILURE ANALYSIS OF DC/DC CONVERTERS: A CASE STUDY

Jérémie Dhennin, ELEMCA
jeremie.dhennin@elemca.com

INTRODUCTION

DC/DC converters are widely used in electronic applications and, in particular, in the aerospace industry. In this case study, a defective part was retrieved from an aircraft following an abnormal system behavior detected by the airline crew. The incriminated component is a DC/DC converter, which has a single 28 V input and two outputs, at 5 and 18 V.

The main difficulty in the failure analysis of such a component is its integration. Two printed circuit board assemblies (PCBAs) are assembled in the same package and molded in a resin (Fig. 1). This layout induces additional challenges for the failure investigation, because 3-D techniques must be used to locate the defect.

As usual, the first step of the failure analysis process is to electrically test the component and determine the region that will be further analyzed in the next steps. Here, any local probing of the PCBAs is complicated by the presence of the overmolding resin. This obstacle makes the failure analysis difficult from the outset.

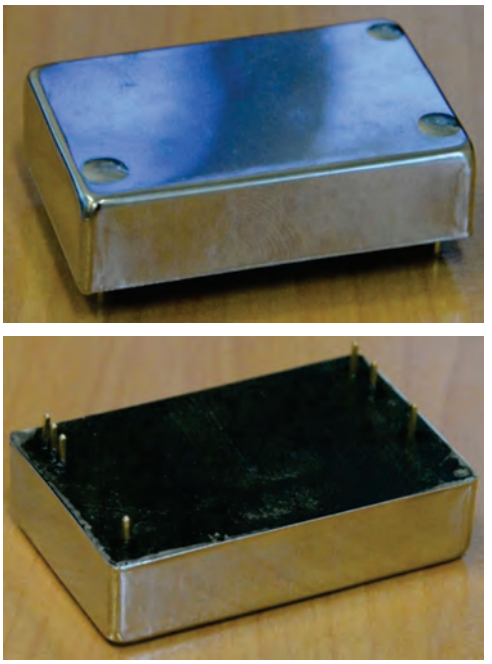


Fig. 1 Photos of the DC/DC converter

DEFECT LOCALIZATION

ELECTRICAL TESTING

The observed failure mode is a bad converter startup. Indeed, the overvoltage/undervoltage protection section seems to be unduly activated. The outputs are correctly set by the component but are trimmed down to 0 V after a few milliseconds. An oscilloscope plot is presented in Fig. 2.

The resin was locally opened to access probing areas to investigate the overvoltage/undervoltage region. This function consists basically in a comparator system (Fig. 3).

LOCAL PROBING

The probing areas were opened with a laser ablation system. To accurately locate the test points, x-ray computerized tomography (CT) of the entire converter was performed. It is important to obtain precise localization of the regions to be opened, because the functionality of the converter must be ensured. Indeed, approximately 1 mm backlash is used to place the PCBAs in the converter cap before molding. Consequently, the exact position of the components inside the converter is not known.

With x-ray CT, a virtual volume of the device was obtained. The latter has been superimposed with an optical image to correlate the internal structure of the PCBA with the external shape of the converter. The 40 µm scan resolution is accurate enough to determine the exact position of the regions to be opened. Figure 4 presents a virtual slice of the PCBA, obtained by x-ray CT, with the opening points identified in red.

Local probing shows that the input of the converter system is not defective, but the output exhibits large oscillations (Fig. 5).

X-RAY IMAGING

Focused x-ray imaging of the small-outline eight-pin (SO8) component (Fig. 6) confirmed that it is the defective

device. Cracks were detected on four pins located on the same side of the component.

Of course, this defect could have been seen from the beginning of the failure analysis process. X-ray imaging had been performed at the start, but it is almost impossible to find the defect when one does not know where to look for it. Also, x-ray images are tricky to read, because the device is a superposition of two double-sided PCBAs.

The same defect was found on other nonfunctional DC/DC converters.

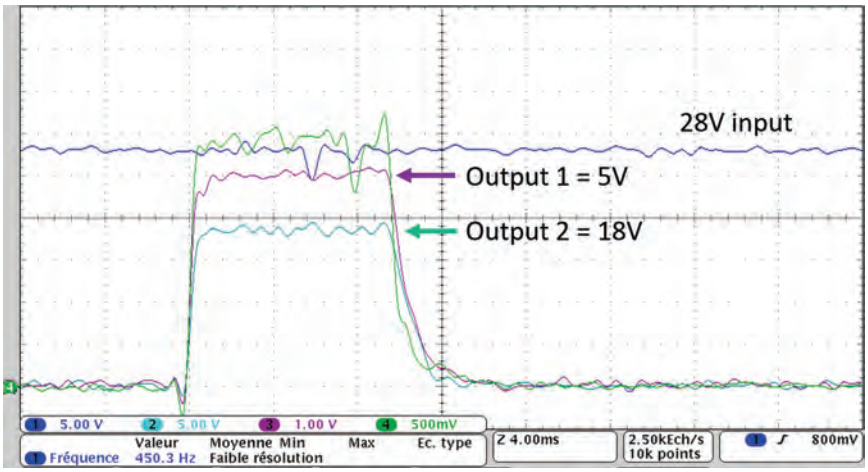


Fig. 2 Oscilloscope plot of the input/output signals

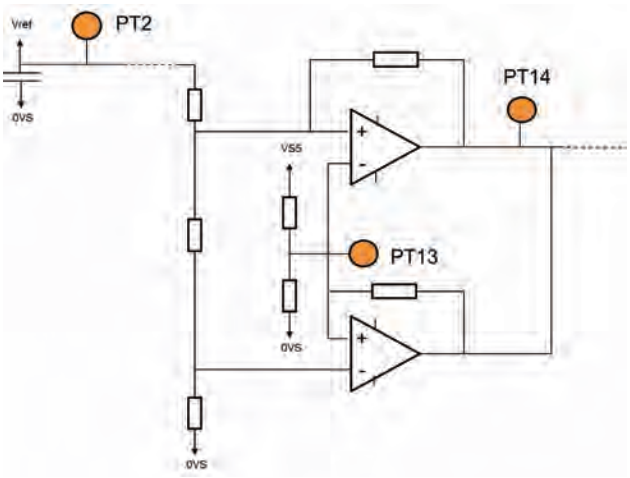


Fig. 3 Simplified design of the overvoltage/undervoltage protection function

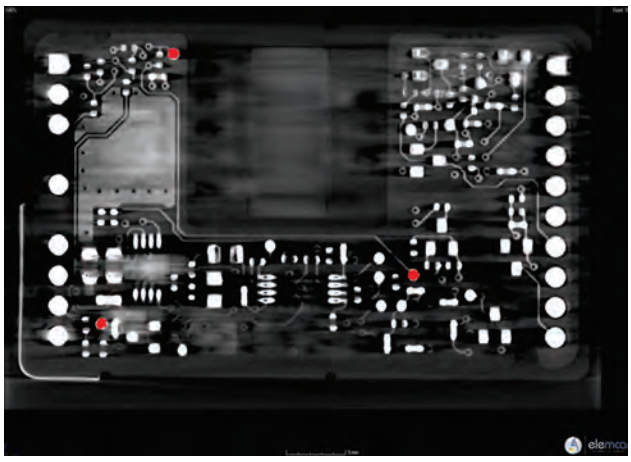


Fig. 4 Identification of the test points on a virtual slice obtained by x-ray CT

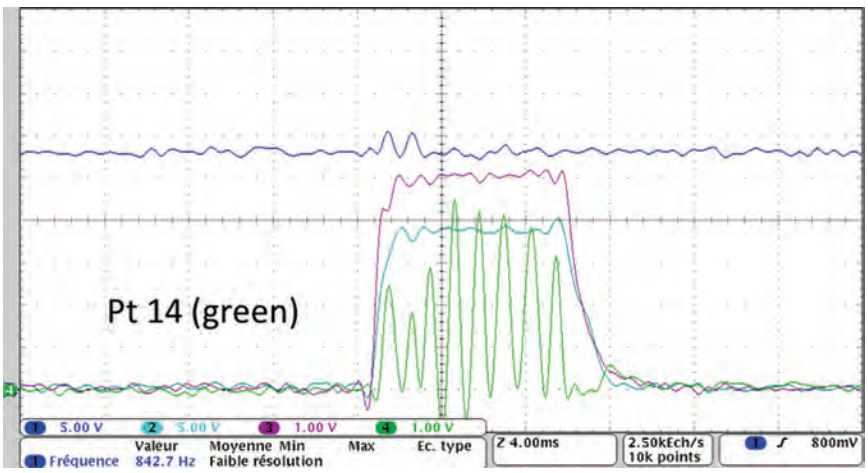


Fig. 5 Local probing results (output of the comparator in green)

DESTRUCTIVE ANALYSIS

To inspect the solder material, a cross section was performed with optical (Fig. 7) and scanning electron microscopy (SEM) imaging (Fig. 8).

A crack was confirmed under one pin. The other side of the component was not affected. The solder material thickness between the pin and the pad was found to be very low.

The SEM observation showed that phase segregation has occurred. The intermetallic at the interfaces with the pin and the pad is continuous and seems correctly formed.

Other functional DC/DC converters were also studied to control the solder material. Recrystallization was found on many of them (Fig. 9). Recrystallization is an early stage of crack formation. The strain that is stored in the material is released by rearranging the atoms in smaller grains.

UNDERSTANDING THE ROOT CAUSE

The hypothesis is that thermomechanical stresses generated by the different coefficients of thermal expansion (CTEs) are the cause of the failure. No clue was found to incriminate the fabrication process. The thermomechanical stresses that apply to the solder joint may stem from various causes:

- The CTE of the molding resin itself
- The different CTEs between the component and the PCB
- The position of the device on the PCB (far from the center)

Because a redesign of the PCB would have implied too many industrial consequences, the focus was on minor modifications, such as a change of resin or solder material.

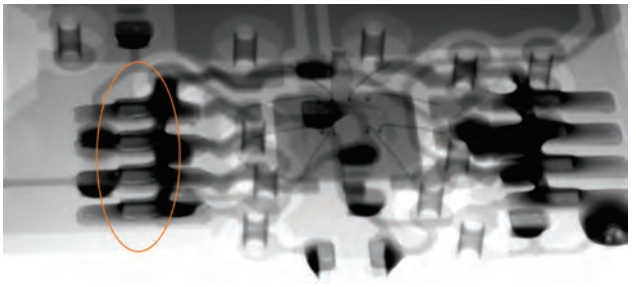


Fig. 6 X-ray image of the SO8 defective device

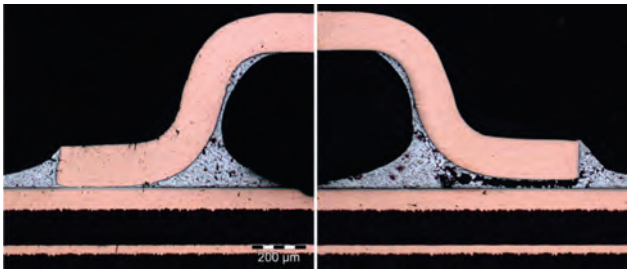


Fig. 7 Optical images of the pins and solder material

IMPACT OF RESIN CTE

The resin CTE was measured with thermomechanical analysis (TMA) in the compression mode (Fig. 10). The postreticulation energy also was controlled with differential scanning calorimetry.

The results show that the resin is correctly reticulated, but the glass transition temperature (T_g) is low compared to the application temperature range. Indeed, the T_g was measured at approximately 80 to 100 °C, but the DC/DC converter itself is supposed to self-heat at approximately 120 °C when operated.

If the operating temperature of the device exceeds the T_g, the CTE increases quickly. This phenomenon implies that the stress applied on the solder joints increases until recrystallization and a crack appear.

IMPACT OF SOLDER JOINT THICKNESS

The plastic strain stored in the solder joints was controlled with the electron backscatter diffraction (EBSD) technique. This type of imaging is performed inside an SEM chamber. It is useful to acquire the orientation of the crystalline network for every pixel of an SEM image. Because strain induces local changes in the crystalline network

(continued on page 8)

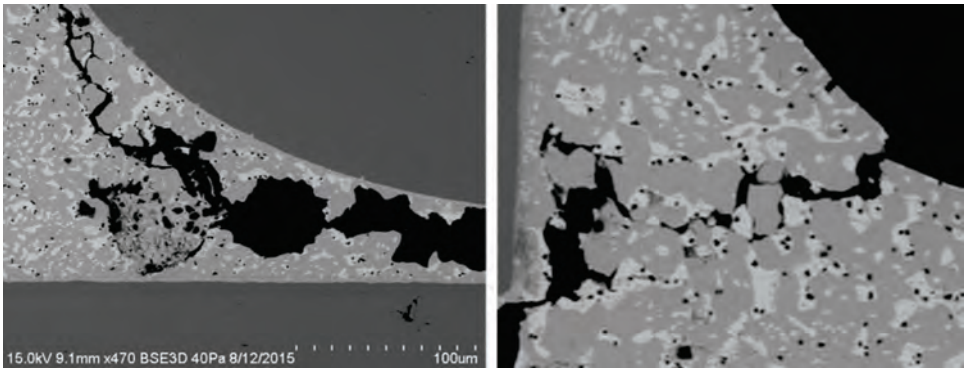
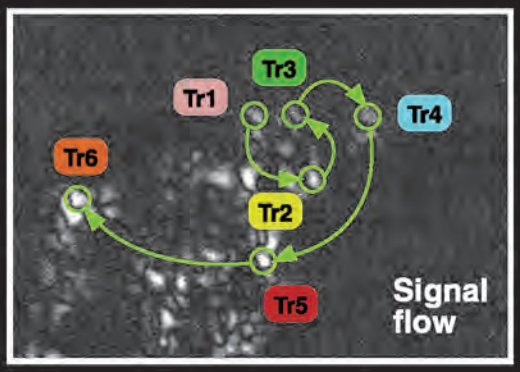


Fig. 8 SEM images of the crack

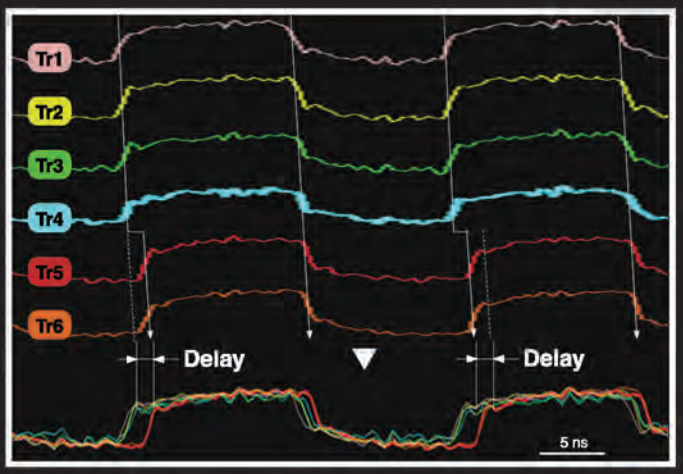
Fast, accurate optical probing of frequency nodes

EO Probing Unit uses an incoherent light source to produce high-quality images without causing thermal damage to the sample chip. Probe waveforms with high S/N are generated in as little as 2 seconds.

NEW



EOFM (electro-optical frequency mapping): This function captures images of nodes in isolated regions operating at a specific frequency. It makes it easier to observe whether or not the circuits are correctly switching.



EOP (electro-optical probing): This feature measures the timing of nodes through high-speed sampling. It improves the accuracy of failure point localization, thus enabling a smoother follow-up physical analysis.

Applications

- Scan chain failure analysis
- Timing shift error observation

Other features

- High-speed sampling up to 4 GHz
- Simultaneous two-channel image acquisition
- Easy-to-use software interface
- Retrofits with Hamamatsu Failure Analysis tools

Available for these systems:
PHEMOS | iPHEMOS | THEMOS | µAMOS | TriPHEMOS

Learn more at www.hamamatsu.com or call 858-210-6703

HAMAMATSU
PHOTON IS OUR BUSINESS

Failure Analysis System

FAILURE ANALYSIS OF DC/DC CONVERTERS: A CASE STUDY *(continued from page 6)*

orientation, a map can be obtained. This technique is not quantitative, but a comparison can be made between two different devices. Here, the author tried to minimize the stress level on the solder material by increasing the thickness of the joint.

EBSD analysis also provides information about grain size, phase identification, and texture, which is the property of a material composed of grains oriented in the same crystalline direction. The following images present the results obtained on a thick solder joint along with a comparison to a thin solder joint. The material used is SnPbAg.

Figure 11 presents the phase mapping for thick and thin solder joints. No aging was applied on the devices prior to this analysis (no thermal cycles and only functional tests of the DC/DC converter). An important difference to note is the presence of needle-shaped silver precipitates (Ag_3Sn) in the thick solder joint, whereas those precipitates are more circular in the thin joint. This

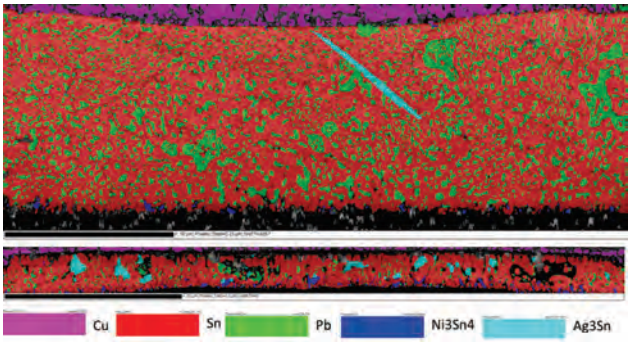


Fig. 11 Phase identification for thick (above) and thin (below) solder joints

form factor modification is an indication of early stages of aging for the solder material.

Figures 12 and 13 show the local misorientation maps for both thick and thin joints. The colormap is representative of the crystalline misorientation from one pixel to the other, which can be interpreted as the strain stored in the material.

The histogram repartition shows that both the average and the maximum misorientation values are higher for the thin joint, which confirms that it was more affected by thermomechanical stresses. This quantitative observation is consistent with a more qualitative approach. The strain applied by the potting resin deformation is spread over a thinner joint, which implies more local stress.

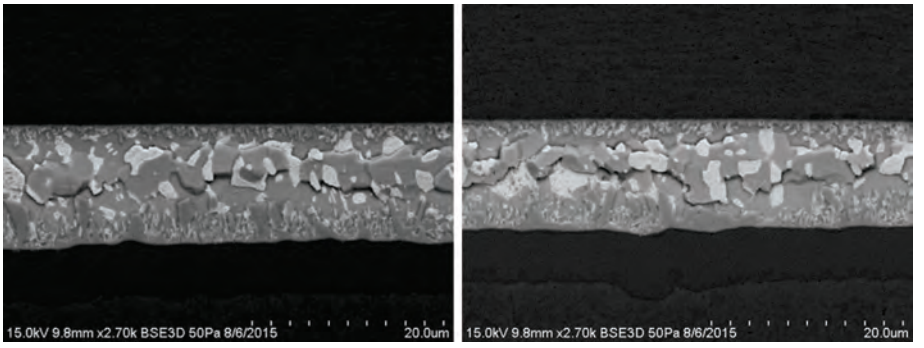


Fig. 9 SEM images of the solder material between the pin and the pad. Recrystallization was found for both devices.

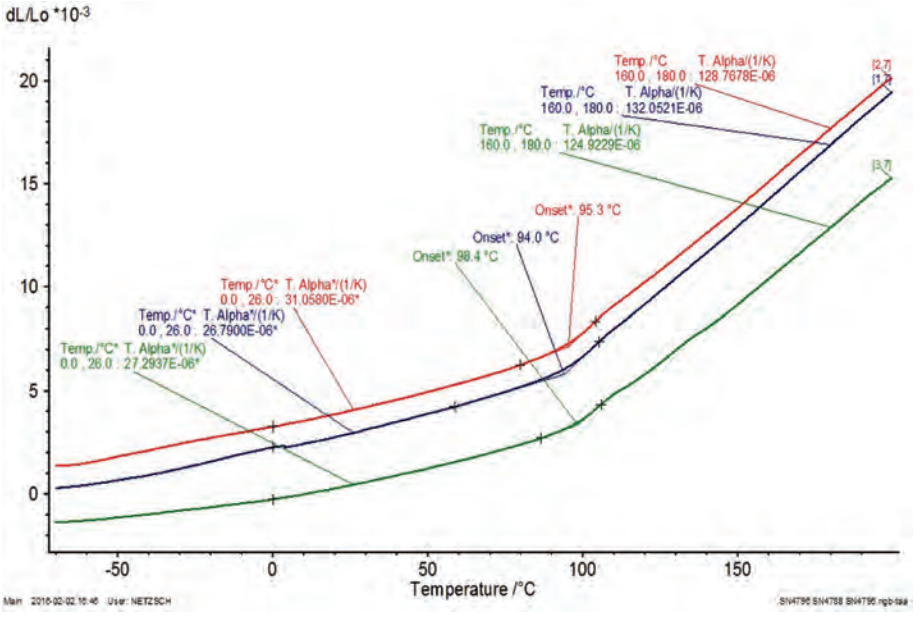


Fig. 10 Strain-versus-temperature curves obtained by TMA

CONCLUSION

Failure analysis of a DC/DC converter was successfully undertaken. When defect localization is tricky—as for 3-D systems—a local probing approach is probably the best way to limit the region of investigation, until the defect is actually detected. This step is quite difficult to undertake. Overmolding resin etching must be nondestructive for both the component and the defect, so sample-preparation techniques must be adapted from device to device. In this case study, laser ablation provided good results,

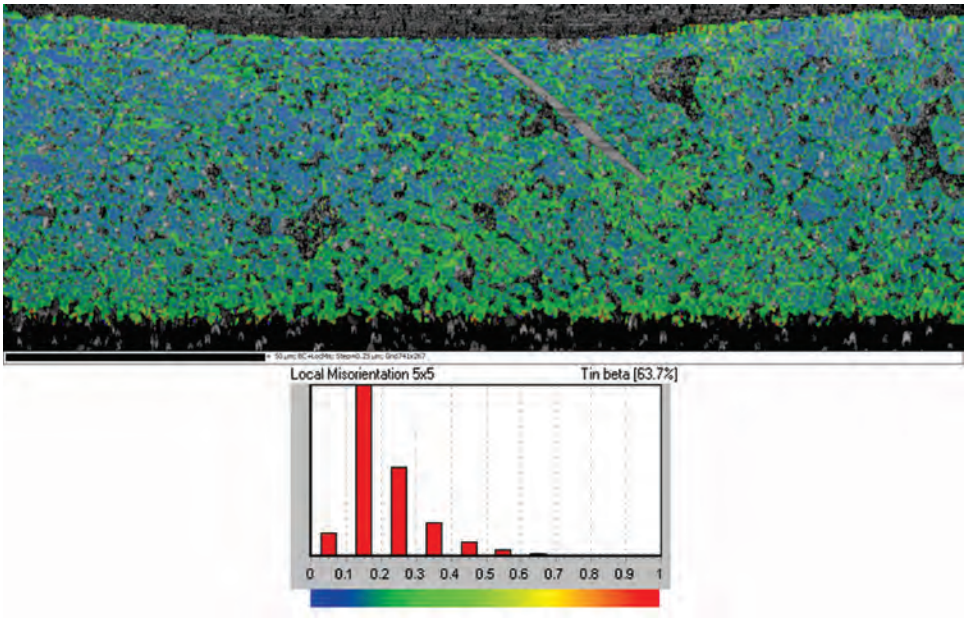


Fig. 12 **Local misorientation mapping and associated histogram repartition for a thick solder joint**

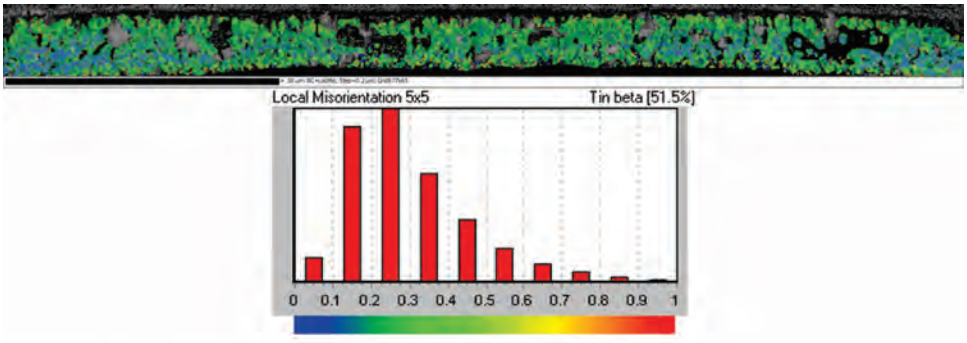


Fig. 13 **Local misorientation mapping and associated histogram repartition for a thin solder joint**

assuming that the location to be opened is precisely known. Superimposition with an x-ray CT virtual slice of the PCB was useful for correctly placing the laser on top of the areas to be opened.

Understanding the root cause of the failure is another challenge. This article showed that thermomechanical stresses applied to a solder joint generate the cracks. Those stresses originate from different phenomena: the resin CTE, the thickness of the solder joint, and its internal ability to withstand shear stress. All three parameters have been optimized to enhance the reliability of the DC/DC converter.

ABOUT THE AUTHOR

Jérémie Dhennin received his Master's degree in micro- and nanophysics from the University of Paul Sabatier in Toulouse, France, in 2005. He joined NOVA MEMS as a research engineer working on multiphysical characterization and modeling of MEMS switches failure mechanisms. His research activities focused on radio-frequency MEMS switches reliability, failure analysis, and modeling, especially dealing with microcontact issues. Since 2012, Mr. Dhennin's technical scope has evolved to more generic reliability issues, dealing with other types of MEMS or electronic components. His managerial experience and broad technical scope allowed him to assume the Chief Executive Officer position at NOVA MEMS (now ELEMCA) in early 2013. He is still involved in many failure analysis processes, dealing with both electronic devices and MEMS components.

QuantumScope™
Failure Analysis Microscopes

FA engineers need proper tools in order to locate IC defects:

- ohmic shorts
- impedance issues
- leakage currents
- leaky capacitors
- oxide defects
- damaged junctions
- resistive vias
- CMOS latch up
- ESD damage
- dynamic failures

QFI suggests maximizing your defect capture rate... NOT your capital expenditure rate.

QuantumScope™ integrates XIVA™ LSIM, Thermal-HS hot spot detection, and emmi™ photoemission into a single, high-performance, microscope platform. Semiconductor FA is more efficient and more accurate when the DUT remains mounted in a single diagnostic tool during all three of these FA microscope techniques. QuantumScope™ eliminates the need for multiple separate systems, freeing capital for other requirements. QFI systems are modular in design and generally compatible with field upgrade.

QFI Quantum Focus Instruments Corporation

2385 La Mirada Drive • Vista CA 92081
Phone: +1 (760) 599-1122
Fax: +1 (760) 599-1242
e-mail: sales@quantumfocus.com
http://www.quantumfocus.com

EDFAAO (2017) 4:12-20 1537-0755/$19.00

NANOSCALE CAPACITANCE AND CAPACITANCE-VOLTAGE CURVES FOR ADVANCED CHARACTERIZATION OF ELECTRICAL PROPERTIES OF SILICON AND GaN STRUCTURES USING SCANNING MICROWAVE IMPEDANCE MICROSCOPY (sMIM)

Oskar Amster, Stuart Friedman, Yongliang Yang, and Fred Stanke
PrimeNano, Inc.
amster@primenanoinc.com

OVERVIEW

A relatively new electrical mode, scanning microwave impedance microscopy (sMIM), measures a material's change in permittivity and conductivity at the scale of tens of nanometers.[1] The use of atomic force microscopy (AFM) electrical measurement modes is a critical tool for the study of semiconductor devices and process development. More specifically, the application of AFM electrical modes is an important tool for characterizing semiconductor devices during process development and failure analysis. The AFM-based electrical measurement techniques, such as scanning capacitance microscopy (SCM) and scanning spreading-resistance microscopy,[2,3] have shown value for dopant profiling in semiconductor samples with sub-50 nm spatial resolution. However, there has been no single scanning probe technique capable of quantifying at submicron dimensions the local electrical properties of materials (dielectric constant and conductivity) with the sensitivity and dynamic range required by the semiconductor industry and research communities.

Scanning microwave impedance microscopy provides the capability to directly probe a sample's permittivity and conductivity at submicron geometries. Scanning microwave impedance microscopy provides the real and imaginary impedance (Re(Z) and Im(Z), respectively) of the probe-sample interface impedance. By measuring the reflected microwave signal of a sample of interest imaged with an AFM, one can capture in parallel the variations in permittivity and conductivity and, for doped semiconductors, the variations in depletion-layer geometry.[4,5] Scanning capacitance microscopy, an existing technique for characterizing doped semiconductors, modulates the tip-sample bias and detects the tip-sample rate of change of capacitance with bias voltage using a lock-in amplifier. A previous study compared sMIM to SCM and highlighted the additional capabilities of sMIM,[6,7] including examples of nanoscale capacitance-voltage curves.

"SCANNING MICROWAVE IMPEDANCE MICROSCOPY PROVIDES THE CAPABILITY TO DIRECTLY PROBE A SAMPLE'S PERMITTIVITY AND CONDUCTIVITY AT SUBMICRON GEOMETRIES."

The initial implementation of sMIM focused on the relative measurement of local permittivity and conductivity at a sample surface. The capability to directly image the local variation of a sample's electrical properties at spatial resolutions of tens of nanometers has stimulated new areas of research. For technologically and scientifically important materials, such as graphene,[8] carbon nanotubes,[9] ferroelectric domains,[10,11] and doped semiconductors,[12-14] researchers are actively using this technique to gain new understanding of materials systems behavior.

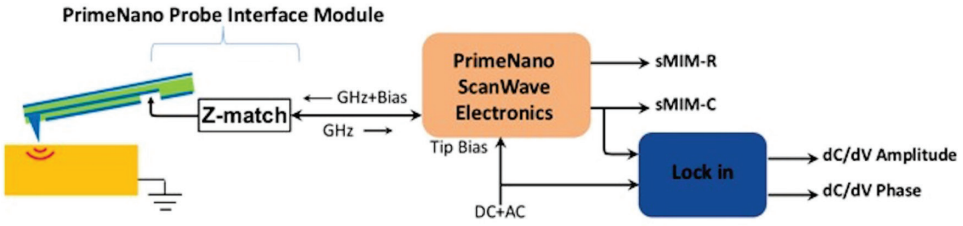


Fig. 1 **Schematic of the PrimeNano ScanWave electronics with a matching circuit and shielded coaxial line to the probe-sample interface**

The natural progression and general interest in the user community is to extend the sMIM capabilities to quantitative measurements. This article presents recent analytical and finite-element modeling developments of tip-bias-dependent depletion-layer geometry and impedance. These are compared to experimental results on reference samples for both silicon- and GaN-doped staircases to systematically validate the response of the sMIM-C channel to the doping concentration.

INTRODUCTION

In a standard sMIM experiment, microwaves are coupled through a custom AFM cantilever to the probe tip, where they interact as evanescent waves with the portion of the sample immediately under the tip. A fraction of the microwaves is reflected, and the amplitude and phase (or equivalently, the real and imaginary parts) of the reflection are determined by the local electrical properties of the sample. For a linear sample (e.g., a dielectric or metallic material), the permittivity and conductivity determine the reflection, while for a nonlinear sample (e.g., a doped semiconductor), the tip-bias-dependent depletion-layer structure contributes significantly. As a result, sMIM measurements can provide valuable nanoscale information about semiconductor devices, processes, and defects.

A custom AFM probe is mounted in a specialized holder so that there is a coaxial connection from the microwave source to the AFM probe tip. The specialized probe module with matching circuit is then fitted to a standard AFM. The AFM typically operates in contact mode for imaging but can also be used in intermittent and tapping modes. The sMIM probes contain a multilayer cantilever with a shielded signal line connecting a contact pad on the carrier chip to the metallic tip at the end of the cantilever. The holder connects to the contact pad and couples 3 GHz microwaves from the sMIM measurement electronics to the AFM probe carrier chip, where they propagate along the signal line in the cantilever to the conductive tip.[15] The reflected signal retraces the same path. This configuration is illustrated schematically in Fig. 1. The probes, probe interface module, and electronics are part of a commercial ScanWave sMIM module (PrimeNano, Inc.). The sMIM is adapted to the most common commercial AFM platforms.[4,5]

The sMIM-C measured on various bulk dielectrics shows a clear linear relationship between sMIM-C and the log of the permittivity.[4,5,16] The red squares shown in Fig. 2 are from a model that originates with a finite-element calculation of the tip-sample admittance for the conical geometry of the sMIM probe. The origins of the log(ε) dependence can be seen in analytical models for spherically terminated conical tips above and in contact with linear materials, documenting the origin of the log dependence published by other researchers.[17]

For sMIM measurements on nonlinear materials, such as a doped semiconductor, the tip-sample bias influences the tip-sample impedance, or, more conveniently, the reciprocal of the tip-sample impedance, the tip-sample admittance, $Y_{T\text{-}S}$. As with linear samples, the sMIM signals are still proportional to the imaginary and real parts of $Y_{T\text{-}S}$, the capacitance and conductance below the tip-sample interface, but the capacitance and conductance now depend not only on the local permittivity and conductivity of the sample under the tip but also on the geometry of

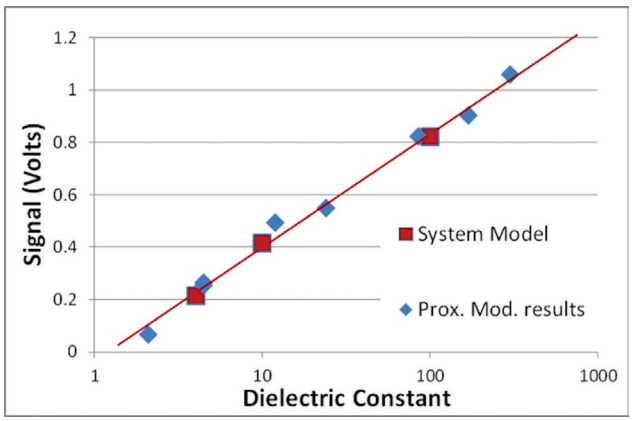


Fig. 2 **Graph of the numerically modeled admittance versus the dielectric value (in red) with the experimentally measured sMIM versus the dielectric value (in blue) from a group of bulk crystal dielectric samples**

the depletion layer. The depletion-layer geometry, in turn, depends on the tip-sample direct current or low-frequency voltage and on the doping level of the semiconductor. Analytical solutions exist for one-dimensional geometries, and these can be used to model the results from macroscopic parallel-plate metal oxide semiconductor (MOS) structures. Figure 3 shows the classic parallel-plate model for describing a MOS device. A lumped-element approximation for an sMIM tip on an oxide-coated semiconductor and expressions from the delta depletion model for depletion-layer thickness[17] are shown in Fig. 3.

Because depletion-layer geometry has a strong impact on sMIM signals and because the depletion-layer geometry varies with tip-sample voltage and with doping, varying the tip-sample voltage is a way to characterize semiconductor materials and devices, particularly the local

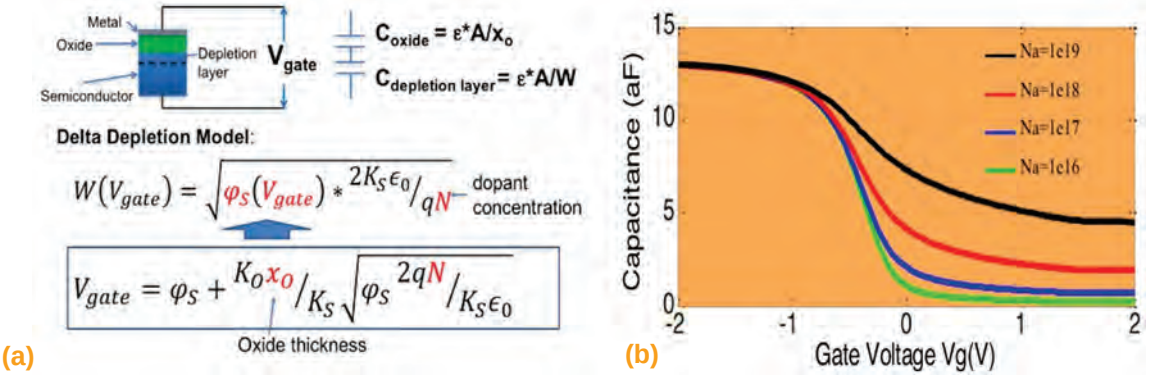


Fig. 3 **(a) Schematic of the classical MOS device configuration with the sMIM probe contacting a sample surface modeled as two series capacitors. The equations describe the relationship of the capacitance (and therefore the sMIM) measurement on the depletion-layer thickness and doping concentration. (b) Numerically generated capacitance-voltage curves from the parallel-plate model illustrate sMIM's sensitivity to semiconductor doping level.**

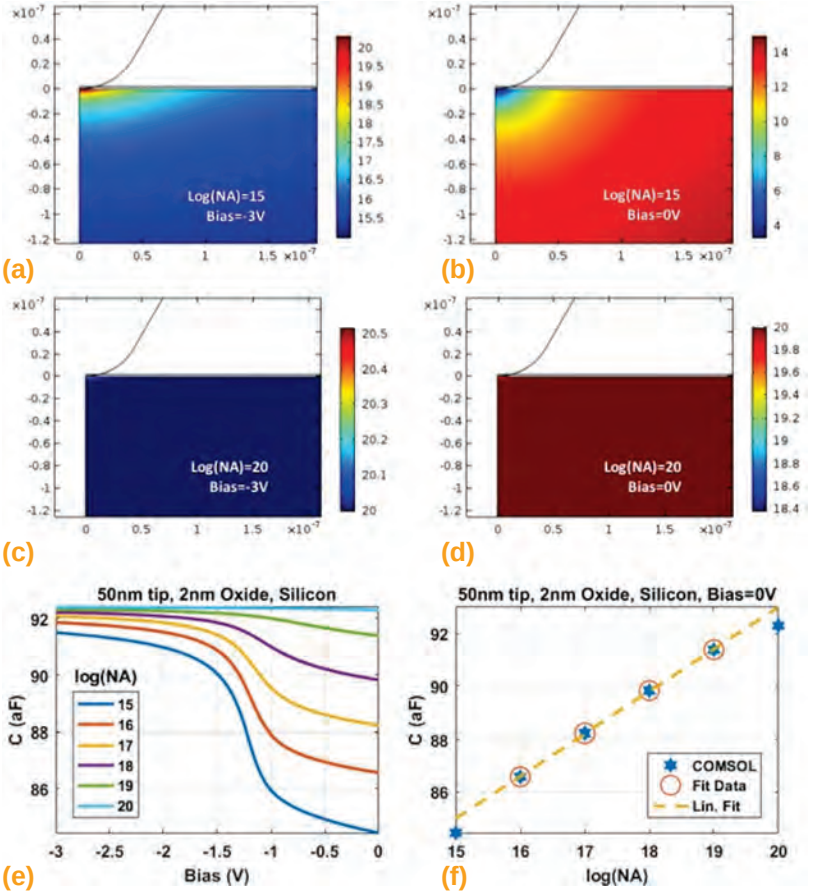


Fig. 4 **(a-d) Finite-element model (FEM) predictions of the majority carrier hole density in the presence of marked biases on an sMIM probe for the marked *p*-type doping densities in silicon. Many more such simulations led to (e) FEM predictions of C-V curves, with the dopings specified by the legend. (f) Calibration of the probe tip's capacitance over the various doped samples as a function of their doping density**

doping level under the tip (or electrode, in the case of patterned samples with electrodes present). This is similar to capacitance-versus-voltage curves from macroscopic samples commonly used to characterize semiconductor materials and test structures. Figure 3(b) presents the classical solution to the parallel-plate model, numerically generated here for a range of doping concentration levels. This model is incomplete for describing the geometries for AFM probe-sample interactions.

Similar to what was observed in the measurements of linear dielectrics shown in Fig. 2, where the sMIM signal is proportional to log(ε), experimental data from doped semiconductors show sMIM signals varying linearly with log([doping concentration]). To confirm the origins of the log([doping concentration]) behavior, finite-element modeling was used to assess the depletion-layer geometry for a conical tip and how this geometry varies for both doping and applied gate (i.e., tip) voltage. Figure 4(a) shows the results for one doping level.

The finite-element models also allow calculation of the tip-sample capacitance for each doping level and gate voltage, resulting in capacitance-voltage (C-V) curves for the geometry of an sMIM probe on an oxide-coated semiconductor (Fig. 4e). Experimental data presented subsequently in this article resemble the model results, indicating that most critical physics are accounted for by the models. Figure 4(f) shows that the capacitance seen and measured by sMIM is linear in log doping over several orders of magnitude for dopings of practical importance, enabling the possibility of calibrating sMIM results to invert for doping density.

EXAMPLES OF sMIM AND C-V ON SILICON SAMPLES

It has been shown in previous work[4,5] that sMIM-C is linear with the log N_A. Results presented in this section show application of sMIM-C's linear relationship to log N_A for quantification of sMIM-C doping concentration in log units. An IMEC *n*-type doped staircase was used as a calibration sample. The IMEC staircase is measured using ScanWave sMIM to determine a calibration curve that can then be applied to an unknown sample to convert sMIM-C to units of doping concentration. Figure 5(a) shows the sMIM-C image of the IMEC staircase doping standard. The sample was measured using a two-pass method with no applied bias. The data are collected line by line; the first line is in contact mode, and the second pass is at a height 100 nm above the sample surface. The difference image is shown in Fig. 5(a). An average profile is shown in Fig. 5(b). The resulting profile shows excellent correlation to the IMEC published doping concentration data. The average profile graph (Fig. 5b) highlights where the average sMIM-C value was calculated for the graph in Fig. 5(c), plotting the measured sMIM-C versus known doping concentration.

Due to the very linear response of the sMIM-C versus log doping concentration, one can use the corresponding

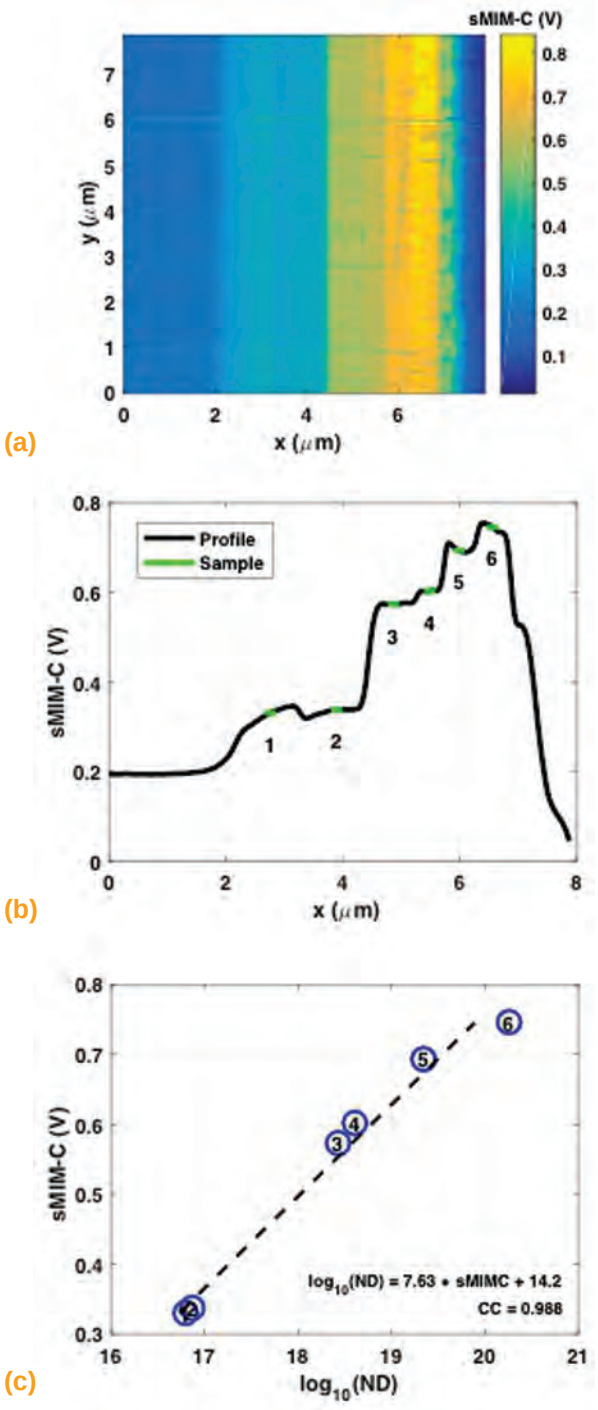


Fig. 5 **(a) Processed sMIM-C image of an *n*-type IMEC staircase. (b) Average profile with "calibration samples" highlighted in green. (c) Plot of sMIM-C calibration values versus published values of log doping. The linear fit is a calibration that can be applied to subsequent unknown doped samples.**

curve (Fig. 5c) as the calibration to convert sMIM-C measured on a device sample to log doping.[10]

Figure 6(a) presents the results of nano-C-V curves from the IMEC staircase, verifying that the nanoscale response matches the theory discussed in the introduction of this article. This "image" is from multiple sMIM scans over the same 8-µm-length line on the sample, collected as the bias voltage scans from 0 to 2.5 V. The demarcations of the doped regions are marked with vertical white lines, separated by exactly the widths of the regions published by IMEC for this sample. The data for the six C-V curves in Fig. 6(b) were taken from the vertical dashed black lines, which are placed exactly midway between the white lines. The C-V curves were shifted so they all have the same sMIM value at the most positive voltage, quite deep into accumulation. These empirical C-V curves for *n*-type silicon closely resemble the mirror images of the theoretical C-V curves for a *p*-type silicon, as they should. (The sMIM-C is proportional to the admittance at the tip/sample interface and therefore to the capacitance.) Figure 6(c) shows the sMIM-C values from the C-V curves in Fig. 6(b) at the tip-sample voltage with the highest doping sensitivity (0.96 V), and they vary linearly with log doping density over approximately 4 orders of magnitude. The derived linear calibration has the formula log(ND) = 1.83 × sMIM-C + 19.9, with a correlation coefficient of 0.972.

sMIM REFERENCE APPLIED TO A GaN DEVICE

This section extends the methods discussed previously on doped silicon systems to III-V semiconductor materials. An *n*-type GaN staircase reference sample was prepared using an *n*-type GaN subtrate and growing four epitaxial layers with varying doping levels. Two of the steps, 2 and 5, have the same doping concentration, as shown in Fig. 7(b). The sample was independently measured using secondary ion mass spectrometry (SIMS) to verify the doped step values, and these values were used for calibration. Figure 7(a) shows the sMIM-C image, with roughly vertical regions representing the individual steps. Using the technique described previously, an average profile of the steps is used to extract the sMIM step value (Fig. 7b), which is then plotted versus log doping to establish the calibration curve (Fig. 7c).

After calculating the calibration curve on the calibration sample, it can now be applied on an "unknown" GaN device to convert the sMIM to units of log doping concentration. The test device is a multilayer structure with both *n*- and *p*-type doped regions. This article concentrates on the *n*-type regions, because the calibration staircase is *n*-type only.

Figure 8(a) shows a cross-sectional schematic of the "unknown" device. The schematic identifies three regions of interest on the sample that are *n*-type doped regions:

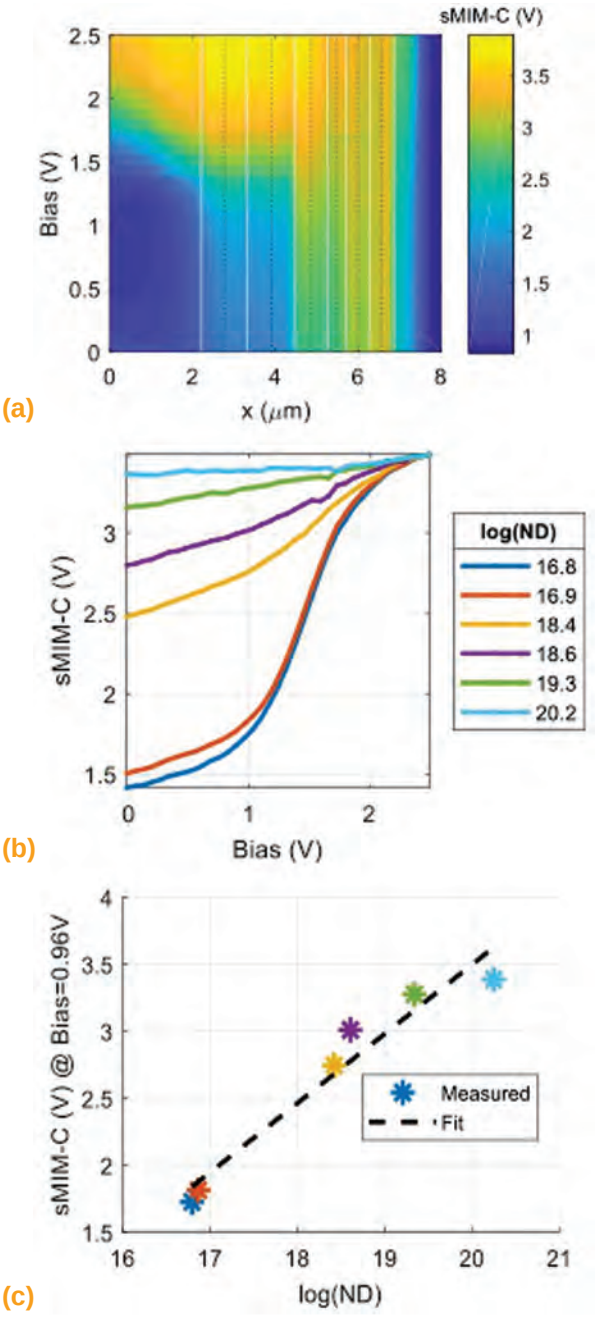
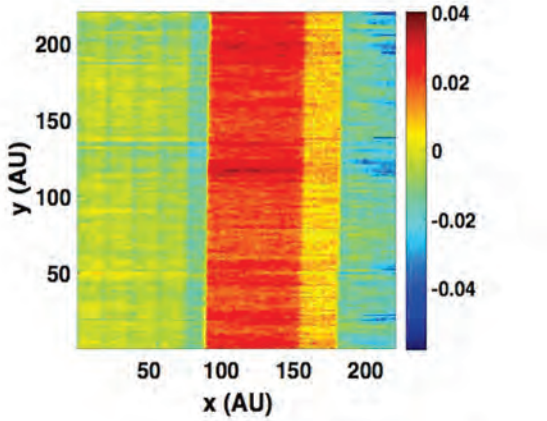
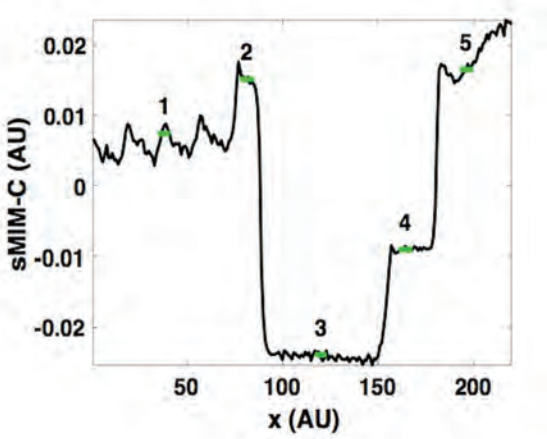


Fig. 6 **(a) Image of an 8 µm line scanned repeatedly while the bias voltage swept from 0 to 2.5 V. The vertical white lines demarcate the doped regions in this cross-sectional sample. The vertical dotted black lines indicate where values were extracted to give C-V curves. (b) C-V curves extracted from (a). The curves have been shifted vertically so they meet at bias = 2.5 V, deep into accumulation. (c) Calibration from sMIM-C to log(ND) at bias = 0.96 V, where sMIM-C has the most doping contrast**

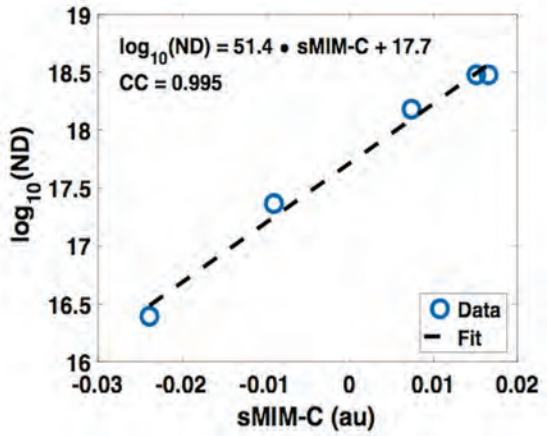
the reference region, L1, and L2. Figure 8(b) shows an sMIM-C image of the "unknown" device. The same three regions of interest are marked with dotted lines and labeled. The image is converted to units of log doping concentration after applying the calibration curve from Fig. 7(c).



(a)



(b)

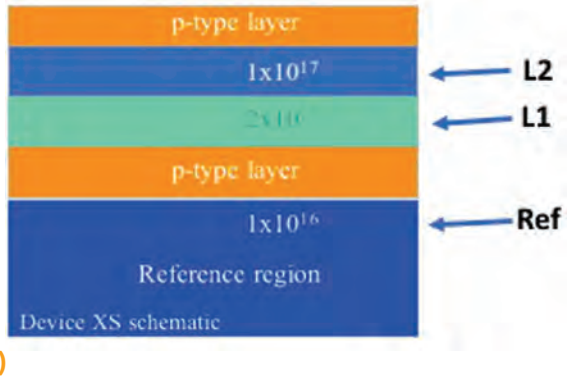


(c)

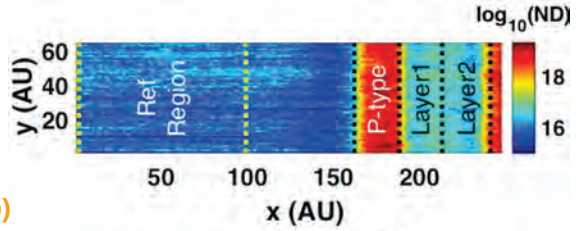
Fig. 7 **Measurement of a GaN epilayer *n*-type doped staircase. (a) sMIM-C image. (b) Average profile of the aligned image, with the highlights showing calibration values. (c) sMIM-C versus doping concentration in log units. The graph shows good linearity over the range of doping and demonstrates the linear relationship of sMIM-C versus log(ND) for a nonsilicon semiconductor material.**

Figure 8(c) is the average profile extracted from the sMIM-C image in Fig. 8(b). The "reference region" of the "unknown" device has the same doping concentration as step 3 of the calibration sample. The common value allows compensation for the potential offsets that may occur due to system drift or systematic errors during the measurements. The calibration curve doping concentration value is shifted to pass through the reference value on the device sample and then applied to the whole profile to calculate doping concentrations.

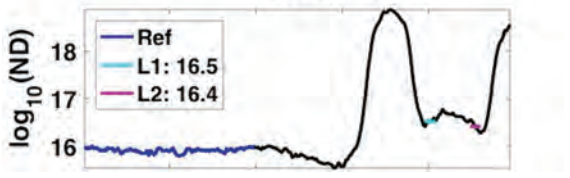
The comparison of the nominal values with the calibrated sMIM values shows that the ratio of L1 to L2 is 2.0 for the SIMS and 1.3 for the sMIM, respectively. The result shows that sMIM is sensitive to the doping concentration difference in the two regions, differing by 0.1 log units. The measured values are lower than the SIMS reference values. The authors speculate that the variation can be caused by



(a)



(b)



(c)

Fig. 8 **(a) Cross-sectional schematic of a GaN device. The sample is labeled with nominal doping values independently obtained by SIMS measurement to verify the nominal doping levels before cross sectioning and measuring with sMIM. (b) sMIM image of the "unknown" sample with color scale converted to *n*-type doping concentration using the calibration data from Fig. 7. (c) Average profile of the sMIM data, where the Ref line is highlighted. The 1×10^{16} region has the same doping concentration as step 3 of the reference sample.**

the difference in measured doping concentration, because SIMS measures the implanted doping density, and sMIM-C measures the activated doping concentration, as well as possible systematic variation during the measurements that could account for the discrepancy. It is expected for GaN that the activated doping concentration would be lower than the implanted density.

The application of sMIM to a cleaved cross-sectional GaN device sample demonstrates the robustness of the method and the flexibility to measure doping levels on an unknown device sample using a known staircase for calibration of III-V materials. Further refinements are ongoing.

SUMMARY

Scanning microwave impedance microscopy as a new mode for electrical measurements integrated to an AFM can address the needs of the semiconductor and failure analysis communities by providing increased sensitivity to investigate semiconductor devices for current and next-generation technologies. Adoption of sMIM will enhance the available toolkit, especially in addressing quantification of doped semiconductors and dielectric materials.

This article presents examples of some of the benefits of the sMIM technology: linear correlation to the log of dielectric coefficient; linear response to the log of doping concentration; visualization of metal, doped materials, and dielectrics in the same image; nanoscale C-V curves; and quantification of doping concentration on different classes of semiconductor materials.

The AFM probes present specific challenges during measurements. This article shows results validating the authors' models with comparison of the classic one-dimensional MOS model with a three-dimensional finite-element analysis cone-shaped model, confirming that using an AFM probe as an electrode for nanoscale C-V curves is different from those acquired with parallel-plate geometry but has similar potential for yielding quantitative characterizations. This article also shows that C-V curves can be measured from doped semiconductors and that they are consistent with what is predicted by theory for this type of three-dimensional geometry.

The article also shows that single-bias images and single-point C-V measurements on an IMEC *n*- and *p*-type doped staircase sample are consistent and therefore can be used together to give an enhanced, quantitative view of a sample's doping state. In addition, it has been shown that sMIM measurements on III-V semiconductor materials and silicon behave very similarly, so methods developed for the latter can be applied to the former; namely, a calibration from a known staircase sample can be applied to the sMIM image of an "unknown" device sample to estimate doping concentrations.

REFERENCES

1. Y. Yang, E.Y. Ma, Y.-T. Cui, A. Haemmerli, K. Lai, W. Kundhikanjana, N. Harjee, B.L. Pruitt, M. Kelly, and Z.-X. Shen: "Shielded Piezoresistive Cantilever Probes for Nanoscale Topography and Electrical Imaging," *J. Micromech. Microeng.,* 2014.
2. N. Duhayon, T. Clarysse, P. Eyben, W. Vandervorst, and L. Hellemans: "Detailed Study of Scanning Capacitance Microscopy on Cross-Sectional and Beveled Junctions," *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct.,* 2002, *20*(2).
3. N. Duhayon, P. Eyben, M. Fouchier, T. Clarysse, W. Vandervorst, D. Álvarez, S. Schoemann, et al.: "Assessing the Performance of Two-Dimensional Dopant Profiling Techniques," *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct.,* 2004, *22*(1).
4. S. Friedman, O. Amster, and Y. Yang, "Recent Advances in Scanning Microwave Impedance Microscopy (sMIM) for Nano-Scale Measurements and Industrial Applications," *Proc. SPIE,* 2014, *9173*, id. 917308.
5. J.R. Matey and J. Blanc: "Scanning Capacitance Microscopy," *J. Appl. Phys.,* 1985, *57*(5), pp. 1437-44.
6. B. Drevniok, St.J. Dixon-Warren, O. Amster, S.L. Friedman, and Y. Yang: "Extending Electrical Scanning Probe Microscopy Measurements of Semiconductor Devices Using Microwave Impedance Microscopy," *Proc. 41st Int. Symp. Test. Fail. Anal. (ISTFA),* 2015, p. 77.
7. Z.Y. Wang et al.: "Evanescent Microwave Probe Measurement of Low-k Dielectric Films," *J. Appl. Phys.,* 2002, *92*, p. 808.
8. E.Y. Ma, M.R. Calvo, J. Wang, B. Lian, M. Mühlbauer, C. Brüne, Y.-T. Cui, et al.: "Unexpected Edge Conduction in Mercury Telluride Quantum Wells under Broken Time-Reversal Symmetry," *Nature Commun.,* 2015.
9. E. Seabron, S. MacLaren, X. Xie, S.V. Rotkin, J.A. Rogers, and W.L. Wilson: "Scanning Probe Microwave Reflectivity of Aligned Single-Walled Carbon Nanotubes: Imaging of Electronic Structure and Quantum Behavior at the Nanoscale," *ACS Nano,* 2015.
10. E.Y. Ma, Y.-T. Cui, K. Ueda, S. Tang, K. Chen, N. Tamura, P.M. Wu, J. Fujioka, Y. Tokura, and Z.-X. Shen: "Mobile Metallic Domain Walls in an All-In-All-Out Magnetic Insulator," *Science,* 2015, *350*(6260), p. 538.
11. A. Tselev, P. Yu, Y. Cao, L.R. Dedon, L.W. Martin, S.V. Kalinin, and P. Maksymovych: "Microwave A.C. Conductivity of Domain Walls in Ferroelectric Thin Film," *Nature Commun.,* May 2016, pp. 1–9, doi:10.1038/ncomms11630.
12. H.P. Huber, I. Humer, M. Hochleitner, M. Fenner, M. Moertelmaier, C. Rankl, A. Imtiaz, et al.: "Calibrated Nanoscale Dopant Profiling Using a Scanning Microwave Microscope," *J. Appl. Phys.,* 2012, *111*(1).
13. St.J. Dixon-Warren and B. Drevniok: "Practical Quantitative Scanning Microwave Impedance Microscopy," *Proc. 42nd Int. Symp. Test. Fail. Anal. (ISTFA),* 2016.
14. W.S. Hu, J.H. Lee, M.H. Kao, H.W. Yang, P. Dewolf, and O. Amster: "Device Dielectric Quality Analysis and Fault Isolation at the Contact Level by Scanning Microwave Impedance Microscopy," *Proc. 42nd Int. Symp. Test. Fail. Anal. (ISTFA),* 2016.
15. Y.L. Yang, K.J. Lai, Q.C. Tang, W. Kundhikanjana, M. Kelly, Z.X. Shen, and X. Li: "A Shielded Cantilever-Tip Microwave Probe for Micro/Nano Surface Imaging of Conductive Properties," *2011 IEEE 24th Int. Conf. Micro Electro Mech. Syst. (MEMS),* 2011.
16. K. Lai, W. Kundhikanjana, M.A. Kelly, and Z.X. Shen: "Calibration of Shielded Microwave Probes Using Bulk Dielectrics," *Appl. Phys. Lett.,* 2008.
17. R. Pierret, *Semiconductor Device Fundamentals,* 2nd ed., Pearson, 1995.

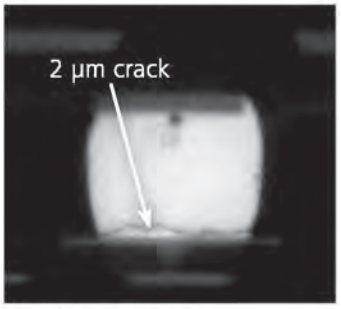
(continued on page 20)

Cross-sectioning without destroying your sample.

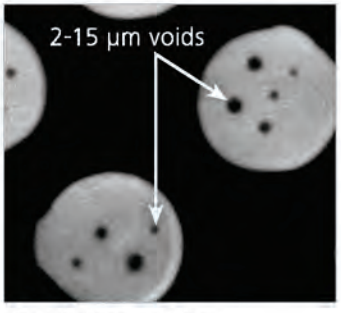
ZEISS Xradia 520 Versa

Visit us at ISTFA booth #725

Image courtesy of AMD Failure Analysis Lab, Singapore



Virtual cross section



Virtual planar section

Identify and visualize failure locations in advanced packaging technologies.

Imagine seeing buried faults in high resolution … non-destructively. ZEISS X-ray microscopes (XRM) provide 3D tomographic data with submicron resolution and contrast for a wide variety of electronics samples, regardless of sample size. With ZEISS XRM, resolution does not degrade as sample sizes increase so whether you are visualizing a 10 mm flip chip package or a 300 mm wafer, you can maintain close to one-micron resolution for any point on your sample.

www.zeiss.com/semiconductor-process-control

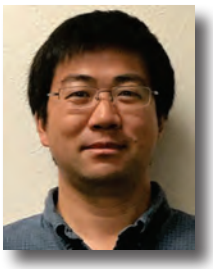
ZEISS

NANOSCALE CAPACITANCE AND CAPACITANCE-VOLTAGE CURVES *(continued from page 18)*

ABOUT THE AUTHORS

Oskar Amster has 20 years of experience working with analytical instruments and metrology tools. His background is in applications development, strategic marketing, and product development. He has extensive experience working in atomic force microscopy, stylus profilers, and optical profiler instruments. Prior to joining PrimeNano, Inc., Oskar was Product Marketing Manager at KLA-Tencor and held positions at Ambios Technology, Ametek Taylor Hobson, Multiprobe, Micron Force Instruments, and Topometrix. He has an M.S. in materials engineering and a B.S. in physics from California Polytechnic State University, San Luis Obispo.

Stuart Friedman has engaged in academic and industrial research in a variety of areas, including image processing, surface science, electron optics, bio-medical instrumentation, and bio-physical simulation. He currently serves as Chief Technology Officer of PrimeNano, Inc., a Silicon Valley instrumentation startup focused on commercial implementation of scanning microwave impedance microscopy for research and commercial applications. Before co-founding PrimeNano, Dr. Friedman founded and led a research and development and systems engineering consulting firm in Silicon Valley, helping transition complex systems to commercial reality for startups as well as Fortune 500 clients. Prior to that, he held research and development, systems architecture, and technical leadership roles at Gatan, Inc., Etec Systems, KLA-Tencor, MDS Sciex, and Signature Bioscience. Dr. Friedman holds a Ph.D. in applied physics from Stanford University, an M.Phil. in physics from Cambridge University, and a B.S.E. in engineering physics from Cornell University.

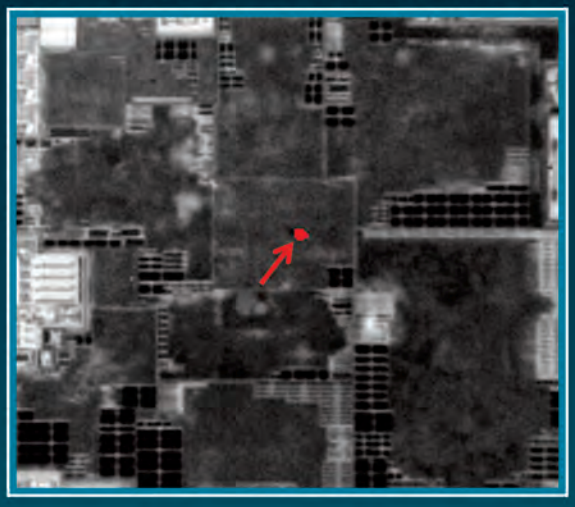


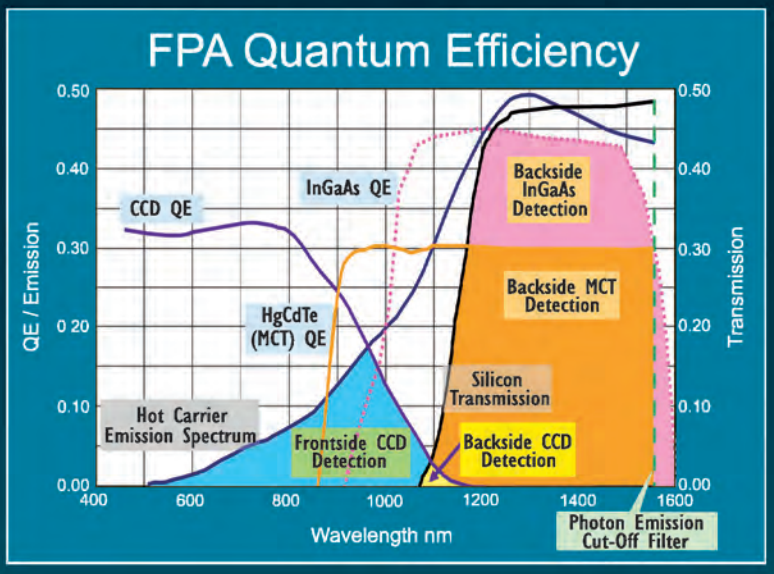
Yongliang Yang has been conducting research on scanning probe microscopy technology for the past five years. He has also spent more than 10 years doing research on MEMS devices. Before joining PrimeNano, Inc. in 2014 as a research and development scientist, Dr. Yang was a postdoctoral student at Stanford University, developing scanning microwave impedance microscopy (sMIM) technology and studying electrical properties of materials with sMIM. Dr. Yang has a B.S. degree from Peking University and a Ph.D. from the Chinese Academy of Sciences. He holds four patents and is the author of more than 40 publications.

Fred Stanke has done research and development of metrology and inspection systems for a wide range of applications. For his Ph.D. dissertation at Stanford University, he developed ultrasonic metrology to nondestructively measure the grain sizes of metals. He did research with Schlumberger Limited on using ultrasound to inspect oil well casings for their capability to provide hydraulic isolation. At the startup Sensys Instruments, Dr. Stanke headed the technical team to develop an optical system using scatterometry to measure the critical dimensions of integrated circuits. He accompanied that product when Tokyo Electron Limited bought it to integrate into semiconductor clean tracks to improve and shorten the control loop for microlithography. At PrimeNano Inc., Dr. Stanke does research and development to allow scanning microwave impedance measurements to quantify properties such as the doping concentrations of semiconductors.

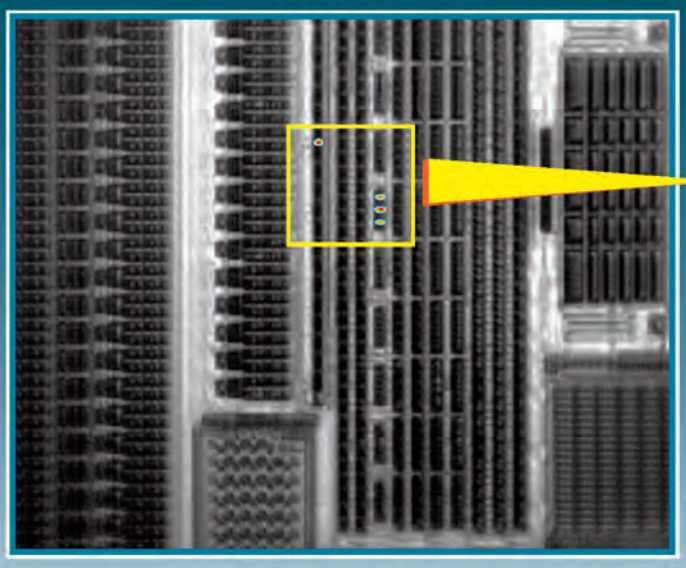
SEMICAPS ARSIL
for
Photon Emission Microscopy (PEM)

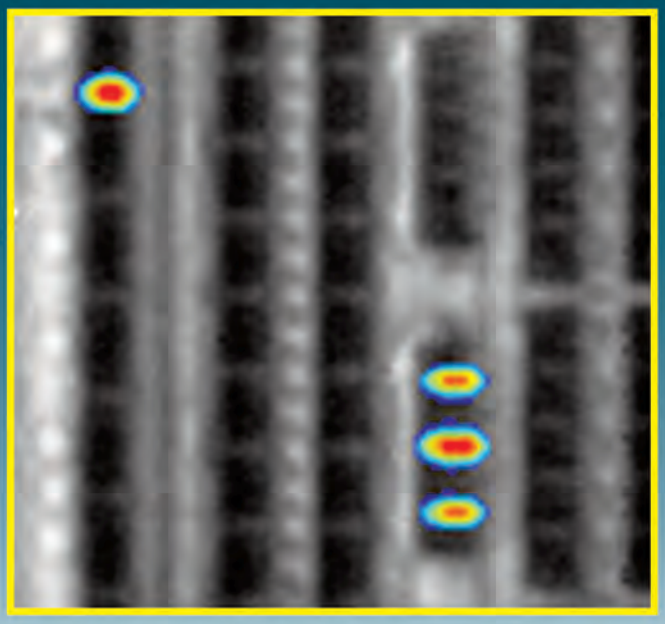
*Backside Emission of Macro Lens





Backside Emission on
SEMICAPS ARSIL





*Microelectronics Reliability Vol 73. June 2017. Pages 76-91

www.semicaps.com
Your Solutions Partner

SEMICAPS
Excellence In Innovation

EDFAAO (2017) 4:22-34

1537-0755/$19.00

PRODUCT CIRCUIT VALIDATION AND FAILURE DEBUG: A SEMICONDUCTOR FOUNDRY CAN HELP

Edy Susanto, S.H. Goh, Edmund C. Manlangit, and Jeffrey Lam
GLOBALFOUNDRIES, Technology Development, Product, Test, and Failure Analysis, Singapore
szuhuat.goh@globalfoundries.com

INTRODUCTION

Before a product enters mass production, a series of design validation and debugging procedures precede as part of the qualification process. Generally, they are broadly classified into simulation-based presilicon validation and postsilicon validation using prototype samples tested under the actual system environment. Despite the painstaking efforts that employ varied simulators and emulators to ensure a clean design tapeout prior to manufacturing, bugs that escape presilicon verification are on the rise[1-3] due to increasing design complexity in modern chips and a widening discrepancy between simulation and actual functional performance as process technologies advance.[4,5] In general, there are two types of design bugs. Logic or functional bugs are caused by design errors or insufficient validation coverage. Electrical or circuit bugs that manifest under certain operating conditions can be caused by design marginalities and process variations. As a statistical reference, it was reported that approximately 2 and 10% of logic and circuit bugs, respectively, were discovered and fixed at postsilicon validation.[1] This situation is expected to be worsened by recent rising trends of third-party intellectual property (IP) modules integration, increasing clock speeds, narrowing design windows due to tightened design rules, and more aggressive production schedules. In addition, there have also been ongoing discussions to enter tapeout early and interrogate the bugs on actual silicon; the justification is a potential shortening of the entire design verification process.[6,7] This explains why postsilicon validation is gaining more traction and why increased efforts are critical to ensure no escapes into production after this final stage of verification.[8-10]

Postsilicon validation encompasses evaluating the functional response of the prototype units per se and their interactions at a system-level platform. Unlike presilicon validation, the tests are usually performed at speed, offering faster lead time. However, this advantage comes at a trade-off of limited observability and intensified debug complexity, because internal nodes cannot be easily assessed and modified on silicon. To achieve debugging, design for testability (DFT) elements such as the IEEE Standard 1149.1 test access port (JTAG),[11] IEEE Standard1687 (IJTAG),[12] and scan-based architecture are leveraged to capture and shift data out of circuit internal nodes.[13] For elusive bugs that only manifest under certain operational time lapse or conditions, a more effective technique is employed that traces internal circuit signals continuously during testing.[14] Although these techniques are well established and efficient, failures in the field, especially related to design marginalities, are inevitable due to shortcomings in test coverage or advanced fault models. Debugging these test escape fails that occur sporadically is challenging but also part of the postsilicon validation process. Over the last decade, the tester-based laser scanning optical microscope tool has been increasingly adopted as an added approach. It is mainly used to debug internal circuit logic and speed paths at large. Some techniques related to such applications are waveform probing of internal nodes[15-18] and logic state mapping.[19]

Fundamentally, be it software- or hardware-based approaches to postsilicon failure debug, an in-depth knowledge of the DFT or design for debug circuitries in the integrated circuit (IC) is requisite. Therefore, it is natural that such activities can only be conducted by design centers and not IC contract manufacturers (foundry). Product time-to-mass-production thus relies solely on the available resources within the design centers to fix the errors.

ROLE OF SEMICONDUCTOR FOUNDRY IN FIRST-SILICON VALIDATION AND FAILURE DEBUG

A semiconductor foundry is strongly motivated by revenue generation to ensure that a design tapeout releases to production from technology development in the shortest possible time. However, besides the advances in design-for-manufacturing efforts to increase the odds of first-silicon success, postsilicon validation and design debug, as a last gate, is usually noncollaborative in nature between design centers and foundries. By tradition, the latter are expected to focus only on process fixes for the reason mentioned in the previous section, while the former assume the responsibilities for design-related matters. Moving forward, the clear demarcation between process or design bugs is becoming more obscured due to the tightening margins in both aspects, and it is time for a paradigm shift for both facilities to step out of their silos and start working together to meet the aggressive schedules for early product time-to-market. Although foundries are not the best candidates to partake in silicon validation entirely, the truth is they can help to some extent, especially with design marginalities, because they often have expertise and toolsets not available to design houses.

One of the most useful tools for identifying design marginalities in ICs is the laser scanning microscope. In most modern foundries, tester-based scanning laser microscope diagnostic tools are readily available for device electrical fault analysis. Automatic test equipment docks onto the diagnostic tool to power up the device while failure analysis is performed concurrently.[20] In this way, functional issues can be interrogated.[21-23] Although the specifications of these tools are capable to apply for design debug, they usually are not utilized for this purpose due to the lack of sufficient design knowledge, such as the expected states at suspected problematic internal nodes. In fact, design centers could leverage this untapped resource for parallel effort in the characterization and root-cause understanding of test failures. This is the first area for collaboration.

The second opportunity for a foundry to contribute is related to debug on the design schematic to postulate the failure mechanism and to guide subsequent failure analysis steps, after the successful localization of suspected problematic circuitries. Often, design centers are relied upon extensively to accomplish this task. Actually, some basic preliminary analysis can be performed by a foundry to shorten the learning cycle. Figure 1 illustrates two examples of abnormal emission hotspot observations after fault isolation. In both cases, a single failing net connecting the signal locations is able to explain the root cause of the failure. In such scenarios, simple layout analyses suffice. For more complicated failure modes,

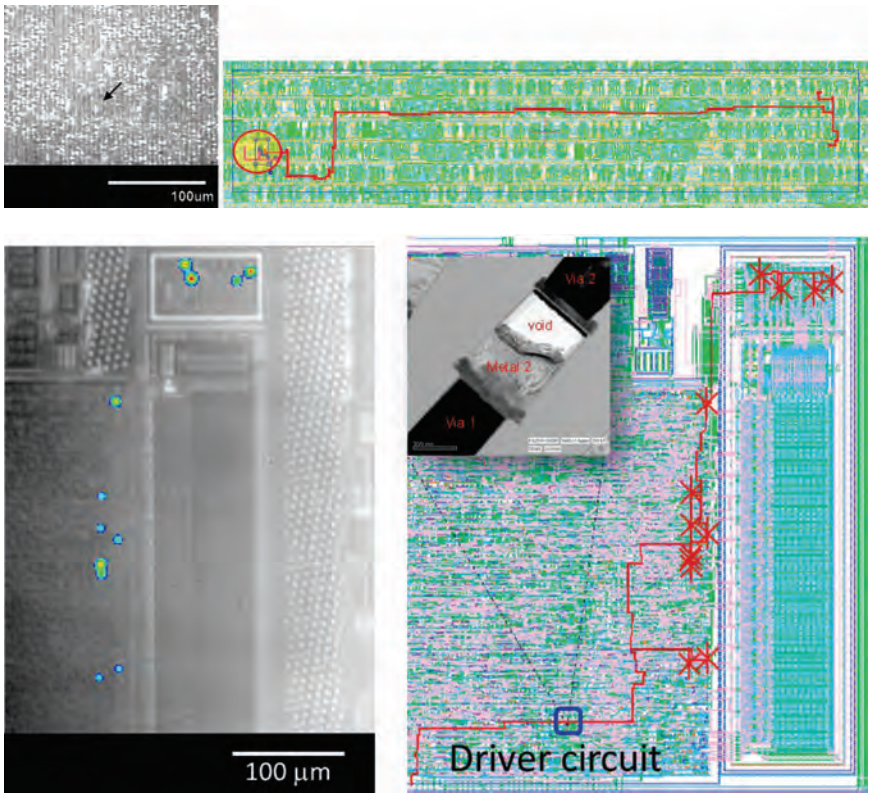


Fig. 1 **Layout trace of suspected failing net connecting (a) single emission hotspot and (b) multiple emission hotspots**

such as multiple emission hotspots that are related by multiple connecting nets and parametric-related issues (Fig. 2a and b, respectively), circuit analysis is necessary.

CIRCUIT ANALYSIS METHODS

Circuit analysis for failure debug is distinctly different from IC reverse engineering that is commonly performed to detect IP infringements or examine chip security. Reverse engineering involves the use of physical methods to remove the materials layer by layer and acquire high-resolution images at each layer for reconstruction of the layout of the entire IP, or even the chip design, and thereafter generate a schematic. Companies and software tools such as Chipworks and Degate have been well established for this purpose.[24-27] Circuit analysis in this article's context refers to examining partial and a much smaller network of circuit components, usually involving one to two levels of fan-in/out net traces that connect the suspected failing instance. In general, this can be accomplished in two ways by the foundry.

MANUAL TRACE

The smallest building block to construct a circuit schematic is a basic transistor. From a layout, it can be extracted based on the overlap of polysilicon and diffusion areas. Subsequently, the connecting nets can be traced to map out the relevant netlist. Although this manual process is tedious and time-consuming, there is no sophistication in the knowledge that is required to accomplish this task. It is fundamental to all semiconductor engineers. Figure 3(a) represents the layout of a typical level-sensitive

(continued on page 26)

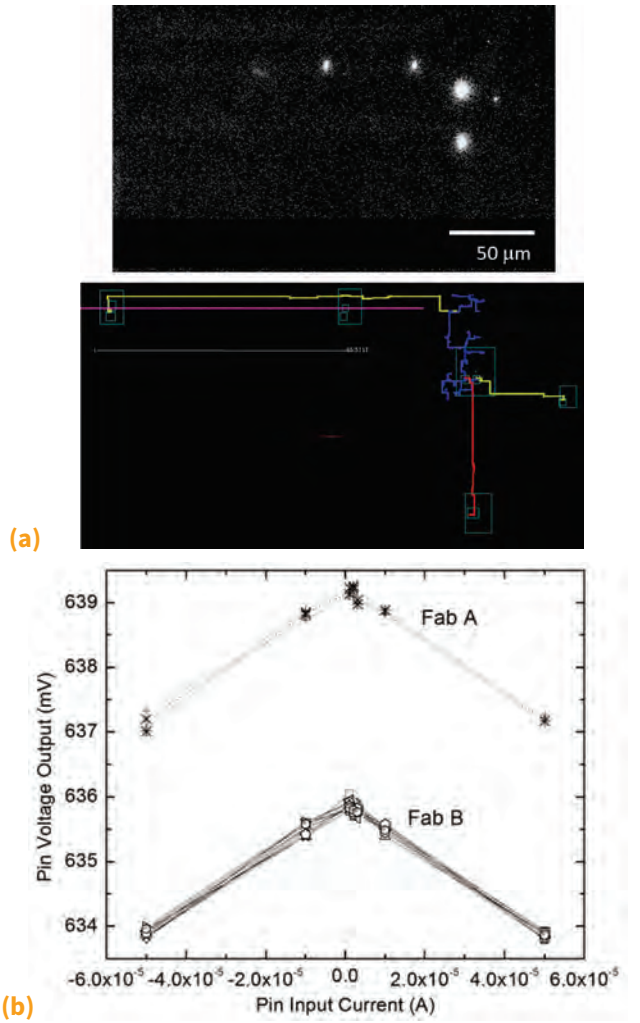


Fig. 2 **(a) Photon emission micrograph showing hotspots not related by a single trace. (b) Parametric test response discrepancies between processed silicon from two foundries**

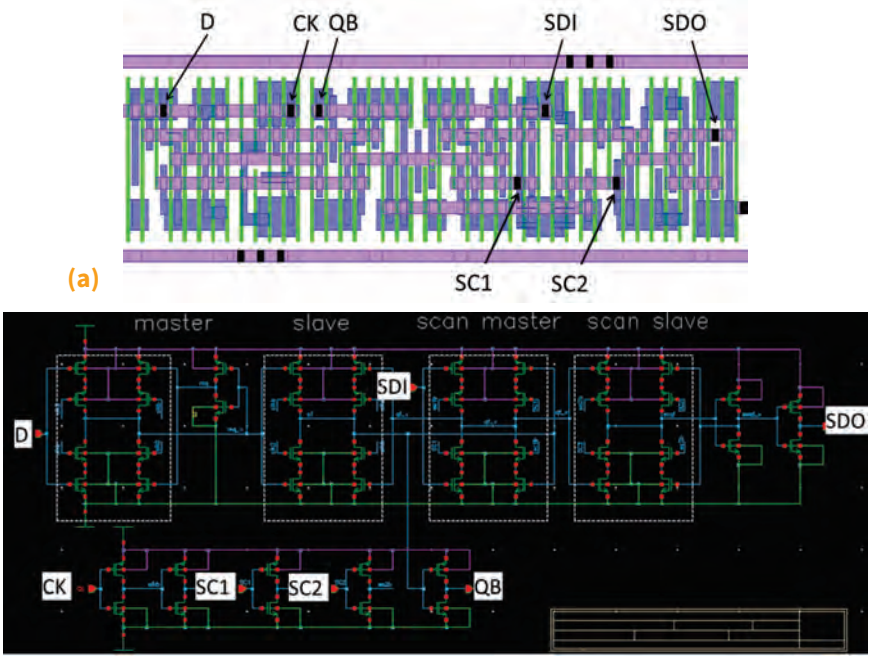


Fig. 3 **(a) Layout representation and (b) corresponding schematic from manual trace of a typical level-sensitive scan flop**

QUARTZ
FOR A FASTER SMARTER LAB

If You Can't Measure It ...You Can't Manage It

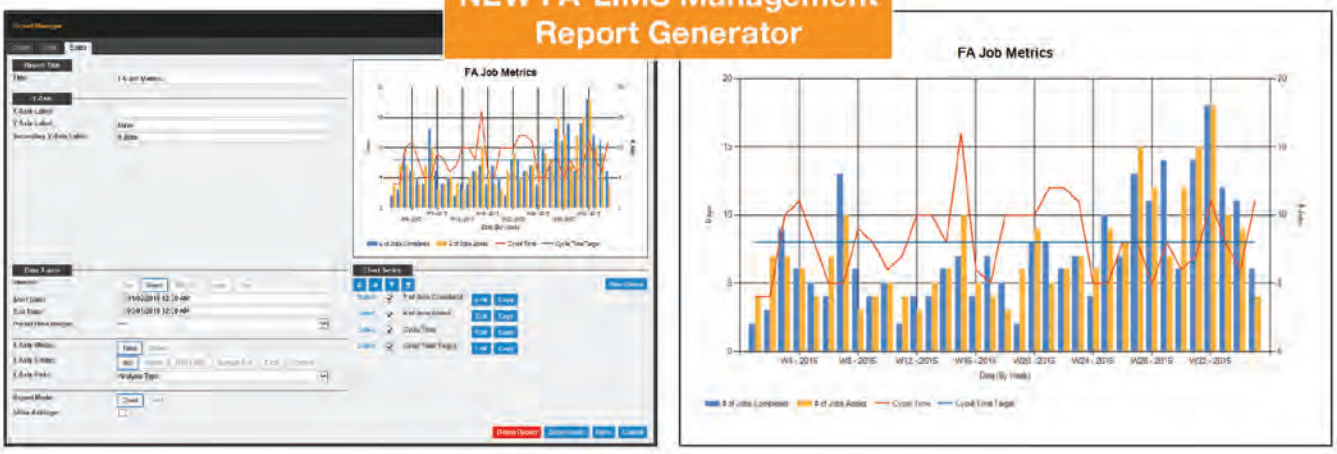
Quartz Laboratory Information Management System for Failure Analysis and Materials Characterization Labs

FA▸LIMS

Do You Really Know How Your Lab Is Performing?

- Where are jobs slowing down?
- How much time does a job really take?
- What resources are holding up jobs?
- Who are the best performers?
- Do I need another tool or more staff?
- What job types are being underestimated?

NEW FA-LIMS Management Report Generator



Want a Faster Smarter Lab?

Increase Lab Productivity by 20%+

CALL US FOR A DEMO

QUARTZ IMAGING CORPORATION

SPECIALIZED SOLUTIONS FOR ELECTRONIC DEVICE LABS

See us at **ISTFA** - Booth **#721**

Phone: 604-488-3911 · inform2@quartzimaging.com · www.quartzimaging.com

PRODUCT CIRCUIT VALIDATION AND FAILURE DEBUG

(continued from page 24)

scan design flip-flop. The corresponding schematic that is derived from manual tracing is shown in Fig. 3(b). A circuit analysis can be performed to shed insight on the bias conditions of the operating modes and the expected performance of the scan cells.

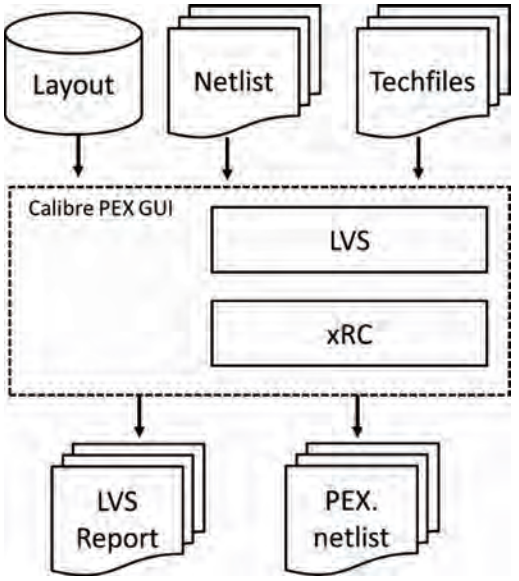


Fig. 4 **Block diagram of a standard Calibre PEX flow**

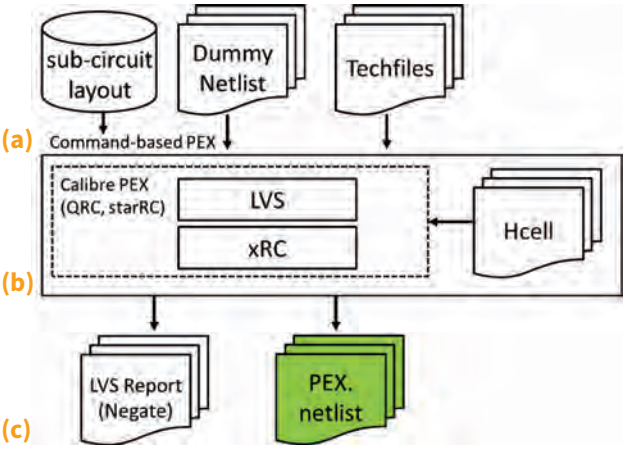


Fig. 5 **Modified Calibre PEX flowchart**

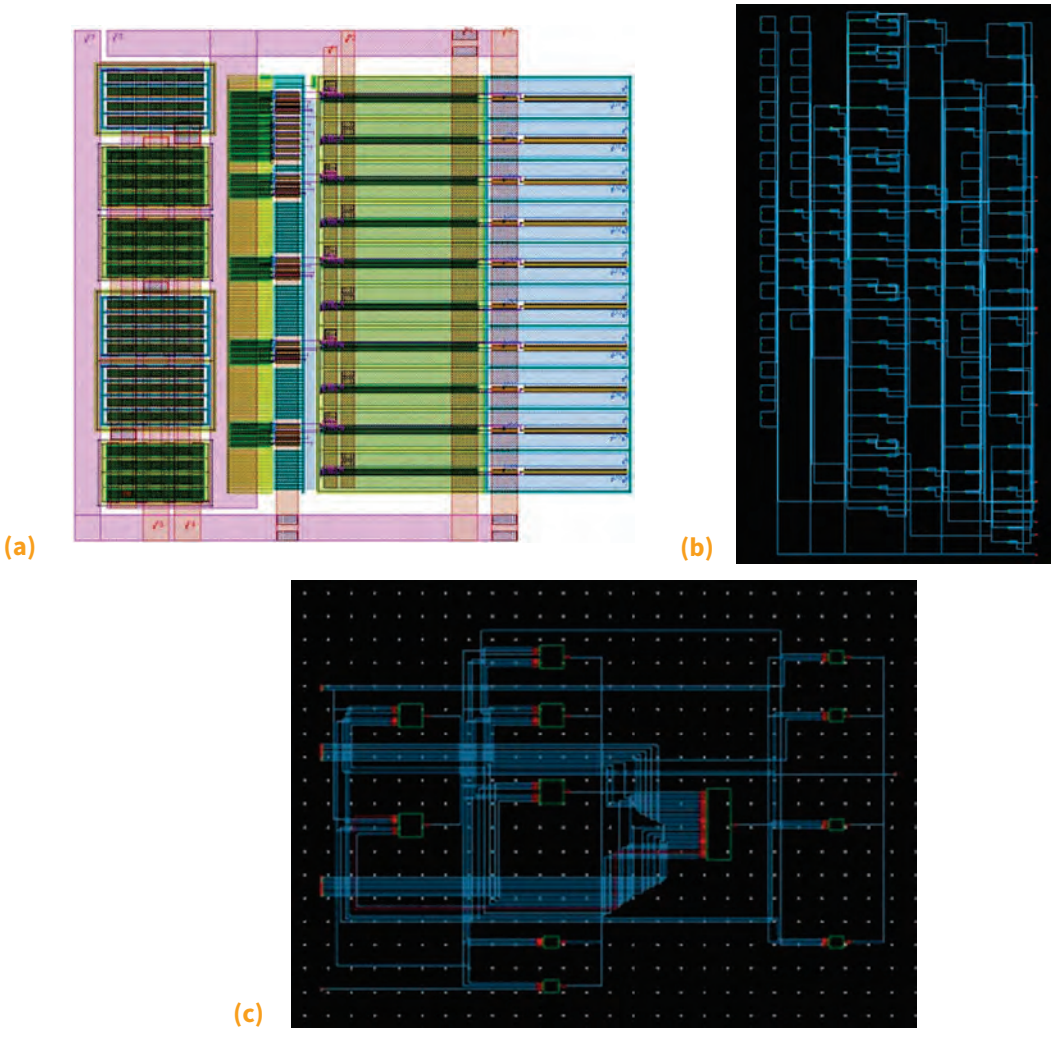


Fig. 6 **(a) Layout, (b) extracted flattened transistor netlist, and (c) hierarchical netlist representation of a generic decoder**

PARASITIC EXTRACTION

A more advanced approach to construct a small-area schematic is to leverage parasitic extraction (PEX), which is a standard procedure as part of the design presilicon validation process. The Mentor Graphics Calibre xRC parasitic extractor[28] is one example, and it is used in this work. Design layout, netlist, and techfiles are the inputs to the tool. Depending on the environment configuration, it is able to execute layout-versus-schematic (LVS) and PEX at the same time. An LVS report together with the parasitic netlist is generated in the process. The LVS compares the extracted transistor-level netlist against the source netlist for discrepancies, and the parasitic capacitances and resistances data can be stitched to achieve an accurate postlayout simulation for verification/debugging. Figure 4 shows a simplified block diagram workflow. For small-circuit schematic extraction, the LVS and parasitic data are not crucial and could be ignored. Figure 5 presents the modified workflow. The design layout is truncated, and a dummy netlist is used as the input file, because no source netlist is available. For hierarchical schematic extraction, a hierarchical cell file is required during the PEX process. In general, Cadence QRC[29] and Synopsys starRC[30] can be used as well.

Figures 6(a) to (c) show the layout of a generic decoder, the corresponding extracted flattened transistor-level netlist, and the hierarchical netlist, respectively. With the PEX netlist, further testbench simulations can be performed (Fig. 7). For the purpose of debug, the circuit of interest can be characterized by assigning sources and sinks to emulate the postulated failing conditions (Fig. 8).

CIRCUIT ANALYSIS ON ELUSIVE PHOTON EMISSIONS

A systematic failure was encountered on first silicon, and photon emission microscopy isolated the problematic

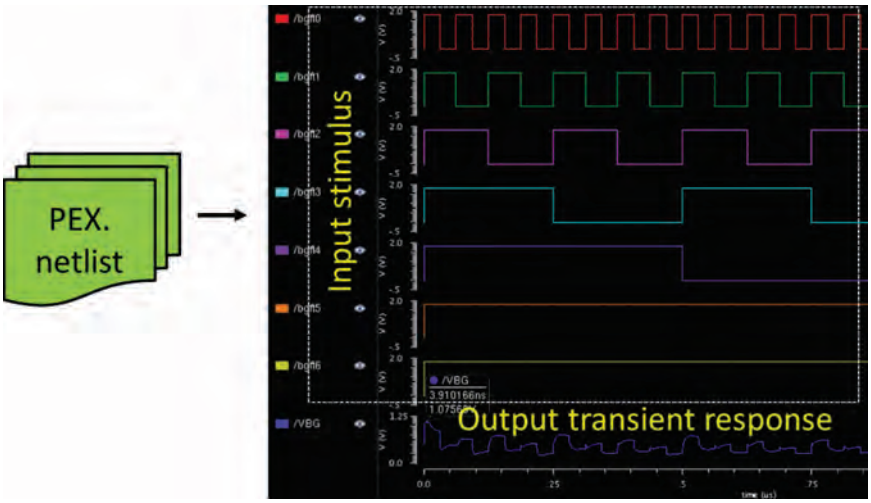


Fig. 7 **Testbench simulation**

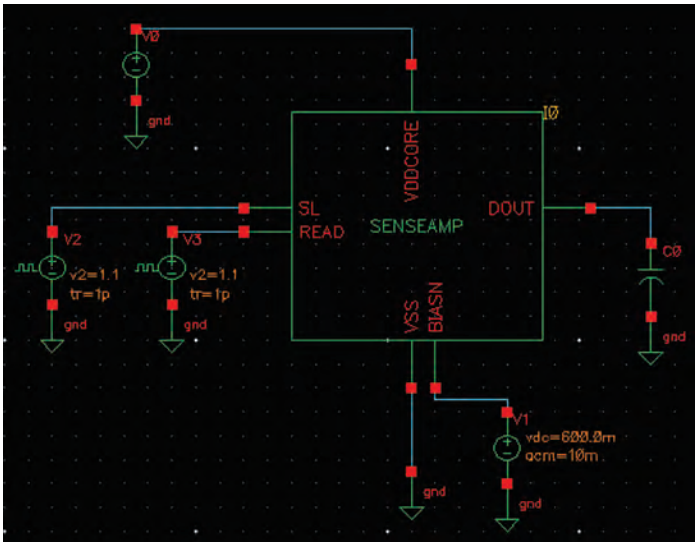


Fig. 8 **Characterization of sense amplifier circuit properties by assigning sources and sinks where appropriate**

circuitry. Next, the schematic was derived using the manual trace method before circuit analysis ensued. Figure 9 shows a schematic of the circuit under debug (CUD) following guidance from the abnormal photon emissions, which were observed on inverter 2 (Inv 2). Inverter 1 (Inv 1) is the preceding instance, while Inverter 3 (Inv 3) is driven by Inv 2. Consider the case of a defect in Inv 1 leading to saturation in Inv 2; intuitively, the input to Inv 3 will be floating, and emissions should be observed as well. Based on experience, direct physical failure analysis on Inv 1 and 2 is not recommended. The inputs A, B, and C to the combinational logic involved in the CUD were identified and a testbench model was created. In the circuit simulation, various combinations to the inputs were applied, and the crossover current of the three inverters was monitored together with the state of the output driving net from Inv 1. The results of two scenarios are presented in Fig. 10. Figure 10(a) shows that when A = 0, B = 1, and C = 0, the driving net to Inv 2 is defined as 0, and the drain current is found to be negligible in all three inverters. However,

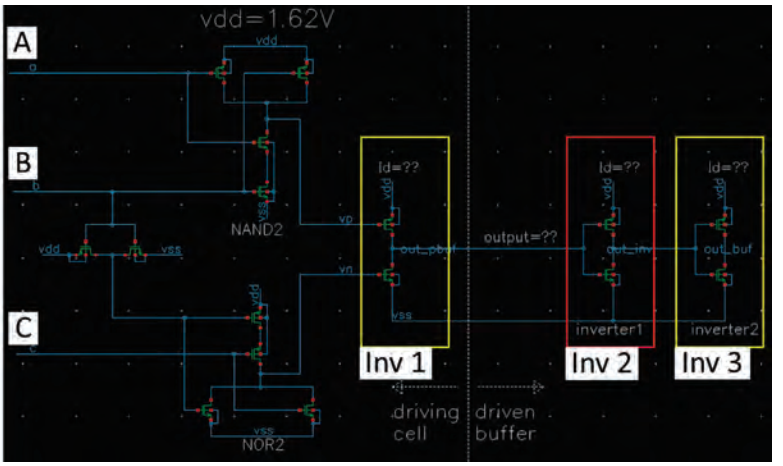


Fig. 9 **Testbench model of CUD. Labels A, B, and C are inputs.**

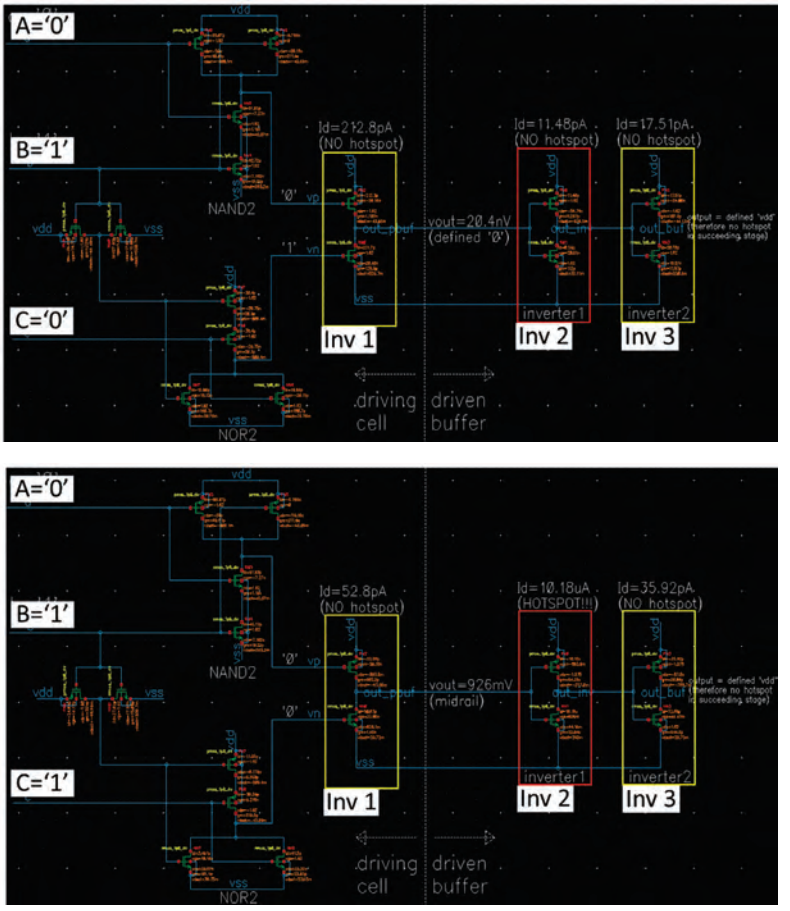


Fig. 10 **Drain current of inverters 1 to 3 under input state of (a) A = 0, B = 1, C = 0 and (b) A = 0, B = 1, C = 1**

when A = 0, B = 1, and C = 1, as shown by the case in Fig. 10(b), the driving net is found to be stuck at midrail bias. The outcome is a leakage in Inv 2, which explains the photon emission micrograph observation. The issue was identified and a process fix was implemented to resolve the failure. Although all nets in a typical combinational logic circuit should be clearly defined, this is a classic example of a design bug escape in presilicon validation. This is a common phenomenon, especially in complex mixed-signal designs.[31]

LAYOUT-DESIGN-RELATED PROCESS SENSITIVITY

Process transfers across wafer fabrication plants (fabs) within a foundry are common to optimize capacity. A case of a consistent higher pin voltage output from a silicon-on-chip from the receiving fab, as shown in Fig. 2(b), is discussed. The test response (voltage readout) presents a negative sensitivity to thermal stimulus. Soft defect localization (SDL) is chosen to isolate the critical circuitries. Figure 11(a) shows the SDL signal overlay image. Five signal spots were obtained, and a layout analysis found them to be related to some contacts of poly resistor chains (Fig. 11b). PEX extraction was performed to derive the schematics of the CUD, and the testbench model is shown in Fig. 11(c). The voltage observation pin as well as the signal locations (area of interest) are indicated. The circuit is a simple potential divider. Figure 12 shows the testbench simulation result. The lowering of the voltage output can be explained by the temperature coefficient

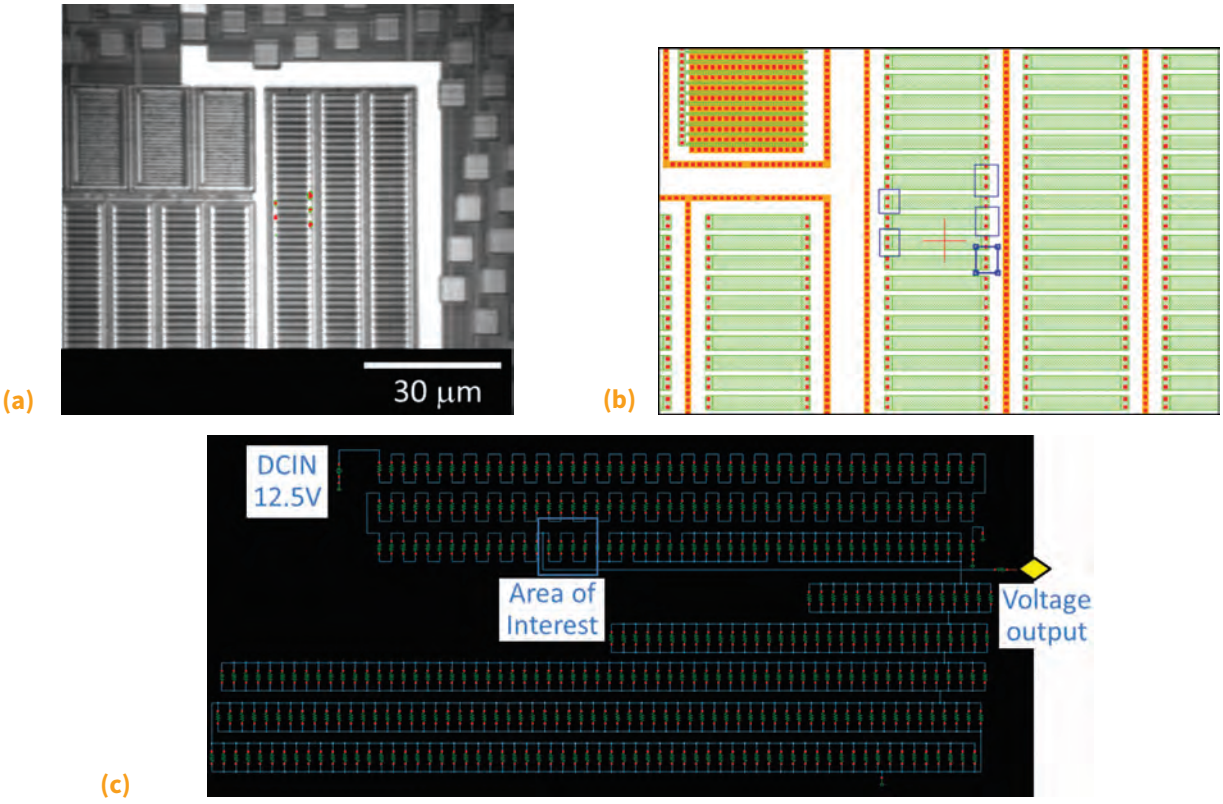


Fig. 11 **(a) SDL signal overlay image and (b) corresponding layout indicating five thermally sensitive sites. (c) Testbench model of CUD**

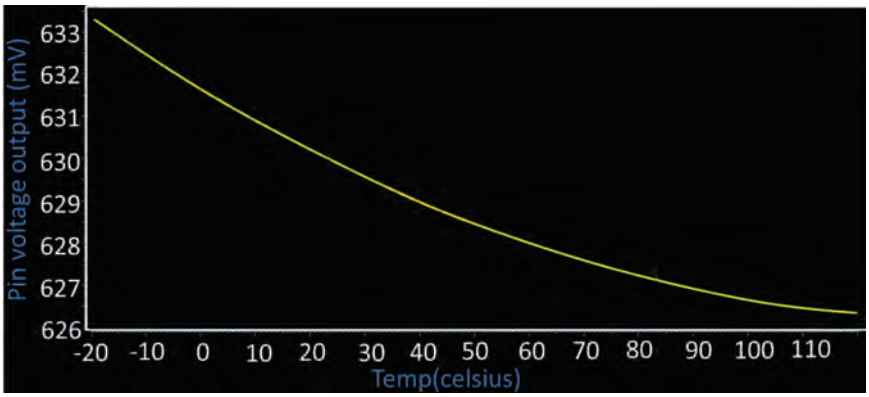


Fig. 12 **Testbench simulation on CUD**

of resistance of the poly resistors. A secondary analysis of the layout reveals that the lower half of the potential divider has a distinctive routing compared to the upper half, which is a straightforward serpentine of discrete resistors in series. The lower half has a combination of resistors connected in series and in parallel. The SDL signals identify the highest-sensitivity region to be on the serial resistors at the lower-half portion of the divider. It is recommended that the routing be consistent on both halves of the divider to mitigate the process sensitivity for better parametric matching.

PEX EXTRACTION CHALLENGES

Although it may seem convenient to generate and study the schematic of the CUD using PEX as compared to manual translation, they are complementary in nature; there are cases where PEX is not effective, as substantiated by Fig. 13. Before any PEX execution, the chip layout is clipped to a smaller region that encompasses the CUD. It includes all process layers within the region of interest, thus leading to multiple transistors that are not directly relevant. An example is dummy transistors. Figure 13(a) shows a cluttered, flattened PEX schematic that cannot be easily interpreted for a reasonable analysis. Figure 13(b) shows the schematic following a post-dummy transistors filtering procedure. Although it may appear manageable, the opportune outcome is to achieve a schematic with not more than three stages from the suspected failing location to minimize the number of intranodes as stimulus and observation points, to facilitate testbench simulations. More work is required to accomplish this, and manual trace is still favored in some situations.

CONCLUSION

There exists a common goal between design houses and foundries: to constantly strive for faster time-to-production of a new product. To accomplish this, first-silicon success or timely issue resolution is paramount. Foundries have an important role to play above their core competence in addressing potential process concerns. This article reinforces the possibility of foundries to engage in preliminary postsilicon validation activities instead of sole reliance on design houses, specifically on design bugs or design-related marginalities failures that are encountered on first silicon. Methods and examples have been presented to demonstrate how foundries can effectively contribute as an added resource to debug such failures. Although the scope is limited to elementary circuitries, the impact exists. In this way, design houses can zero in on more complicated design issues. It is time to revamp the collaboration between design house and foundry. This is just the beginning.

REFERENCES

1. N. Hakim: “Introduction to Post-Silicon Validation,” 2010, eecs.wsu.edu/~rliu1/files/PostSiValidation.pdf.

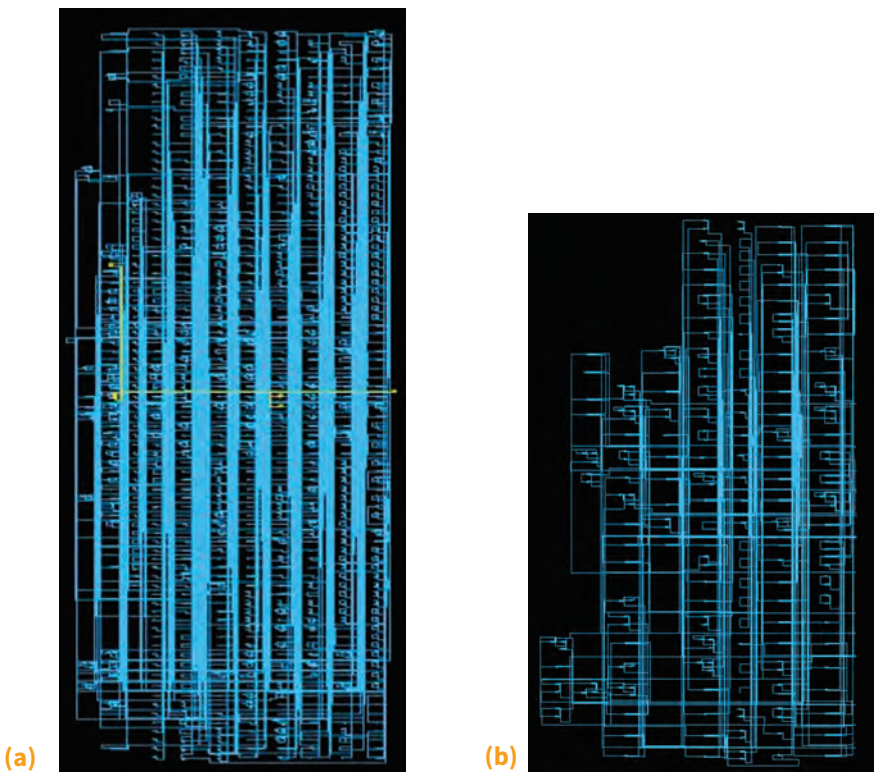


Fig. 13 PEX netlist based on a random clipped layout (a) in the raw form and (b) after filtering dummy transistors

2. V. Bertacco: "Post-Silicon Debugging for Multi-Core Designs," *Proc. Des. Autom. Conf.,* 2010, pp. 255-58.
3. M. Dehbashi and F. Görschwin: "Automated Post-Silicon Debugging of Design Bugs," *Proc. System, Software, SoC, and Silcon Debug Conf.,* 2011, pp. 67-71.
4. T.C. Luo, E. Leong, M.C.T. Chao, P.A. Fisher, and W.H. Chang: "Mask versus Schematic—An Enhanced Design-Verification Flow for First Silicon Success," *Proc. Int. Test Conf. (ITC),* 2010, pp. 1-9.
5. K.L. Yeh, C.S. Chang, and J.C. Guo: "Layout-Dependent Effects on High Frequency Performance and Noise of Sub-40 nm Multi-Finger *n*-Channel and *p*-Channel MOSFETs," *Proc. Microwave Symp. Digest (MTT),* 2012, pp. 1-3.
6. M. Bartley: "The Risks & Rewards of Early Tapeout," *EETimes,* 2014, eetimes.com/author.asp?section_id=36&doc_id=1323158.
7. C. Edward: "Early Tape-Out: Smart Verification or Expensive Mistake?" *Tech Des. Forum,* 2014, techdesignforums.com/practice/technique/tape-out-verification-shift-left.
8. J. Keshava, N. Hakim, and C. Prudvi: "Post-Silicon Validation Challenges: How EDA and Academia Can Help," *Proc. Des. Autom. Conf.,* 2010, pp. 3-7.
9. D. Lin, E. Singh, C. Barrett, and S. Mitra: "A Structured Approach to Post-Silicon Validation and Debug Using Symbolic Quick Error Detection," *Proc. Int. Test Conf. (ITC),* 2015, pp. 1-10.
10. F. Farahmandi, R. Morad, A. Ziv, Z. Nevo, and P. Mishra: "Cost-Effective Analysis of Post-Silicon Functional Coverage Events," *Proc. Des., Autom., Test Eur. Conf. Exhib.,* 2017, pp. 392-97.
11. D. Gizopoulos: *Advances in Electronic Testing: Challenges and Methodologies,* Springer, 2006.
12. B. Eklow and B. Bennetts: "New Techniques for Accessing Embedded Instrumentation: IEEE P1687 (IJTAG)," *Proc. Int. Test Symp.,* 2006, pp. 253-54.
13. B. Vermeulen, T. Waayers, and S.K. Goel: "Core-Based Scan Architecture for Silicon Debug," *Proc. Int. Test Conf. (ITC),* 2002, pp. 638-47.
14. X. Liu and X. Qiang: *Trace-Based Post-Silicon Validation for VLSI Circuits,* Springer, 2014.
15. D. Bockelman et al.: "Multi-Point Probing on 65 nm Silicon Technology Using Static IREM-Based Methodology," *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2005, pp. 40-45.
16. S.Y. Ng et al.: "Laser Voltage Imaging: A New Perspective of Laser Voltage Probing," *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2010, pp. 5-13.
17. M.R. Bruce, L.K. Ross, and C.M. Chua: "On Die Logic Analysis through the Backside," *Proc. Int. Phys. Fail. Anal. Integr. Circuits (IPFA),* 2014, pp. 366-69.
18. W. Lua, G. Ranganathan, V.K. Ravikumar, and A. Phoa: "Combinational Logic Analysis Case Studies Using Laser Voltage Probing," *Proc. Int. Phys. Fail. Anal. Integr. Circuits (IPFA),* 2016, pp. 51-54.
19. B. Niu, G.M.E. Khoo, Y.C.S. Chen, F. Chapman, D. Bockelman, and T. Tong: "Laser Logic State Imaging," *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2014, pp. 65-72.
20. S.H. Goh et al.: "Evolution of Wafer Level Tester-Based Diagnostic System: More than just a Dynamic Electrical Fault Isolation Tool," *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2013, pp. 587-93.
21. S.H. Goh et al.: "Effectiveness of Frequency Mapping on 28 nm Device Broken Scan Chain Failures," *Rev. Sci. Instrum.,* 2012, *83*(2), p. 023702.
22. S.H. Goh et al.: "Wafer-Level Fault Isolation Approach to Debug Integrated Circuits JTAG Failures," *Proc. Int. Phys. Fail. Anal. Integr. Circuits (IPFA),* 2014, pp. 30-34.
23. B.L. Yeoh, S.H. Goh, et al.: "Debugging MBIST Hard Fails without Bitmapping," *Proc. Int. Phys. Fail. Anal. Integr. Circuits (IPFA),* 2015, pp. 138-43.
24. "Reverse Engineering Software," Chipworks, chipworks.com/en/technical-competitive-analysis/resources/ reverse-engineering-software, accessed May 2014.
25. Degate, degate.org/documentation.
26. M. El Massad, S. Garg, and M.V. Tripunitara: "Integrated Circuit (IC) Decamouflaging: Reverse Engineering Camouflaged ICs within Minutes," *Proc. Network Distrib. Syst. Security (NDSS) Symp.,* 2015.
27. K.Y. Kenneth and C.N. Berglund: Automated System for Extracting Design and Layout Information from an Integrated Circuit, U.S. Patent 5,086,477, 1992.
28. "Calibre xRC Parasitic Extraction," Datasheet, Mentor Graphics, 2004.
29. QRC, *Extraction User Manual,* Version 11, Cadence, 2015, p. 1.
30. "Extraction Techniques for High-Performance, High-Capacity Simulation," Synopsys, 2009.
31. Dolphin Integration, "Analog & Mixed Signal IC Debug: A High Precision ADC Application," *2017 Design and Reuse,* https://www.design-reuse.com/articles/19575/analogmixed-signal-ic-debug.html.

ABOUT THE AUTHORS

Edy Susanto received his M.Sc. degree in IC design from Nanyang Technological University. He joined Philips Semiconductors, later NXP Semiconductors, and ST-Ericsson as an analog IC design engineer focusing on universal serial bus transceiver design and later communication combo chips with FM radio, Bluetooth, wireless local area network, and near-field communication applications. He joined GLOBALFOUNDRIES in 2013, where he is responsible for process integration and has subsequently ventured into product diagnostics for CMOS, MEMS, and silicon photonics products. Edy has vast experience in the semiconductor industry, including design, verification, validation, process, electrical test, process control modules, and product testing. He takes great interest in leveraging his immense experience to enhance yield ramping in the foundry.

Szu Huat Goh received his B.Eng. and Ph.D. degrees in electrical and computer engineering from the National University of Singapore. Dr. Goh is currently with GLOBALFOUNDRIES' Product, Test, and Failure Analysis Division in Singapore, where he leads a team responsible for product failure diagnostics and advanced methodologies to accelerate yield ramp. His main focus is the development of dynamic fault isolation techniques, wafer-level fault isolation methods, and leveraging cross-functional domain knowledge of design, test, and failure analysis to enhance yield learning.

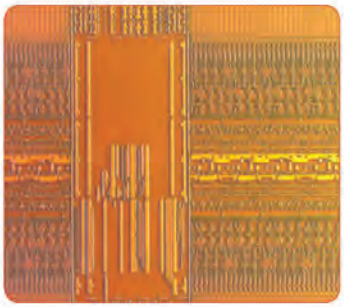
(continued on page 34)

MultiPrep™ System

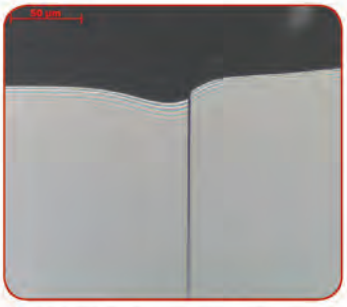
The **MultiPrep™ System** enables precise semiautomatic sample preparation of a wide range of materials for microscopic (optical, SEM, FIB, TEM, AFM, etc.) evaluation.

Capabilities include parallel polishing, angle polishing, site-specific polishing or any combination thereof. It provides reproducible results by eliminating inconsistencies between users, regardless of their skill.

Unequalled Sample P

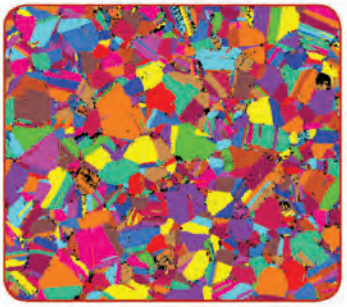


IC Delayering



TEM Preparation

Cross-Sectioning



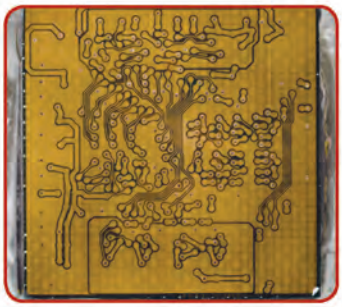
EBSD Preparation

Advancing Technology Through Sample Prep

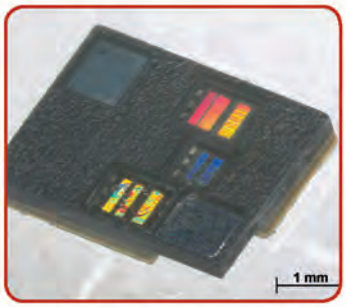
X-PREP®

The **X-Prep®** is a specialized 5-axis CNC-based milling/grinding/polishing machine designed to support electrical and physical failure analysis techniques and other applications through high precision sample preparation. This easy-to-use, highly versatile system is capable of working with flat (2D) and convex/concave (3D) device profiles, providing unmatched precision and accuracy.

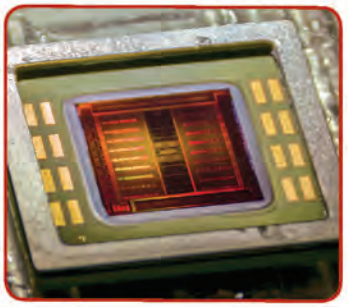
reparation Results



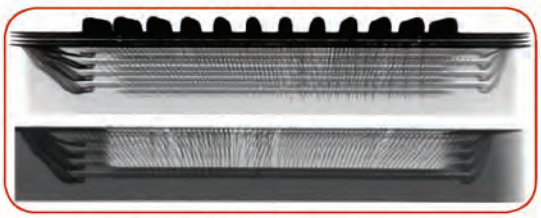
Uniform Substrate Delayering



Open areas as small as 100 x 100 µm



Visible & IR SIL Applications



Stacked Die Deprocessing

ALLIED
HIGH TECH PRODUCTS, INC.

paration

800.675.1118 US/Canada
310.635.2466 Worldwide
info@alliedhightech.com
www.alliedhightech.com

PRODUCT CIRCUIT VALIDATION AND FAILURE DEBUG *(continued from page 31)*

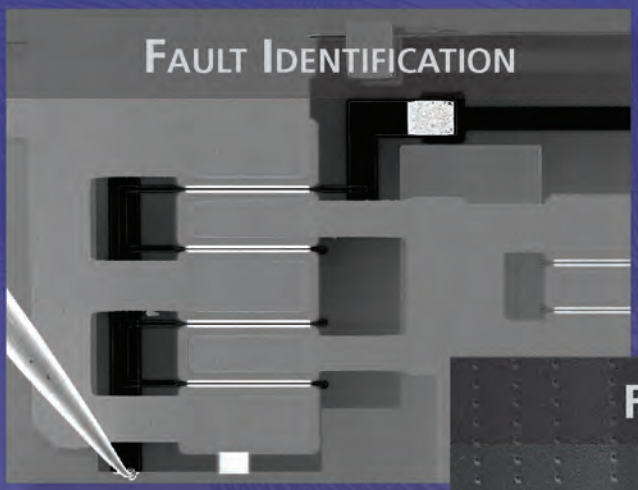
His work has been published in conference proceedings and journals. He was the technical program chair and general co-chair for the IPFA conference in 2016 and 2017. Dr. Goh also contributes actively in technical committees for the ISTFA and SEMICON Southeast Asia conferences.

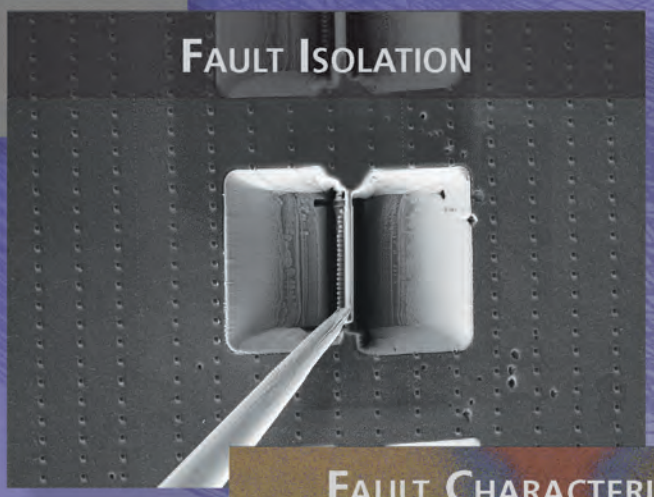
Edmund C. Manlangit received his B.S. and M.S. degrees in electrical engineering (microelectronics option) from the University of the Philippines in 2004 and 2007, respectively. In 2007, he joined Intel Technologies Philippines as an IC design engineer in the flash memory group. In 2011, he moved to Singapore and joined ST-Ericsson (eventually acquired by Intel Singapore) as a senior analog/radio-frequency design engineer for the near-field communication and global navigation satellite system development group. His research interests are in the low-power design of analog and radio-frequency front-end internet protocols. He is currently employed as a principal engineer at GLOBALFOUNDRIES, Singapore, where he does product diagnostic and debugging (IC layout and circuit analysis).

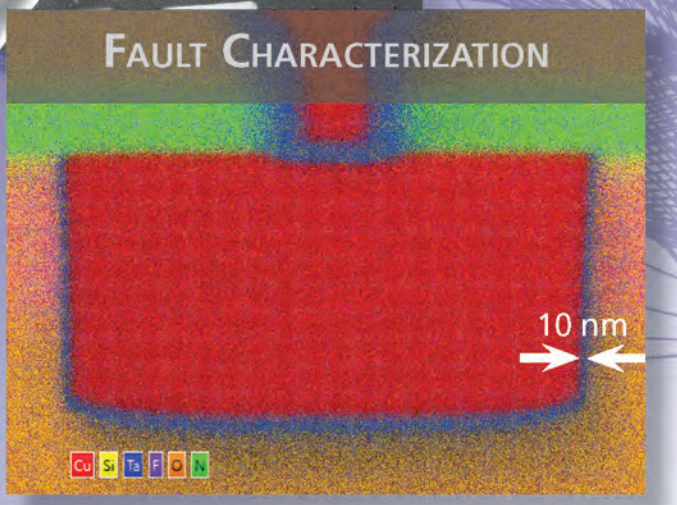
Jeffrey Lam received his B.S. and M.S. degrees in chemical engineering from the University of California, Berkeley and the University of California, Davis in 1979 and 1981, respectively. He obtained a second M.S. degree in electrical engineering and computer science from the University of Santa Clara in 1986. In 2014, he received his Ph.D. from the school of mathematics and physics at Nanyang Technological University. Dr. Lam is currently a vice-president at GLOBALFOUNDRIES, Singapore, where he is in charge of the Product/Test and Yield Engineering Department in technology development. He has more than 35 years of experience in FA, design, product/yield engineering, and test development. Dr. Lam holds 7 technical patents and has more than 20 publications. He has also been the chairman of the SEMI SGP Product and Test Committee since 2009, and he is an adjunct associate professor at the National University of Singapore.

FAILURE ANALYSIS

Full failure analysis solutions in a FIB-SEM







Current generation smartphone CPU. Image courtesy MSS Corp.

Fault identification
EBIC & EBAC with **OmniProbe®**

Fault isolation
Advanced lamella preparation workflows

Fault characterization
Sub 10 nm chemical imaging on bulk and thin samples using **Ultim® Extreme**

Visit us at ISTFA.
Booth 521.

Learn about our failure analysis workflow
www.oxinst.com/failureanalysis

OXFORD INSTRUMENTS

EDFAAO (2017) 4:36-44 1537-0755/$19.00

PLASMA FIB DEPROCESSING OF INTEGRATED CIRCUITS FROM THE BACKSIDE

E.L. Principe[1], Navid Asadizanjani[2], Domenic Forte[2], Mark Tehranipoor[2], Robert Chivas[3], Michael DiBattista[3], and Scott Silverman[3]
[1]Synchrotron Research, Inc., Melbourne Beach, Fla.
[2]Florida Institute for Cybersecurity, University of Florida, Gainesville, Fla.
[3]Varioscale Inc., San Marcos, Calif.
eprincipe@synchres.com

INTRODUCTION

Deprocessing of integrated circuits (ICs) is often the final step for defect validation in failure analysis (FA) cases with limited fault-isolation information and is an essential process for reverse engineering for design verification and competitive analysis. State-of-the-art methods include expert hand polishing, selected area milling, and focused ion beam deprocessing. These techniques struggle to maintain a high success rate as semiconductor process nodes scale down due to the increased number of layers, a reduction in dielectric thickness, adoption of porous low-k dielectrics, increased IC density, and smaller metal interconnect features. Large-area delayering has recently advanced via plasma-source focused ion beam-scanning electron microscopy (FIB-SEM) deprocessing that couples high currents over large areas with new chemistries, providing superior control and homogeneous material removal of heterogeneous materials in ICs, notably copper interconnects and porous silicon-based dielectrics.

A new concept, based on plasma FIB deprocessing of devices from the silicon substrate backside, is now introduced to enable a greater success rate on lower-metal interconnects and high-density transistor levels. A comparison is shown between plasma FIB deprocessing from the interconnect side (frontside) and the backside deprocessing approach, using samples ultrathinned in the packaged device. Ultrathinning the silicon substrate significantly reduces the amount of time required and provides an even starting surface for deprocessing, making it possible to image most dense lower layers first while the sample is uniform and enabling larger volumes of the IC to be deprocessed with increased success rate, resolution, and uniformity. Automated backside thinning followed by plasma FIB deprocessing integrates with the typical workflow, which includes nondestructive evaluation via optical imaging and x-ray computed tomography (CT) scanning.

X-RAY CT SCANNING

X-ray tomography is a nondestructive process to visualize the internal structure of an object, and it is often completed on an IC device prior to any mechanical, charged particle, or chemical deprocessing. The principle of tomography is based on a well-known method of acquiring a stack of 2-D images from different angles and using mathematical algorithms to reconstruct the 3-D model. The typical role of lab-based x-ray CT systems in FA and reverse engineering is to provide connectivity information on the printed circuit board (PCB) level and packaging components.[1-5] Synchrotron-based x-ray tomography can improve on the spatial resolution of lab-based x-ray tomography tools and has been applied to extract interconnect and trace data corresponding to 14 nm node technology.[6] However, at present no singular x-ray tomography system, in a lab or in a synchrotron facility, has sufficient spatial resolution to extract IC structural and component detail at the finest scales corresponding to 10 nm or throughout the entire volume of a 1 cm^2 die. Therefore, x-ray methods alone may not be relied on to nondestructively reconstruct the entire architecture of

This article was presented at the Washington, D.C.-area 10th Annual FIB SEM Workshop, National Institute of Standards and Technology (NIST), Gaithersburg, Md., March 2, 2017.

modern IC devices, and SEM imaging is relied on to provide the spatial resolution required to resolve features at the finest scale. Despite the shortcomings of synchrotron-based x-ray 3-D imaging in terms of spatial resolution and accessible volume, this method has played an important role in the evolution of x-ray-based techniques to "non-destructively" analyze ICs and to extract interconnect and trace data as well as material composition information.[7] The Intelligence Advanced Research Projects Activity (IARPA) has issued a challenge through its Rapid Analysis of Various Emerging Nanoelectronics (RAVEN) program to extend the capabilities of nondestructive and destructive techniques to enable the complete deprocessing of a modern IC device across an entire 1cm^2 die within a span of 25 days at a target resolution of 10 nm using a lab-based tool.[8] BAE Systems and its partners have taken on this challenge and are developing a tool that combines high-resolution x-ray CT tomography (X-Mode) using transition-edge sensors with ultrahigh-resolution SEM (E-Mode) on backside-thinned devices.[9] Such a hybrid approach—using electron microscopy to obtain high-resolution imaging data from the backside, where the density is highest and the structures are of the finest scale, combined with novel x-ray tomography in one laboratory-based tool—may become a key component to a deprocessing tool suite in the near future. It is conceivable that gas-assisted delayering technologies in combination with other charged particle beams could be woven into such a system to permit in situ delayering. Regardless, x-ray CT imaging technology will remain a key component to nondestructive characterization, FA, and reverse engineering. The image panel in Fig. 1 illustrates three individual *X-Z* image frames representing part of the complete image series used to reconstruct the device volume. The data were acquired on a Bruker Skyscan 2211.

AUTOMATED BACKSIDE THINNING

Automated backside thinning represents a critical advance to enable the most versatile deprocessing work flow. The technology required to achieve automated backside thinning to within 1 to 3 µm of the active silicon is no small feat. It should be appreciated that a silicon die is never perfectly flat, and regardless whether it remains in the package or is extracted, it is subject to complex strain and deformation induced by thermal expansion and mechanical constraints. Moreover, during the thinning process there is relaxation and sag; therefore, it is necessary to continuously monitor both shape and thickness. This dynamic process requires precision laser monitoring coupled to feedback driving an adaptive five-axis computer numerical control (CNC) multitool. The tooling combines both grinding and polishing with a floating tool head that follows the contoured surface of the die during the process, as schematically represented in Fig. 2.

Through this automated process, an initial wafer thickness of 775 µm was thinned using the VarioMill by Varioscale, which combined automated grinding and polishing processes to achieve a final residual thickness between 1 and 2 µm across the entire die. In the case of the AMD Opteron processor, the die size is 18 × 16 mm. The residual backside silicon is sufficiently thin that it is possible to image into the active silicon and reveal the

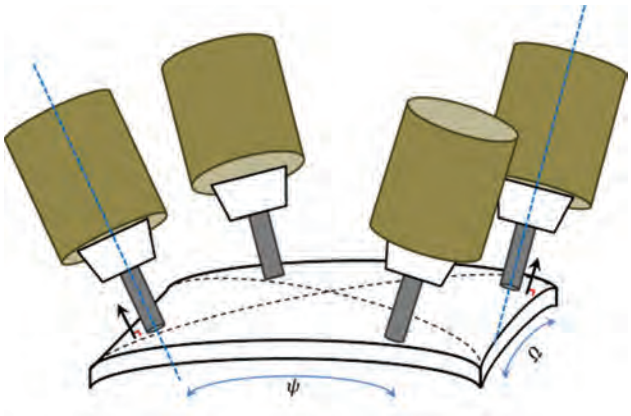


Fig. 2 **Schematic representation of adaptive CNC five-axis machining tool head to follow the evolving shape and thickness during mechanical backside thinning**

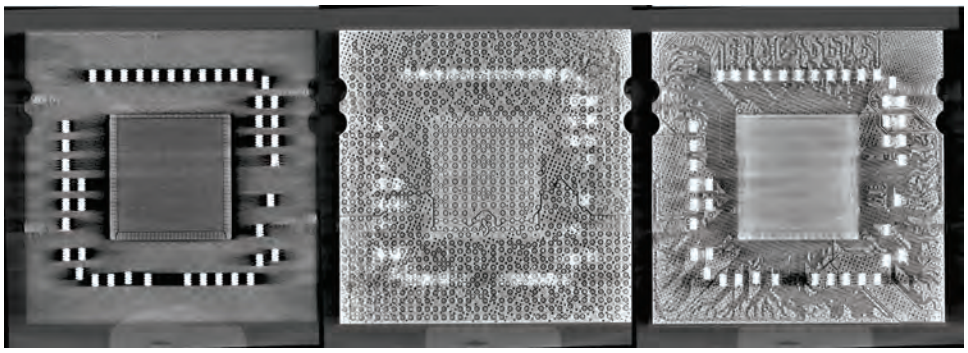


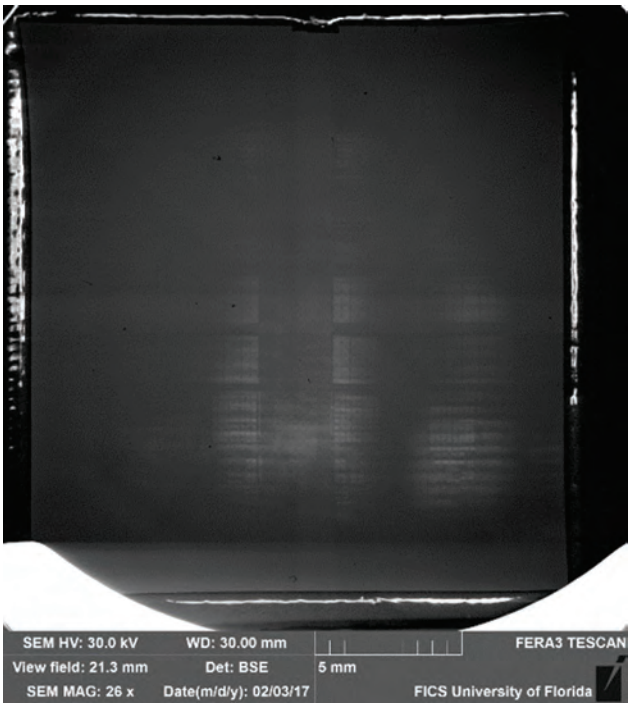
Fig. 1 **Three image panels from the complete dataset series from the x-ray tomogram of an AMD Opteron chip. The x-ray CT data form the volumetric boundary of the device and provide connectivity at the level of the PCB.**

device structure via backscattered electron (BSE) imaging within the electron microscope (Fig. 3). At this stage, the sample is prepared for further deprocessing through gas-assisted etching (GAE) and delayering in the plasma FIB. The plasma FIB delayering was completed in a FERA3 by Tescan.

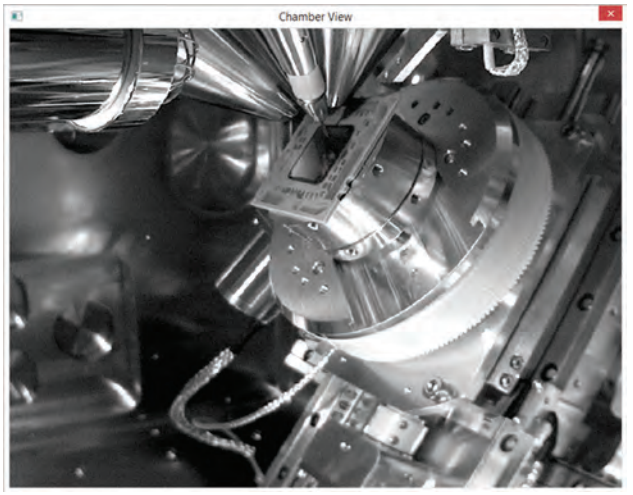
Obvious advantages to the backside thinning approach include the ability to eliminate the depackaging and mechanical planarization of upper layers typically required prior to plasma FIB delayering when approaching from the frontside. An SEM cross section of an Intel Skylake i7 processor (Fig. 4) provides a perspective for discussion. Mechanical planarization is often applied to remove the top four to five layers of the device, consisting of the largest interconnect structures and the thickest interlayer dielectric. Aside from the additional processing step, the quality of the subsequent plasma FIB delayering is dictated by the quality of the initial planarization surface. Automated backside thinning yields a superior starting surface and excellent uniformity at the most critical layers.

Following the automated backside thinning approach, the device is accessed directly at the dense active areas to achieve better uniformity. Note that it is possible to insert the entire die into the FIB-SEM tool for deprocessing without the need to remove the die from the packaging. Importantly, a backside approach also provides the

(continued on page 40)



(a)



(b)

Fig. 3 **(a) 30 kV BSE image immediately following automated backside thinning. The entire 22 × 24 mm die structure is visible in the image, and the residual thickness varies from 1 to 2 µm. The interaction volume yields image information through the residual silicon and into the active silicon. It is apparent that the remaining silicon is thinnest in the lower-right portion of the die. This represents the typical starting condition prior to GAE and delayering with the plasma FIB. (b) Infrared camera image showing the entire die within the package inserted into the plasma FIB-SEM for deprocessing**

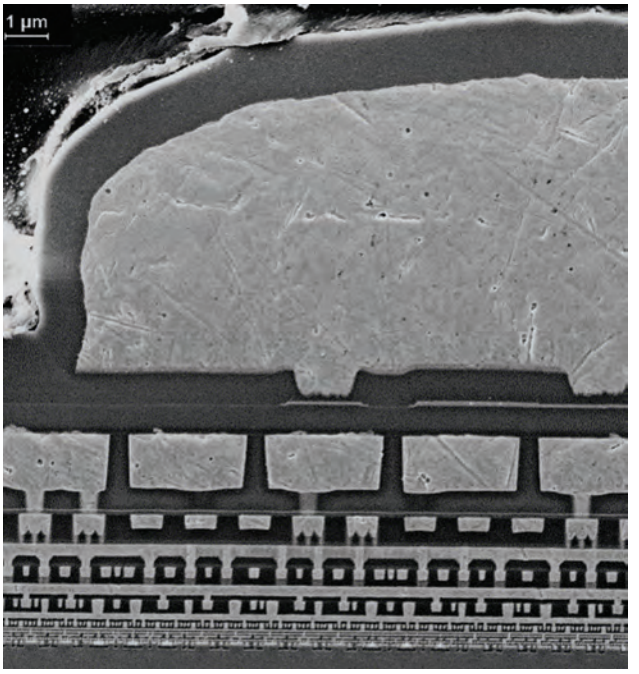


Fig. 4 **SEM cross section of Intel Skylake i7 processor. The frontside of the device is at the top of the image, and the backside is at the bottom of the image, where the density of structures is the highest and the features are of the finest scale. Automated backside processing permits the most direct access to the active areas of the device and yields the highest-quality imaging and uniformity while maintaining maximum device functionality.**

IRLabs

A SUBSIDIARY OF INFRARED LABORATORIES, INC.

ISTFA 2017
Booth
#205

IREM-IV Photon Emission Microscope

NEW FOR 2017

10X Improvement In Signal-To-Noise

Longer LN2 hold time (> 12 hours)

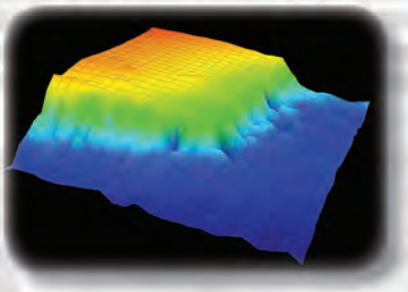
PROVEN!

400 mV Sensitivity on 10 nm Tri-gate/FinFET devices:

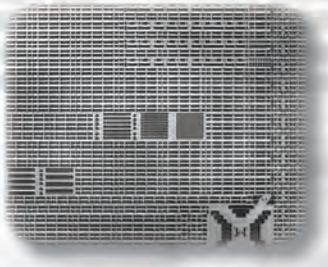
3.3NA SIL on 6-position motorized lens turret
800-2500 nm, 1016 x 1016 px camera
Dual internal cooled filter wheels

Contact IRLabs And Arrange A Demonstration On Your Device Or Wafer!

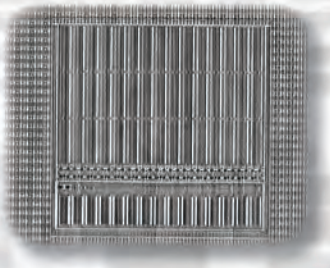
NEW! LASER SURFACE PROBE
Measure device tilt and surface profile



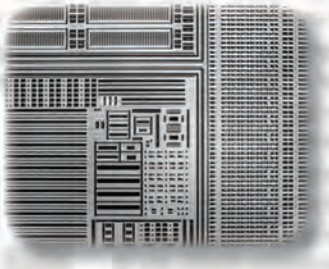
HIGHEST RESOLUTION
Debug 10 nm Process



MOST SENSITIVE
Image 400 mV Emissions



LARGEST FIELD OF VIEW
Custom Optics



1808 East 17th Street • Tucson, AZ 85719-6505 • +1. 520.622.7074
sales@irlabs.com • www.irlabs.com

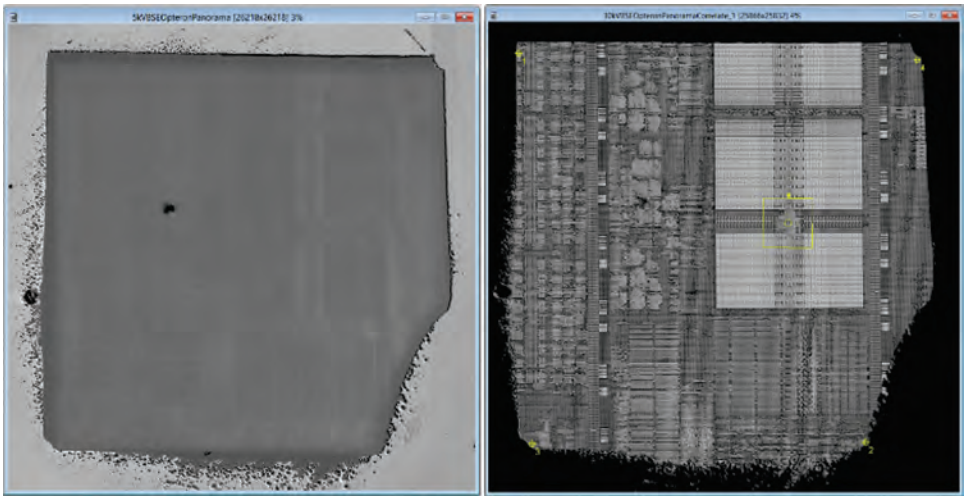
PLASMA FIB DEPROCESSING OF INTEGRATED CIRCUITS FROM THE BACKSIDE *(continued from page 38)*

opportunity to preserve the maximum functionality of the device. By using this approach, it is possible to not only image the device structures but also to interrogate by using a variety of probing techniques for the purpose of fault analysis or reverse engineering. Options include noncontact probing as well as electrical contacts using in situ manipulators and/or powering the device from outside the vacuum chamber.

PLASMA FIB BACKSIDE DELAYERING

Several proprietary gas chemistries are available for plasma FIB-SEM delayering. In general terms, the goal of the gas chemistry, in conjunction with appropriate ion beam energy and current density, is to homogenize the material removal of very heterogeneous structures consisting of a varying density of metal (i.e., copper and tungsten) and interlayer dielectric comprised of a type of porous silicon. To achieve this, the gas chemistry is typically designed to impede the rate of the faster milling components in order to balance the process. The gas chemistry may be modulated depending on the density of metal in the region of interest.

The plasma FIB-SEM delayering process is relatively straightforward, consisting of a repeating sequence of steps that marry chemicophysical delayering with scanning electron imaging. Planar ion milling is performed while simultaneously exposing the region of interest to the delayering chemistry. Following a user-defined period of exposure, the gas-assisted plasma FIB milling is terminated, and the system is prepared for electron imaging in the region of interest, using one or more imaging conditions (i.e., combining both low- and high-voltage imaging montages at each delayering sequence). Imaging conditions include the desired optical parameters, such as accelerating voltage, beam current, field of view, pixel density, and the choice of detectors (secondary electrons, BSEs, etc.). The accelerating voltage governs the interaction volume and hence the depth from which the information is extracted from the volume. Low voltage (i.e., 2 to 5 kV) produces the highest surface sensitivity and provides the best contrast to directly observed *p*- and *n*-doping contrast at the transistor contact level. This information can in turn be used to identify NMOS and PMOS regions during the circuit-extraction process. High accelerating voltage (i.e., 30 kV) yields the greatest depth information and, when combined with BSE detection, allows one to peer one to three layers into the device structure to produce impelling pseudo-3-D perspective. Both types of information content are useful, and the choice of imaging condition(s) is driven by the aims of the analysis. If one is attempting to maintain device functionality, such as in the case of an advanced circuit edit, it is critical to minimize the electron dose to avoid burning up the device. In other situations, the capability to use high voltage and moderate current density allows one to predict the density and location of subsequent layers not visible in low-voltage image data. This information may be useful as part of a multiresolution imaging strategy to optimize the imaging montage schema. The imaging described here employed an automated montage process that is user-defined. The user



(a) (b)

Fig. 5 An image pair showing the initial ~800 × 800 µm area following removal of residual silicon from the backside of an Opteron processor. (a) 5 kV image acquired using an Everhart-Thornley-style secondary electron detector. Doping contrast is visible under these conditions. (b) 30 kV image at the same delayering step acquired with a backscatter detector. Under these imaging conditions, the interaction volume is greater, and the image signal is coming from a greater depth.

defines the overall region of interest for the montage as well as the size of each field of view. The degree of overlap is another variable as well as the dwell time. Altogether, a user has control over the resolution, signal-to-noise, and hence time required for each montage. Optimizing imaging conditions for speed quality and the application of multiresolution imaging strategies is the subject of another paper.[10]

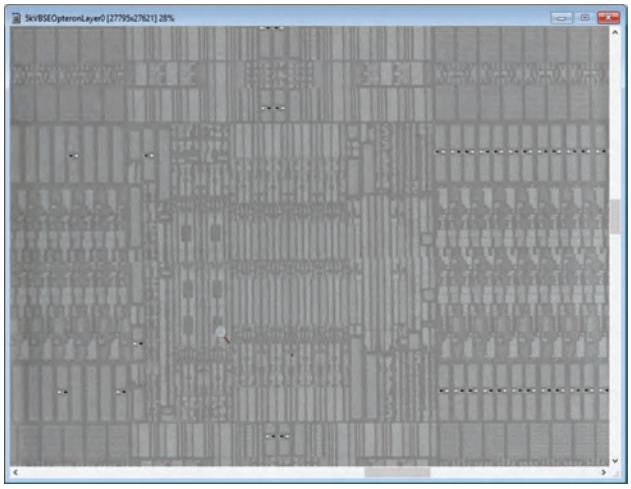
The ion beam conditions may vary between 15 and 30 kV, while the beam current density may range from 0.5 to 2.0 pA/μm^2. At lower ion beam energy, there is a dual benefit. Moderate ion beam energy yields an optimal material-removal rate in conjunction with the gas chemistry. In addition, lower ion beam energy permits a larger field of view and therefore can be applied to yield larger delayering areas. In the case of 15 kV xenon ions, areas as large as 800 μm^2 can be accessed. The distribution of the gas chemistry is also a critical parameter in governing the uniformity that can be achieved over large delayering areas. Multiple gas-injection nozzles and/or gas-concentration schemes may be applied to optimize the gas distribution for the purpose of maximizing large-area delayering uniformity.

The entire process of chemical-assisted ion beam delayering coupled to montage imaging in a plasma FIB-SEM lends itself quite well to integrated automated processing. Aspects of automation, as well as opportunities in computationally guided microscopy in plasma FIB-SEM delayering, is the subject of a related paper.[10]

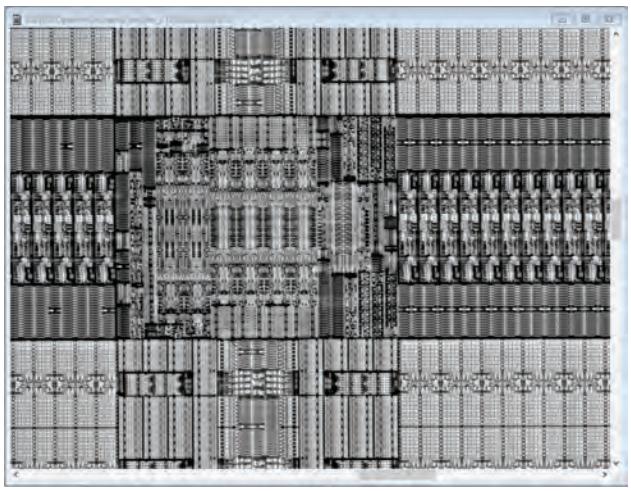
Figure 5 shows a pair of images acquired at two different accelerating voltages to highlight different information. The 5 kV image (Fig. 5a) is a montage of 49 images acquired using a BSE detector, while Fig. 5(b) is a 30 kV BSE image montage. The low-voltage secondary electron image is more surface-sensitive, while the 30 kV image has a larger interaction volume, because the BSE signal emanates from a greater depth in the sample, allowing the structure to be discerned past the metal 1 layer. Each image in the montages contains 4096 × 4096 pixels and required approximately 50 s/image to acquire under the imaging conditions used. The imaging conditions selected in this work do not represent an optimal imaging condition to minimize acquisition time. Optimization of both imaging conditions and strategy, including the application of multiresolution imaging, is the subject of a related paper.[10] Here, the purpose is to validate and demonstrate the overall process and to evaluate a specific delayering gas chemistry applied to this particular device. Delayering exposure times varied between 3 and 7 min/cycle between imaging, depending on the area exposed.

A detailed image pair is shown in Fig. 6, taken from the region highlighted by the yellow box in Fig. 5(b). Metal vias are distinctly bright in the low-kV image (Fig. 6a), while the underlying structure is visible in the 30 kV image (Fig. 6b). Stitching errors in the montage created by the native instrument software are evident. Improving the correlated stitching functions as well as segmentation and feature extraction is the subject of future work.[10]

Figure 7 shows an image pair from a region of interest within the delayering sequence following removal of the contact layer. The gate structures are highlighted at 5 kV, and the underlying M1/M2 structure is observed at 30 kV. The M2 layer is relatively "fuzzy" due to the electron scattering at greater depth. As the lower layers are removed from the backside, the near-surface structures seen at 30 kV become progressively sharper. A final image pair

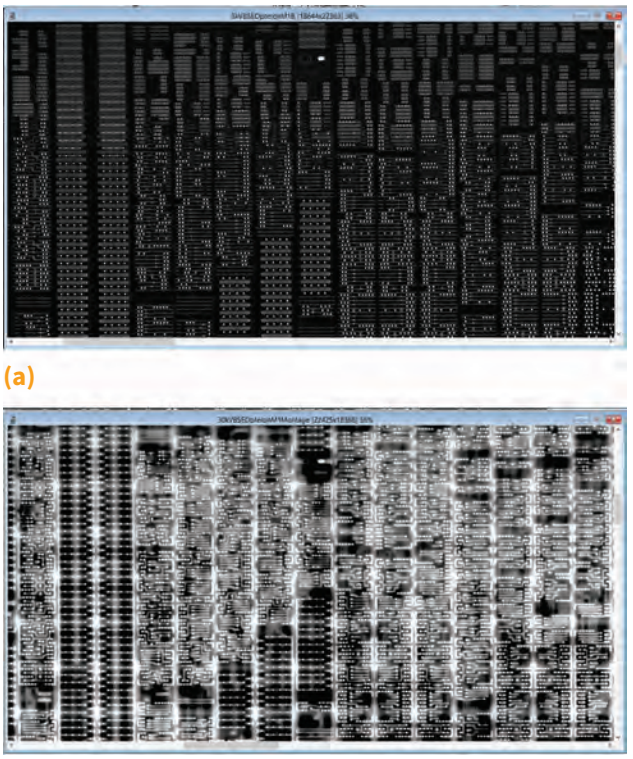


(a)



(b)

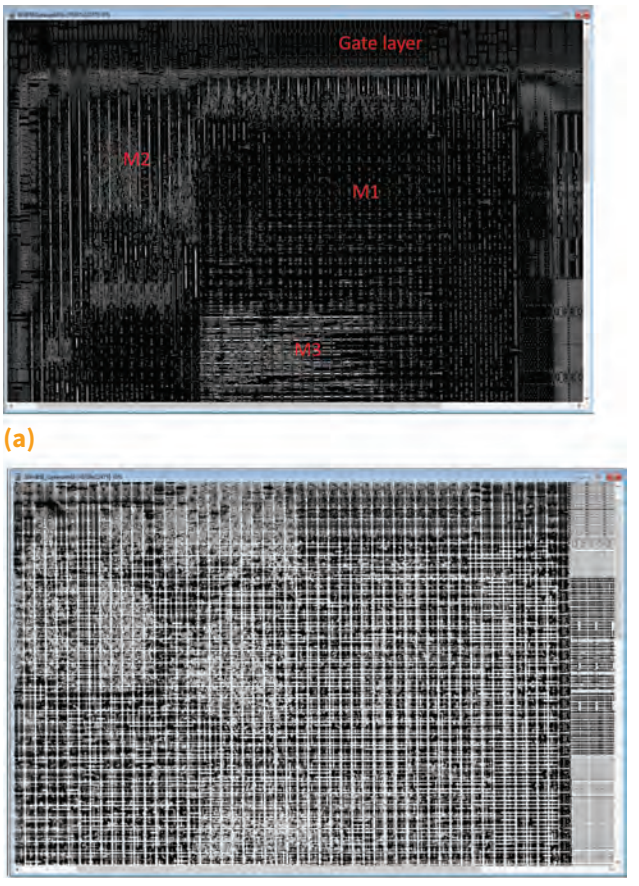
Fig. 6 Image pair taken from the region of interest within Fig. 5(b). Metal vias and doping contrast are emphasized in the 5 kV image (a), while the underlying structure deeper into the device is seen in the 30 kV montage section (b). The field of view is 127 μm in both images.



(a)

(b)

Fig. 7 **(a) Gate structures are highlighted at 5 kV following removal of the contact layer. (b) The 30 kV image from the sequence in the delayering process reveals the M1 and M2 layers. The field of view is 30 µm in both images.**



(a)

(b)

Fig. 8 **(a) 5 kV and (b) 30 kV image pair taken from the same region of interest and at the same cycle in the delayering sequence. The area shown is part of the dose matrix where regions were exposed to different plasma FIB delayering times. The field of view is 107 µm.**

(Fig. 8) depicts the dose matrix in subregions within the 800 µm × 800 µm window. The exposed regions vary from the contact level through to M3.

CONCLUSIONS

This article demonstrated a workflow for deprocessing ICs from the backside using a combination of automated adaptive backside ultrathinning and large-area plasma FIB delayering. Advantages to this approach include a reduction in manual planarization and depackaging. Automated ultrathinning also achieves a higher degree of precision and repeatability. The plasma FIB delayering process following ultrathinning initiates from within 1 to 2 µm of the active device structure, permitting high-quality delayering and imaging over large areas beginning at the highest-density device structures. Using a backside approach, it is also possible to preserve maximum device functionality for probing and powering the device within the plasma FIB-SEM.

Recently the entire process for plasma FIB delayering and SEM imaging has been fully automated via Python scripting. This additional automation permits higher precision in the process and allows unattended operations to perform any desired number of delayering/imaging cycles. The delayering time and imaging parameters may be defined by the user. This automation has been coupled with a commercial computational visualization engine by Object Research Systems. The computation visualization engine is programmatically controlled via Python, and capabilities related to the delayering application include the ability to perform image analysis, stitching, and visualization in a near-real-time environment. Image data may be collected by the computational visualization engine as it becomes available. Instrument control commands can also be fed back into the FIB-SEM during operation, all within the same Python program environment. The x-ray data, thickness data from the ultrathinning process, and delayering image data may be processed and displayed within an integrated volume representing the data cube. Collectively, the interfacing of a programmatic computational visualization engine with an FIB-SEM platform creates a new and significant opportunity for computational guided microscopy and user-defined automation.

The details and future work related to these activities are discussed elsewhere.[10]

REFERENCES

1. N. Asadizanjani et al.: "Non-Destructive PCB Reverse Engineering Using X-Ray Micro Computed Tomography," *Proc. 41st Int. Symp. Test. Fail. Anal. (ISTFA),* 2015.
2. N. Asadizanjani, M. Tehranipoor, and D. Forte: "PCB Reverse Engineering Using Nondestructive X-Ray Tomography and Advanced Image Processing," *IEEE Trans. Compon., Packag., Manuf. Technol.,* 2017, *7*(2), pp. 292-99.
3. S.E. Quadir, J. Chen, D. Forte, N. Asadizanjani, S. Shahbazmohamadi, L. Wang, J. Chandy, and M. Tehranipoor: "A Survey on Chip to System Reverse Engineering," *ACM J. Emerg. Technol. Comput. Syst. (JETC),* 2015.
4. Z. Guo, B. Shakya, H. Shen, S. Bhunia, N. Asadizanjani, M. Tehranipoor, and D. Forte: "A New Methodology to Protect PCBs from Non-Destructive Reverse Engineering," *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2016.
5. M. Alam, H. Shen, N. Asadizanjani, M. Tehranipoor, and D. Forte: "Impact of X-Ray Tomography on the Reliability of Integrated Circuits," *IEEE Trans. Dev. Mater. Reliab.,* 2017, *17*(1), pp. 59-68.
6. M. Holler et al.: "High-Resolution Non-Destructive Three-Dimensional Imaging of Integrated Circuits," *Nature,* March 16, 2017, *543,* pp. 402-06.
7. E.M. Lavely, Y.-S. Lai, K. Gopalakrishnan, and R. Thompson: "3D Element-Specific Bare Die Reconstruction with X-Ray Fluorescence Tomography," Government Microcircuit Applications and Critical Technology Conference (GOMACTech), 2012.
8. "Rapid Analysis of Various Emerging Nanoelectronics (RAVEN)," IARPA, iarpa.gov/index.php/research-programs/raven.
9. M. Rowe: "Fake ICs: Another Weapon in Their Detection," EDN News, May 22, 2017, edn.com/design/test-and-measurement/4458370/Fake-ICs--Another-weapon-in-their-detection.
10. E.L. Principe et al.: "Steps toward Automated Deprocessing of Integrated Circuits," to appear in *Proc. Int. Symp. Test. Fail. Anal. (ISTFA),* 2017.

SELECTED REFERENCES

- M. Bajura, G. Boverman, J. Tan, G. Wagenbreth, C.M. Rogers, M. Feser, J. Rudati, A. Tkachuk, S. Aylward, and P. Reynolds: "Imaging Integrated Circuits with X-Ray Microscopy," Government Microcircuit Applications and Critical Technology Conference (GOMACTech), 2011, pdfs.semanticscholar.org/b19e/ad21a9ff552398378ed847d-17be19348ff61.pdf.
- T.E. Collins III, J.D. Cali, D.A. Chan, D. Dimitrov, S. Turner, E. Lavely, and K. Gopalakrishnan: "Multimodal Imaging Techniques and Strategies for Mixed Signal Integrated Circuits," Government Microcircuit Applications and Critical Technology Conference (GOMACTech), 2014.
- E.M. Lavely, Y.-S. Lai, and K. Gopalakrishnan: "Joint Inversion of Multi-Mode Data for IC Estimation," Government Microcircuit Applications and Critical Technology Conference (GOMACTech), 2013.

ABOUT THE AUTHORS

Edward Principe obtained a Ph.D. in engineering science from The Pennsylvania State University. He has worked for more than 19 years in the area of instrument development for both ultrahigh-vacuum and high-vacuum microscopy and spectroscopy equipment. He is the founder and current President of Synchrotron Research Inc., a designer and manufacturer of imaging near-edge x-ray-absorption fine structure tools. Dr. Principe has written two textbook chapters on the application of FIB-Auger and FIB-based 3-D nanotomographic reconstruction. He holds two patents in FIB-based 3-D reconstruction and has recently focused on the development of computational guided microscopy.

Navid Asadizanjani received a Ph.D. in mechanical engineering from the University of Connecticut in 2014. He is an Assistant Professor with the Electrical and Computer Engineering Department at the University of Florida. His current research interest is on supply chain security and the assurance of everything. This covers a wide range of products, including electronic systems and devices, automotive parts, pharmaceuticals, medical devices, and so on. He is also involved with counterfeit detection and prevention, system- and chip-level reverse engineering, antireverse engineering, and so on.

Domenic Forte received a B.S. degree in electrical engineering from Manhattan College in 2006 and M.S. and Ph.D. degrees in electrical engineering from the University of Maryland in 2010 and 2013, respectively. He is an Assistant Professor with the Electrical and Computer Engineering Department at the University of Florida. Dr. Forte's research covers the entire domain of hardware security, from nanodevices to PCBs, with more than 100 publications. His research has been recognized through Best Paper awards and nominations.

Mark Tehranipoor received a Ph.D. from the University of Texas at Dallas in 2004. He is currently the Intel Charles E. Young Preeminence Endowed Professor in Cybersecurity at the University of Florida. His current research projects include hardware security and trust, supply chain security, VLSI design, test, and reliability. Dr. Tehranipoor has published more than 300 journal articles and refereed conference papers and has given more than 150 invited talks and keynote addresses. He has published six books and eleven book chapters and serves on the program

committee of more than a dozen leading conferences and workshops. He co-founded the IEEE International Symposium on Hardware-Oriented Security and Trust.

Robert Chivas received a Ph.D. in electrical engineering from Boston University in 2007. He is a research scientist at Varioscale, Inc. Since 2012 he has helped pioneer the true five-axis adaptive CNC mill for grinding and polishing ICs. Dr. Chivas also has broad experience in the fields of semiconductor materials, photonics, optics, and fiber optics. He has published more than eleven papers, and his work on synthesizing nanoscale scintillating particles for high-definition radiation sensing was patented in September 2011.

Michael DiBattista is the Vice President of Engineering at Varioscale, Inc. He has worked in the semiconductor industry for 18 years and is currently focused on large-scale deprocessing of semiconductor devices and high-speed imaging. Dr. DiBattista has more than 20 publications in the semiconductor, microscopy, and chemical sensor fields, and he holds 10 issued patents. He received Ph.D., M.S.E., and B.S.E. degrees in chemical engineering from the University of Michigan.

INTERNET RESOURCES FOR ENGINEERING

Rosalinda M. Ring, Qorvo Corp.
Rosalinda.Ring@qorvo.com

BROOKHAVEN NATIONAL LABORATORY

URL: bnl.gov/world

Located on Long Island, New York, Brookhaven National Laboratory is a multipurpose research institution funded primarily by the U.S. Department of Energy's Office of Science. It is a multipurpose lab that serves to build alternative sustainable energy for tomorrow. Almost 3000 scientists, engineers, and support staff are joined each year by more than 4000 visiting researchers from around the world. The lab offers cutting-edge, large-scale facilities for studies in physics, chemistry, biology, medicine, applied science, and a wide range of advanced technologies.

FERMI NATIONAL ACCELERATOR LABORATORY

URL: fnal.gov

Since 1967, Fermilab has been the United States' premier physics laboratory. Located in Batavia, Illinois, Fermilab collaborates with more than 20 countries on physics experiments based in the United States and elsewhere. Online versions of several brochures tell about the laboratory, its work, and its place in the global scientific community.

LAWRENCE BERKELEY NATIONAL LABORATORY

URL: lbl.gov

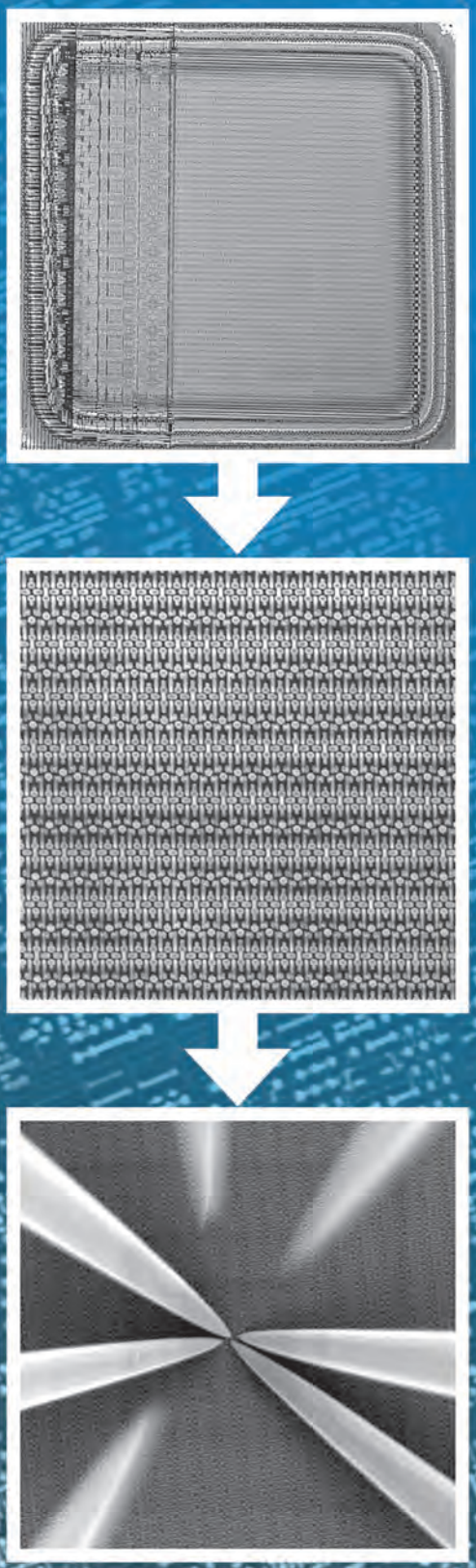
Ernest Orlando Lawrence founded this lab, the oldest of the national laboratories, in 1931. Lawrence invented the cyclotron, which led to a golden age of particle physics and revolutionary discoveries about the nature of the universe. Known as a mecca of particle physics, Berkeley Lab long ago broadened its focus. Today, it is a multiprogram lab where research in advanced materials, life sciences, energy efficiency, detectors, and accelerators serves America's needs in technology and the environment. Berkeley Lab is a member of the national laboratory system supported by the U.S. Department of Energy through its Office of Science. It is managed by the University of California and is charged with conducting unclassified research across a wide range of scientific disciplines.

Gas-assisted IC deprocessing with TESCAN Xe Plasma FIB

TESCAN
PERFORMANCE IN NANOSPACE

HIGHER THROUGHPUT, FASTER TIME-TO-RESULT IN ROOT-CAUSE FAILURE ANALYSIS OF SEMICONDUCTORS

- Damage-free delayering of 14 nm and beyond technology nodes
- Large-area windows > 200 µm × 200 µm at site-specific locations with minimal damage to surroundings
- Proprietary gas chemistry for uniform planarity on physical layers and absence of layer intermixing
- Precise end-point detection
- Probe shuttle for *in-situ* electrical fault isolation (EBIC, EBAC, RCI, current imaging)
- Optional AFM measurement techniques



www.tescan.com

ISTFA/2017

EXHIBITORS

ISTFA 2017 EXHIBITORS as of 9-21-17

BOOTH #	COMPANY
620	Advanced Circuit Engineers
522	Advantest Corporation
507	Allied High Tech Products
110	Anasys Instruments
409	Angstrom Scientific, Inc.
817	Applied Beams
504	Attolight AG
103	Automated Manufacturing, Inc.
206	Balazs Nanoanalysis
402	Bruker
805	BSET EQ
626	Buehler
725	Carl Zeiss Microscopy
806	Checkpoint Technologies
302	Contech Solutions Inc.
822	Control Laser Corp.
209	Digit Concept
816	EAG Laboratories
520	Ebatco
705	EDAX Inc.
406	Ephemeron Labs Inc.
823	FLIR Systems, Inc.
815	Gatan
303	Hamamatsu Corporation
826	HDI Solutions-Hitachi
824	Herzan LLC
207	Hi-Rel Laboratories
415	Hitachi High Technologies
502	ibss Group
622	Imina Technologies SA
205	IR Labs
605	IXRF Systems, Inc.
503	JEOL USA
405	JIACO Instruments
309	Keyence Corporation
407	Kleindiek Nanotechnik
523	Leica Microsystems
603	Mager Scientific, Inc.
414	Materials Analysis Technology
607	Mentor, A Siemens Business
317	MESOSCOPE Technology Co., Ltd.

BOOTH #	COMPANY
506	Micro Support
114	Micromanipulator
420	Microsanj LLC
202	Microtech Laboratories
423	MSSCORPS Co., Ltd.
624	Nanolab Technologies
731	Nanotronics
204	neaspec GmbH
717	Neocera, LLC
203	Nikon Metrology
109	Nippon Scientific Co., Ltd.
702	Nisene Technology Group
115	Nordson DAGE
825	Olympus
521	Oxford Instruments
321	Park Systems Inc.
829	PrimeNano Inc.
112	PVA TePla America, Inc.
814	Quantum Focus Instruments Corp.
721	Quartz Imaging Corp.
730	Raith America, Inc.
304	Raytheon
621	RKD Engineering
819	Robson Technologies, Inc.
315	SAMCO Inc.
706	SELA USA Inc.
221	SEMICAPS
631	SmarAct Inc.
421	Sonoscan
508	SPI Supplies
408	Synopsys
307	TeraView Ltd.
707	TESCAN USA, Inc.
615	Thermo Fisher Scientific (formerly FEI)
723	TMC Ametek
807	Trion Technology
703	ULTRA TEC Mfg., Inc.
306	Varioscale Inc.
715	XEI Scientific, Inc.
403	Yxlon FeinFocus
804	Zurich Instruments AG

ISTFA 2017 EXHIBITORS SHOWCASE

ISTFA/2017

Visit these key exhibitors and more at ISTFA '17 in the Exhibit Hall of the Pasadena Convention Center in Pasadena, Calif.

Exhibition dates and times*
Tuesday, November 7
Show hours: 9 a.m. – 6:30 p.m.
Networking reception: 5 – 6:30 p.m.
Wednesday, November 8
Show hours: 9:30 a.m. – 3:30 p.m.
Dessert reception: 1:30 – 3:30 p.m.
**Times are subject to change*

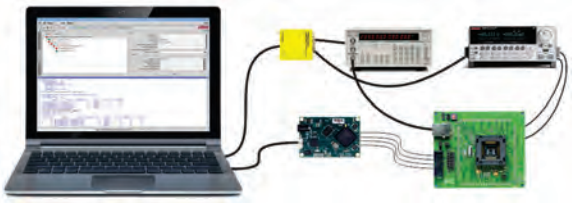
ALLIED HIGH TECH PRODUCTS, INC.

For over 34 years, **Allied High Tech Products** has provided sample preparation products for microscopic evaluation to the microelectronics industry. Allied manufactures state-of-the-art equipment at its California headquarters, and all design, manufacturing, and assembly takes place in-house to ensure the highest-quality equipment is produced. Items on display include Allied's state-of-the-art X-Prep® Precision Polishing/Grinding/Milling Machine, MultiPrep™ Polishing System, TechCut™ Sectioning Saws, and Zeiss microscopes. A range of consumable products will also be shown.

alliedhightech.com

BOOTH 507

MENTOR, A SIEMENS BUSINESS



The Tessent Diagnosis software accelerates defect localization in digital semiconductor devices. With layout-aware and cell-aware technology, interconnect as well as transistor-level defects can be precisely identified based on manufacturing test fail data. Tessent SiliconInsight makes silicon diagnosis even more accessible, enabling bench-top test, characterization, and diagnosis of ATPG-, compression-, and BIST-tested circuits.

mentor.com

BOOTH 607

QUARTZ IMAGING CORPORATION

Software for a FASTER SMARTER Lab!

- **FA-LIMS:** The only laboratory information management system built specifically for failure analysis and materials characterization labs. Configured to match your specific workflow and terminology requirements. Improve lab productivity and efficiency!
- **RE-LIMS:** For reliability and quality assurance labs. Generate qual plans quickly, track all times and results, manage priorities and resources. Interfaces with FA-LIMS.
- **PCI-AM (Automated Measurement of Semiconductor Features) Version 5.0:** This module for Quartz PCI provides automated measurement features for engineers who measure different types of semiconductor device features. Now you can fully characterize a folder of images with a single click!

QUARTZ
FOR A FASTER SMARTER LAB

quartzimaging.com

BOOTH 721

XEI SCIENTIFIC, INC.

XEI Scientific, Inc. is the world leader in remote plasma cleaning of hydrocarbon contamination in vacuum chambers. The Evactron Plasma De-Contaminator uses a unique, energy-efficient RF plasma source to generate oxygen radicals plus UV from nitrogen metastables for dual-action removal of adventitious carbon. Evactron plasma cleaners operate at RP, TMP, and VHV levels for in situ cleaning of EUV and x-ray optics as well as SEM, FIB, and TEM samples. The Evactron De-Contaminator can be installed on most vacuum chambers and electron microscopes. Reach base pressure faster, increase daily throughput, and obtain better analytical data with Evactron plasma cleaning.

Evactron® Plasma Cleaning By XEI Scientific

evactron.com

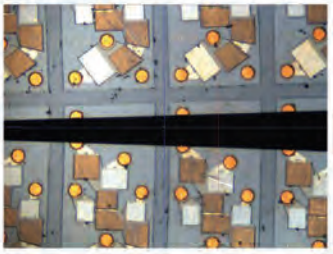
BOOTH 715

FULL RANGE OF CLEAVING SOLUTIONS

For over 25 years SELA has developed and delivered advanced cleaving solutions for failure analysis in the semiconductor industry and analytical purposes in research labs and universities around the world. SELA's patented cleaving technologies address emerging and challenging requirements of the cross-section for a wide variety of structures, materials and substrates.

100% CUSTOMER SATISFACTION
SELA
25 YEARS
1992 - 2017

BY USING SELA TECHNOLOGY YOU ALWAYS ACHIEVE CROSS-SECTION WITH



- HIGH QUALITY
- HIGH ACCURACY
- HIGH THROUGHPUT

PCM

Manual control

Perfect Cleaving Technology
Small size
Ease of use

MC10

Semi-automatic

Precise Cleaving Technology
Accuracy of 2-3um in 1 minute
Tabletop
Smart, simple to use

MC600i

Fully Automatic

Micro-cleaving Technology
Accuracy of 100 nanometers
High success rate cleaving
Ease of use

NO DELAMINATION | NO DEFORMATION | ARTIFACT FREE CROSS-SECTION

SELA USA Inc., 476 Sapena Cr.,Santa Clara, CA 95054
SELA Ltd., 5 Hamada St., Yokneam, Israel 20692

Learn more at
WWW.SELA.COM

Design Flexibility

A Core Component of QFI Microscopes

Integrated Probe Stations 200/300 mm

Portable LabWalker™

ATE-Docking

Application requirements drive configuration decisions.

QuantumScope™ failure analysis microscopes and InfraScope™ temperature measurement microscopes are available in a variety of configurations. Flexibility has always been a core design principle at QFI. We understand the need to consider both current and projected applications when establishing the appropriate capability set for any analytical equipment. QFI systems are generally compatible with field upgrade to address changing requirements. We invite you to discuss your specific analytical needs. Please let us know how we can assist you via the contact information listed below.

QFI Quantum Focus Instruments Corporation

2385 La Mirada Drive • Vista CA 92081
Phone: +1 (760) 599-1122
Fax: +1 (760) 599-1242
e-mail: sales@quantumfocus.com
http://www.quantumfocus.com

INVENTOR'S CORNER

A VERMONT FARMER WALKS INTO A BAR …

Dave Vallett, FASM, PeakSource Analytical
dvallett@peaksourcevt.com

No, seriously! An old Vermont farmer walks into a bar and meets a Texas rancher. They quickly hit it off and eventually get around to discussing their respective agricultural operations. The rancher, being a Texan, proudly boasts that his acreage is so vast that it takes him an entire day to drive its perimeter. The wily Vermonter quips in return, "Yup. I know just what you mean … had a truck like that once myself." The joke—one of my favorites—works because the punch line is so totally unexpected.

Creativity, certainly not unique to Vermonters (notwithstanding Samuel Hopkins of Pittsford, Vt., holder of the first-ever U.S. patent, US X1, in 1790), is also the art of fashioning something unexpected—going in a different direction, twisting things around, or turning them upside down. It's also the essence of a good patent. In this column, after reviewing basic U.S. patent eligibility requirements, we'll focus on the most critical one, novelty (i.e., creativity), and how you can leverage it to become an inventor or improve your future patent ideas.

While an original idea is the foremost prerequisite for a patent, alone it is insufficient to be granted the exclusive right to its use. In fact, the U.S. Patent and Trademark Office has five eligibility requirements: novelty, utility, nonobviousness, suitable subject matter, and no prior public disclosure. The first three are the most significant and are typically stated more succinctly together as "new, useful, and nonobvious." (Apparently the other antonyms for *obvious* are things you wouldn't want your patent known as, like "ambiguous," "obscure," or "unclear" … although if you've ever actually read through an entire patent, you may think those descriptions are perfectly apt.)

Utility or usefulness is the most straightforward of the three. A patent must "provide some identifiable benefit" and be "capable of use." That is to say, it must solve a problem and it must work, or at least theoretically be able to work, in that it follows the laws of physics, mathematics, and so on. Therefore, your idea needs to provide value to some industry or endeavor, and while you don't have to have already built it or demonstrated its function, it must at least be operable. After all, if it won't work, it's not very useful.

> "A PATENT MUST 'PROVIDE SOME IDENTIFIABLE BENEFIT' AND BE 'CAPABLE OF USE.'"

As it turns out, the "nonobvious" requirement is actually far from obvious. A patent application must show that the idea would not be obvious to "one having ordinary skill in the art." This concept is actually best understood in the words of Thomas Jefferson from an 1813 letter to Isaac McPherson on the nature of ideas: "… a machine of which we were possessed, might be applied by every man to any use of which it is susceptible, and that this right ought not to be taken from him and given to a monopolist." In other words, let's say our Vermont farmer puts a longer handle on a hammer and uses it to persuade his dodgy truck's starter solenoid to engage (not that I have ever done this …). Jefferson would assert that the hammer's inventor (the monopolist) shouldn't be legally able to stop him. He went on to explain that a change in purpose, material, or form does not entitle a prospective patentee to claim the exclusive right to a different application of a known invention, altering it slightly, making only changes that would be *obvious* to anyone familiar with such articles. In modern practice, however, legal determinations can be quite subjective and receive much debate in patent law. What constitutes "ordinary skill"? Who possesses such skill? What is the scope of that art? Other than following the above general guidelines, and making sure your patent idea passes the "duh" test among your colleagues, obviousness is best left to patent examiners and attorneys. So, we return to novelty, the creative nugget of every successful patent. How can the failure analyst, researcher, or instrument developer find innovation and "advance the state of his or her art"?

We can categorize two general sources of ideas that might lead to patents: problems in search of a solution, and solutions in search of a problem. The former is of course more common. Engineers, technicians, and scientists encounter problems and find solutions every day. But not every new way of doing something is patentable. More often we merely apply "good engineering," for example, automating a test program, altering an illumination path for higher quantum efficiency, or making a chemical waste system more efficient. New? Yes, but maybe only to you or your lab. Useful? To your work, certainly. But would most other labs benefit from it? And finally, is it nonobvious? Re-read Jefferson's words and think about how much you've changed the original approach. All of this is not to say that problem solutions are never patentable—quite the contrary—but it's usually a matter of the size of the problem and the breadth of the solution.

Another pitfall is assuming your potentially patentable idea must be cost-effective and timely. In our work we naturally look for the least-expensive approach that we can implement as soon as possible. But neither condition is among the U.S. patent prerequisites. Our normal tendencies toward problem solving can really limit creative thinking. So, for patent purposes, it's best to consider broader solutions to a problem apart from the one you actually need now and within budget. If it's a serious enough issue that would generally affect others in the industry, fix your lab's problem first. Then, with cost as no object and no time pressure, focus on more creative approaches. As Faber College's Dean Wormer might have said to hapless Delta pledge Kent Dorfman if the 1978 classic film "Animal House" had taken place in a laboratory: "Fast, cheap, and obvious is no way to get through the patent process, son."

So, how do we effect more innovative solutions and patentable ideas? Creativity is in large part a personality trait, but there are techniques we use to prime ourselves to think more openly and unlock our imaginative tendencies. One method is to apply knowledge from a hobby or another field. Curiosity drives many failure analysis people, and they tend to be tinkerers with skills and interests in a variety of fields. Trying to find a better way to mill a chip or package? Think about how router bits work on wood. Looking for a new way to sense acoustic signals in packages or printed circuit boards? Maybe guitar pickups have an answer. Want to improve the way a probe embeds into a metal pad? How does the shape and motion of a moldboard plow blade enable it to efficiently dig into soil? While a patentable idea cannot be obvious to anyone "skilled in *the* art," the requirement says nothing about using skills from *another* art to solve problems. Another path is to consider the exact opposite of what you're hoping to accomplish with your solution. Thinking about how things break forces us to think more broadly about how to keep them from breaking.

The second and arguably more original category of generating patentable ideas is using solutions in search of problems. In failure analysis we see many different types of defects: unique processing anomalies, design errors, mask problems, reliability failure mechanisms, and so on. They can be an especially rich source of distinctive structures or processes that might be used to make something useful and *solve* a problem instead of creating one. What made your device fail might indeed be the seed of an entirely new structure. For example, the seminal idea of a MOSFET sidewall spacer (U.S. patent 4,256,514 A) to enable a lightly doped drain came from a manufacturing defect created by the accidental patterning of a narrow stud or mandrel. Referenced by almost 160 subsequent patents, it's a wonderful example of a solution in search of a problem. And when it comes to using defects and failures as patent ideas, remember that you only need to show that it's "operable," or *able* to be made, not that it can be made inexpensively, quickly, repeatedly, or reliably. What better proof than the image from your failure analysis report!

Finally, a quick word of advice about creativity and thinking broadly. Everyone has "good ideas." While many seem creative and unique to their work group, most are not actually patentable. A simple online search usually shows someone else got there first or solved the problem another way. Deeper digging in a patent database can frequently turn up the same or similar idea as well. Evidence of prior publication or use is frustrating and disappointing, but it's better to find out early in the game. Do your homework. It's easy and it will make you a better inventor. You'll learn not only what HAS been patented in your area of expertise, but more importantly, what HASN'T, resulting in more robust ideas.

We've reviewed the three most important U.S. patent requirements: novelty, utility, and nonobviousness. We then focused on a few ways to bring patent-worthy novelty and creativity to your everyday work (and did it without once referring to "thinking outside the six-sided cubical subpolyhedron"). Good luck and happy patenting. It can be a fun and challenging complement to your "day job" and rewarding to both you and your employer. And if you ever make it up to northern Vermont, I have a truck you might be interested in. But you'll need your own long-handled hammer … I grant myself the exclusive right to keep using mine.

PRODUCT NEWS

PRESS RELEASE SUBMISSIONS:
MAGAZINES@ASMINTERNATIONAL.ORG

Larry Wagner, LWSN Consulting Inc.
lwagner10@verizon.net

THERMO FISHER SCIENTIFIC ADDS NEW FA PRODUCTS

For semiconductor manufacturers seeking fast, high-quality electrical and physical failure analysis, Thermo Fisher Scientific (Hillsboro, OR) announced three new additions to its broad portfolio of semiconductor failure analysis workflows. The company demonstrated these products and its other market-leading technologies during the 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2017) in Chengdu, China.

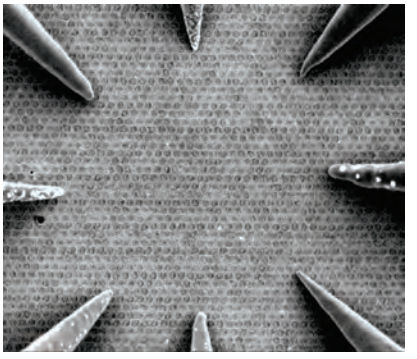
The new Helios G4 plasma focused ion beam (FIB) system is designed to deprocess and provide ultra-high-resolution scanning electron microscopy (SEM) analysis on a wide variety of semiconductor devices. The new flexProber system is used for fast electrical fault isolation to identify and locate faults at both interconnect and transistor levels of the semiconductor wafer. The new Themis S transmission electron microscope (TEM) is designed to provide atomic-level resolution imaging and high-throughput chemical analysis on the most challenging semiconductor devices.

"The semiconductor market continues to evolve at a fast pace, with strong growth in the memory, foundry, Internet of Things (IoT), advanced packaging, and display markets," said Rob Krueger, Vice President and General Manager of Semiconductors at Thermo Fisher. "This growth has increased the need for fast, high-quality electrical and physical failure analysis. These products add new capabilities and increased flexibility to our existing portfolio of failure analysis solutions."

The Helios G4 plasma FIB system

The Helios G4 plasma FIB system is Thermo Fisher's latest-generation DualBeam microscope. It can perform a wide variety of failure analysis applications, from high-speed delayering to SEM cross-sectional imaging of devices and TEM sample preparation. Semiconductor delayering is an increasingly important application in fault localization at sub-14 nm technology nodes. The plasma FIB and proprietary Dx chemistry is used to expose metallization layers, allowing electrical fault isolation and analysis to be performed with Thermo Fisher nanoprobing tools.

The Helios G4 plasma FIB system can support deprocessing down to the 7 nm node and offers automated end pointing that stops milling automatically when the metal or via layer of interest is exposed. It provides up to 10 to 20 times faster milling rates than conventional (Ga^+) FIB solutions, allowing engineers to create larger samples for nanoprobing and TEM imaging, as well as large-area SEM cross sections, on a broad range of advanced (2.5-D) packaging, light-emitting diodes, display, and microelectromechanical systems.



The flexProber includes eight probe positioners and a high-resolution sample stage.

The new flexProber system is designed to help engineers quickly locate and identify electrical faults, using an SEM to position fine mechanical probes on exposed circuit elements. Accurately locating the fault can improve productivity and cost-effectiveness in subsequent analysis by ensuring that the fault is included when a thin section is extracted for high-resolution imaging in a TEM. The flexProber system includes a new SEM column specifically designed for probing applications, with a 2× improvement in resolution compared to its predecessor, the nProber II. It incorporates many of the capabilities of Thermo Fisher's high-end Nanoprober product line and is designed to address a broad range of semiconductor device types and process technologies. It provides an ideal pathway into electrical probing, offering an

entry-level configuration while preserving the option to upgrade to full Nanoprober system capability in the future.

The Themis S system

The Themis S system is Thermo Fisher's latest addition to the industry-standard Themis TEM platform. Targeted to the needs of semiconductor failure analysis labs working at the sub-20 nm technology node, the Themis S system is designed for high-volume semiconductor imaging and analysis and includes an integrated vibration-isolation enclosure and full remote-operation capability. The probe-corrected 80 to 200 kV column, automated alignments, XFEG source, and DualX x-ray spectrometer provide robust, sub-Ångström imaging and fast, accurate elemental and strain analysis.

"We have customers working on a wide variety of devices, from the most advanced memory and logic at the sub-20 and even 7 nm nodes, to more mature device technology that is still critically important and used in many state-of-the-art applications, like smart phones and IoT products," said Krueger. "Our suite of failure analysis tools covers a diverse set of semiconductor customers with a wide array of requirements."

For more information: web: thermofisher.com.

BRUKER INTRODUCES TRIBOLAB SYSTEM

Bruker's Nano Surfaces Division announced the introduction of the TriboLab CMP Process and Materials Characterization System, which provides a unique characterization capability for the development of chemical mechanical polishing (CMP) processes on the proven robust Universal Mechanical Tester TriboLab platform. The new TriboLab CMP system is the only tool on the market that can provide a broad range of polishing pressure (0.05 to 50 psi), speeds (1 to 500 rpm), friction, acoustic emissions, and surface temperature measurements for the accurate and complete characterization of CMP processes and consumables.

"CMP is more critical than ever for advanced semiconductor device fabrication. The industry has been calling for a means to effectively characterize the detailed process and consumables interactions that take place while polishing a wide range of materials," said Dr. Robert Rhoades, Chief Technology Officer of Entrepix, a leading provider of equipment and wafer-processing services to the CMP industry. "We are pleased to partner with Bruker and assist in the launch of the TriboLab CMP platform. With the addition of this new system to our capabilities, we are poised to provide a reliable R&D solution for testing and characterization of complex interactions among pads, slurries, conditioning, and process parameters, with unmatched repeatability and detail."

For more information: web: bruker.com.

DIRECTORY OF INDEPENDENT FA PROVIDERS

Rosalinda M. Ring, Qorvo Corp.
Rosalinda.Ring@qorvo.com

Electronic companies of all types and sizes require failure analysis (FA) services. Our goal is to supply a resource of FA service providers for your reference files. The directory lists independent providers and their contact information, expertise, and types of technical services offered.

ANALYTICAL SOLUTIONS—ALBUQUERQUE

DPA & FA Services
10401 Research Rd. SE
Albuquerque, NM 87123
Tel: 800.622.2382/505.299.1967
Web: integra-tech.com/analytical-solutions
Services: Destructive physical, failure, and construction analyses; counterfeit IC detection; etc.
Tools/Techniques: External/internal visual inspection; x-radiography inspection; PIND; seal fine and gross leak testing; dye penetrant testing; XRF; bond pull and die shear; ball shear; copper wire evaluations; FIB editing; physical dimension; marking permanency; AC, DC, and full functional electrical test; 150 to 200 °C temperature test; OEM date code verification; blacktop test; burn-in/qualification; solderability testing; etc.

FAST ANALYSIS LABORATORIES, INC.

1135 E. Arques Ave.
Sunnyvale, CA 94085
Tel: 408.868.2948
e-mail: service@fa-labs.com
Web: fa-labs.com
Services: Electrical and physical failure analyses, nondestructive analysis, package analysis, sample preparation, reverse engineering, consulting, etc.
Tools/Techniques: Advanced laser decapsulation of copper wire, chemical delidding, backside bulk silicon sample preparation, bulk laser marking and cutting, dye and pry, electrical analysis and curve tracing, fault isolation (front and backside) with OBIRCH, FIB circuit edit and cross sectioning, high-resolution digital optical microscopy, IR inspection, SEM/EDS, real-time x-ray inspection, wet and parallel lap deprocessing, etc.

IEC ELECTRONICS

105 Norton St.
Newark, NY 14513
Tel: 315.331.7742/888.688.3570
e-mail: info@iec-electronics.com
Web: iec-electronics.com
Services: Material analysis testing, detection and avoidance of counterfeit components
Tools/Techniques: Destructive physical analysis, failure analysis, decapsulation, SEM, cross-sectional analysis, 3-D x-ray inspection, XRF, optical microscope, dye and pry, microhardness testing, strain gage testing, compression and tensile testing, FTIR/TGA, SEM/EDX (elemental mapping), bond/die shear, wire pull, delidding and decapsulation, etc.

ITRI INNOVATION

Unit 3, Curo Park
Frogmore, St. Albans
Hertfordshire, AL2 2DD, U.K.
Tel: +44 (0) 1727 875 544
e-mail: wayne.lam@itri.co.uk
Web: itri.co.uk
Services: PCB quality control, reliability testing, failure analysis, counterfeit components testing, consulting, etc.
Tools/Techniques: Dye and pry analysis, microsectioning, optical microscopy inspection, SEM/EDX analysis, solderability testing, thermal cycling testing, x-ray inspection, etc.

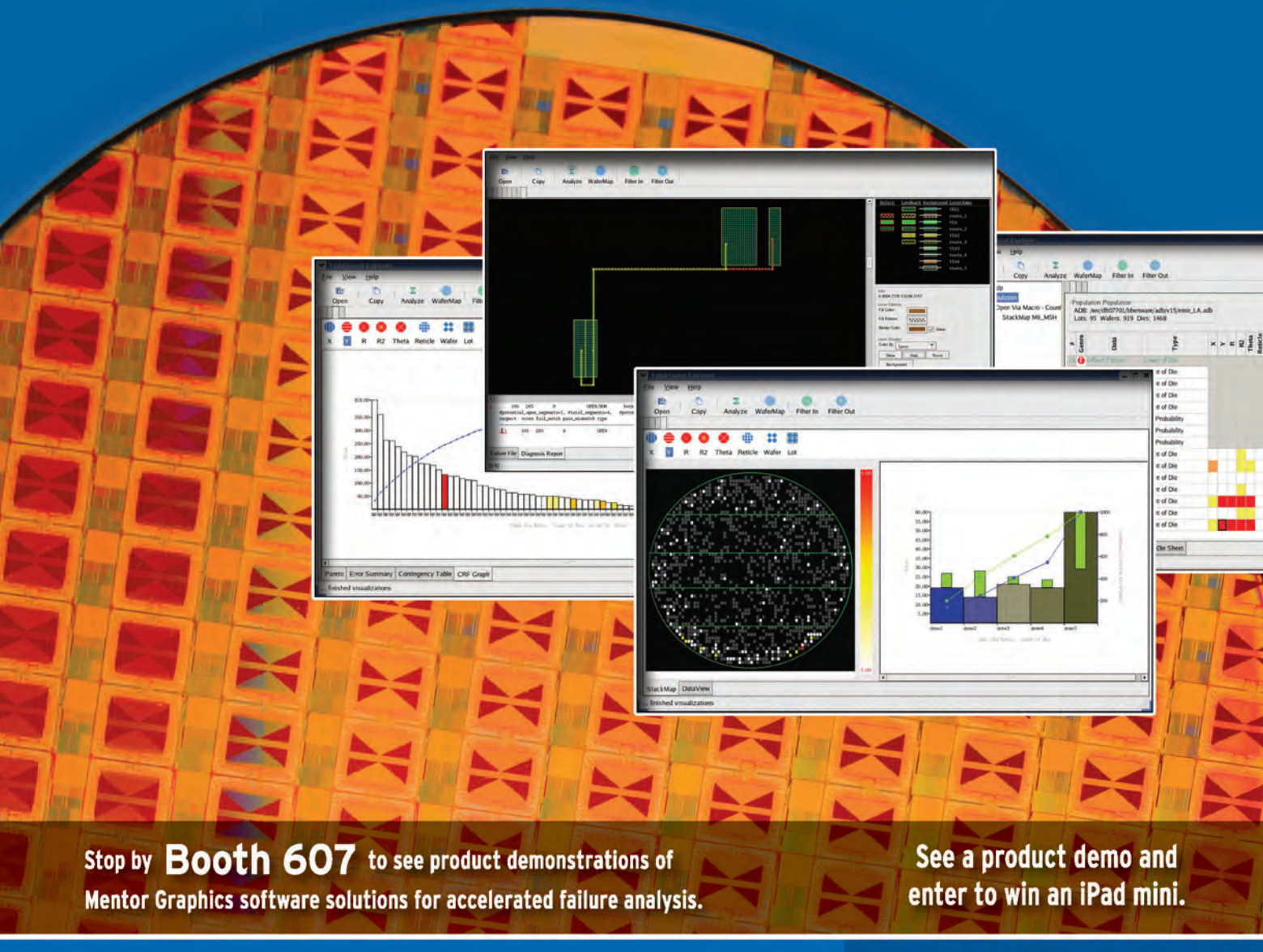
MICROLABS SCIENTIFIC, LLC

100 Burtt Rd., Suite 125
Andover, MA 01810
Tel: 978.409.2812
e-mail: contact@microlabsscientific.com
Web: microlabsscientific.com
Services: Analytical, consulting, and failure analysis services
Tools/Techniques: SEM, EDS, FIB milling, optical profilometry, thermal imaging, film-thickness measurement, optical microscopy, vibration measurements, etc.

MICROTECH LABORATORIES, LLC

538 Haggard St., Suite 402
Plano, TX 75074
Tel: 972.633.0007
e-mail: contact@micro-labs.com
Web: microtechlaboratories.com
Services: Turn-key failure analysis, component analysis, PCB analysis, reverse engineering, construction analysis, sample preparation, consulting and training, etc.
Tools/Techniques: Real-time x-ray, scanning acoustic microscopy, SEM/EDX (elemental mapping), backscattered or secondary electron imaging, backside sample preparation, decapsulation (die exposure), die deprocessing, emission microscopy, liquid crystal, FIB, cross section, mechanical probing, etc.

TIME TO ROOT CAUSE GETTING OUT OF CONTROL?



Stop by Booth 607 to see product demonstrations of Mentor Graphics software solutions for accelerated failure analysis.

See a product demo and enter to win an iPad mini.

The Tessent® silicon learning software products are specialized for understanding and identifying yield loss from test data, maximizing failure analysis success rate, and accelerating test bring-up of digital semiconductor devices. Get more information at mentor.com/silicon-yield

Mentor®
A Siemens Business

TRAINING CALENDAR

Rose M. Ring, Qorvo, Inc.
rosalinda.ring@qorvo.com

SEMICONDUCTOR ONLINE TRAINING

EDFAS offers online training specialized for semiconductor, microsystems, and nanotechnology suppliers and users. These online training courses are designed to help engineers, technicians, scientists, and managers understand each of these dynamic fields. This one-year subscription provides access to several courses covering semiconductor failure analysis, design, packaging, processing, technology, and testing. Find out more by visiting edfas.org and clicking on Education.

November 2017

EVENT	DATE	LOCATION
Los Angeles/Orange County SMT Expo & Tech Forum	11/2	Long Beach, CA
Rocky Mountain-PCBA Electrical Test Demo & Tour at Acroname	11/14	Boulder, CO
SMT Processes Certification	11/14-16	Dallas, TX
New England SMT Expo & Tech Forum	11/16	Worcester, MA
LED Assembly, Reliability & Testing Exhibition/Symposium	11/28-30	Research Triangle Park, NC
Silicon Valley SMT Expo & Tech Forum	11/29	San Jose, CA
Contact: SMTA		
ISTFA 2017	11/5-9	Pasadena, CA
Corrosion	11/6-9	Novelty, OH
Advanced Metallographic Techniques	11/6-9	Novelty, OH
Practical Fracture Mechanics	11/13-14	Novelty, OH
Metallography for Failure Analysis	11/13-16	Novelty, OH
Elements of Metallurgy	11/13-16	Novelty, OH
Practical Fractography	11/15-16	Novelty, OH
Contact: ASM International		
ESD Basics for the Program Manager	11/8	Jiangsu, China
How To's of In-Plant ESD Auditing and Evaluation Measurements	11/9	Jiangsu, China
Essentials for ESD Programs Factory: Technologies, Controls, Procedures	11/10	Jiangsu, China
Contact: EOS/ESD		

November 2017 (cont'd)

EVENT	DATE	LOCATION
ESD Control Workstations: Set-up, Practical Considerations & Measurements	11/14	Ho Chi Minh City, Vietnam
How To's of In-Plant ESD Auditing and Evaluation Measurements	11/15	Ho Chi Minh City, Vietnam
Hands-on ESD Measurements & Instruments—Uses and Pitfalls	11/16	Ho Chi Minh City, Vietnam
Ultra-Sensitive (Class 0) Devices: ESD Controls and Auditing Measurements	11/16	Ho Chi Minh City, Vietnam
Contact: EOS/ESD		

December 2017

EVENT	DATE	LOCATION
IEEE International Electron Devices Meeting	12/2-6	San Francisco, CA
Contact: IEDM 2017		
ESD Training for Internal Auditors and Supplier Quality	12/4	Rome, NY
Costly Controversial ESD Myths	12/5	Rome, NY
Perfect ESD Storm	12/5	Rome, NY
Contact: EOS/ESD		
Metallurgy for the Non-Metallurgist	12/4-7	Novelty, OH
Introduction to Metallurgical Lab Practices	12/11-13	Novelty, OH
Contact: ASM International		
19th Electronics Packaging Technology Conference	12/6-9	Singapore, Singapore
Contact: EPTC 2017		
29th International Conference on Microelectronics	12/10-13	Beirut, Lebanon
Contact: ICM 2017		

January 2018

EVENT	DATE	LOCATION
Consumer Electronic Symposium	1/9-12	Las Vegas, NV
Contact: CES 2018		
Conference on Electronic and Advanced Materials	1/17-19	Orlando, FL
Contact: EAM 2018		

January 2018 (cont'd)

EVENT	DATE	LOCATION
Space Coast SMTA Expo & Tech Forum	1/18	Melbourne, FL
Rocky Mountain SMTA Expo & Tech Forum	1/25	Denver, CO
Contact: SMTA		
IS&T International Symposium on Electronic Imaging	1/28-2/1	Burlingame, CA
Contact: EI 2018		

Contact Information

ASM International
Tel: 800.336.5152, ext. 0
e-mail: MemberServiceCenter@asminternational.org
Web: asminternational.org

CES 2018
Tel: U.S.: 866.233.7968; Outside U.S.: 703.907.7605
e-mail: U.S.: CESreg@CTA.tech;
Outside U.S.: internationalreg@CTA.tech
Web: ces.tech

EAM 2018
Tel: 866.721.3322 or 240.646.7054
e-mail: customerservice@ceramics.org
Web: ceramics.org/eam2018

EI 2018
Tel: 703.642.9090
e-mail: info@imaging.org
Web: imaging.org/site/IST/IST/Conferences/EI/Symposium_Overview.aspx

EOS/ESD
Tel: 315.339.6937
e-mail: info@esda.org
Web: esda.org

EPTC 2017
e-mail: secretariat@eptc-ieee.net
Web: eptc-ieee.net

ICM 2017
e-mail: ali.hamie@aul.edu.lb or mohamad.sawan@polymtl.ca
Web: aul.edu.lb/ICM2017

IEDM
Tel: 301.527.0900, ext. 2
e-mail: info@ieee-iedm.org
Web: ieee-iedm.org

SMTA
Tel: 952.920.7682
e-mail: smta@smta.org
Web: smta.org

InfraScan SWP™

Shortwave Probing System

High Resolution Optical Probing to 5nm

- 532nm, 577nm, 785nm laser wavelengths
- 2.4 to 3.3NA SIL
- Easy-to-use software interface
- Retrofits with all Checkpoint FA tools
- Dual SIL
- Emission, MCT or InGaAs

Available In Top-Down and Inverted Systems

CHECKPOINT TECHNOLOGIES, LLC

CHECKPOINTTECHNOLOGIES.COM • 408.321.9780

ISTFA 2017
Booth #806

Helping integrated circuit manufacturers produce more reliable, faster and better functioning electronic devices.

LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Beam-Based Analysis Techniques

Michael R. Bruce, Consultant
mike.bruce@earthlink.net

The current column covers peer-reviewed articles published since 2015 on beam-based analysis techniques; this includes atomic, electron, neutron, ion, and x-ray beam technologies. These technologies typically offer the highest resolution, sometimes down to the atomic level; in addition, focused ion beams (FIBs) are fundamental to inspecting and modifying electronic circuits. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

- D. Basta, M. Endrizzi, F.A. Vittoria, et al.: **"Compact and Cost Effective Lab-Based Edge-Illumination X-Ray Phase Contrast Imaging with a Structured Focal Spot,"** *Appl. Phys. Lett.,* 2016, *108*, p. 224102.
- L. Bischoff, P. Mazarov, L. Bruchhaus, et al.: **"Liquid Metal Alloy Ion Sources—An Alternative for Focused Ion Beam Technology,"** *Appl. Phys. Rev.,* 2016, *3*, p. 021101.
- A. Denisyuk, T. Hrnčíř, J.V. Oboňa, et al.: **"Mitigating Curtaining Artifacts during Ga FIB TEM Lamella Preparation of a 14 nm FinFET Device,"** *Microsc. Microanal.,* 2017, *23*, p. 484.
- P.C. Diemoz, C.K. Hagen, M. Endrizzi, et al.: **"Single-Shot X-Ray Phase-Contrast Computed Tomography with Nonmicrofocal Laboratory Sources,"** *Phys. Rev. Appl.,* 2017, *7*, p. 044029; see also K. Wright: **"Focus: 3D Images 10 Times Faster,"** *Physics,* 2017, *10*, p. 48.
- Y. Dreznera, Y. Greenzweig, S. Tan, et al.: **"High Resolution TEM Analysis of Focused Ion Beam [FIB] Amorphized Regions in Single Crystal Silicon—A Complementary Materials Analysis of the Teardrop Method,"** *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron: Mater., Process., Meas., Phenom.,* 2017, *35*, p. 011801.
- R. Estivill, M. Juhel, G. Servanton, et al.: **"Boron Atomic-Scale Mapping in Advanced Microelectronics by Atom Probe Tomography [APT],"** *Appl. Phys. Lett.,* 2017, *110*, p. 252105.
- M. Garbrecht, B. Saha, J.L. Schroeder, et al.: **"Dislocation-Pipe Diffusion in [Hafnium] Nitride Superlattices Observed in Direct Atomic Resolution [Using TEM],"** *Sci. Rep.,* 2017, *7*, p. 46092; see also *Microscopy and Microanalysis* Editorial **"STEM Captures Elusive Atomic Motion,"** microscopy-analysis.com/editorials/editorial-listings/stem-captures-elusive-atomic-motion, May 22, 2017.
- L.A. Gomes Perini, P. Bleuet, J. Filevich, et al.: **"Developments on a SEM-Based X-Ray Tomography System: Stabilization Scheme and Performance Evaluation,"** *Rev. Sci. Instrum.,* 2017, *88*, p. 063706.
- H. Han, A. Beyer, J. Belz, et al.: **"Quantitative Atomic Resolution at Interfaces: Subtraction of the Background in STEM Images with the Example of (Ga,In) P/GaAs Structures,"** *J. Appl. Phys.,* 2017, *121*, p. 025301.
- P.M. Haney, H.P. Yoon, B. Gaury, et al.: **"Depletion Region Surface Effects [Induced by FIB] in Electron Beam Induced Current [EBIC] Measurements,"** *J. Appl. Phys.,* 2016, *120*, p. 095702.
- M. Holler, M. Guizar-Sicairos, E.H.R. Tsai, et al.: **"High-Resolution Non-Destructive Three-Dimensional [X-Ray] Imaging of Integrated Circuits,"** *Nature,* 2017, *543*, p. 402; see also P. Piwnicki: **"3-D X-Ray Imaging Makes the Finest Details of a Computer Chip Visible,"** phys.org/news/2017-03-d-x-ray-imaging-finest-chip.html, March 16, 2017.
- J. Huang, M. Loeffler, U. Muehle, et al.: **"A Study of Gallium FIB Induced Silicon Amorphization Using TEM, APT and BCA Simulation,"** *Microsc. Microanal.,* 2015, *21*, p. 1839.

- R. Ishikawa, S.J. Pennycook, A.R. Lupini, et al.: **"Single Atom Visibility in STEM Optical Depth Sectioning,"** *Appl. Phys. Lett.,* 2016, *109*, p. 163102.
- C.S. Kaira, C.R. Mayer, V. De Andrade, et al.: **"Nanoscale Three-Dimensional Microstructural Characterization of an Sn-Rich Solder Alloy Using High-Resolution Transmission X-Ray Microscopy (TXM),"** *Microsc. Microanal.,* 2016, *22*, p. 808.
- T.F. Kelly: **"Atomic-Scale Analytical Tomography,"** *Microsc. Microanal.,* 2017, *23*, p. 34.
- M.A. Khan, S.P. Ringer, and R. Zheng: **"Atom Probe Tomography [APT] on Semiconductor Devices [Review],"** *Adv. Mater. Interfaces,* 2016, *3*, p. 1500713.
- J. Kujala, J. Slotte, F. Tuomisto, et al.: **"Si Nanocrystals and Nanocrystal Interfaces Studied by Positron Annihilation,"** *J. Appl. Phys.,* 2016, *120*, p. 145302.
- P. Lu, R. Yuan, and J.M. Zuo: **"Fast Atomic-Scale Elemental Mapping of Crystalline Materials by STEM Energy-Dispersive X-Ray Spectroscopy Achieved with Thin Specimens,"** *Microsc. Microanal.,* 2017, *23*, p. 145.
- S. Matsuyama, S. Yasuda, J. Yamada, et al.: **"50-nm-Resolution Full-Field X-Ray Microscope without Chromatic Aberration Using Total-Reflection Imaging Mirrors,"** *Sci. Rep.,* 2017, *7*, p. 46358.
- S. Morishita, M. Mukai, K. Suenaga, et al.: **"Atomic Resolution Imaging at an Ultralow Accelerating Voltage by a Monochromatic Transmission Electron Microscope [TEM],"** *Phys. Rev. Lett.,* 2016, *117*, p. 153004.
- K. Mukherjee, B.A. Wacaser, S.W. Bedell, et al.: **"Rapid Imaging of Misfit Dislocations in SiGe/Si in Cross-Section and through Oxide Layers [Plan-View] Using Electron Channeling Contrast [Imaging (ECCI) in an SEM],"** *Appl. Phys. Lett.,* 2017, *110*, p. 232101.
- M. Nord, P.E. Vullum, I. MacLaren, et al.: **"Atomap: A New Software Tool for the Automated Analysis of Atomic Resolution Images Using Two-Dimensional Gaussian Fitting,"** *Adv. Struct. Chem. Imag.,* 2017, *3*, p. 9.
- M. Picher, S. Mazzucco, S. Blankenship, et al.: **"Vibrational [Raman] and Optical Spectroscopies Integrated with Environmental Transmission Electron Microscopy [TEM],"** *Ultramicroscopy,* 2015, *150*, p. 10.

SPEEDING UP FAILURE ANALYSIS USING FAB AND DESIGN DATA

Rao Desineni and Yan Pan, GLOBALFOUNDRIES
rao.desineni@globalfoundries.com

Identifying, quantifying, and eliminating systematic defects is critical to the profitability of integrated circuit (IC) manufacturing. Ramping logic yield, as compared to that of SRAM arrays, is especially difficult due to the irregular nature of the underlying physical design in advanced technologies. Double- and triple-patterning schemes, self-aligned via and metal-line strategies, and nonplanar transistor architectures such as FinFETs add extra complexity to yielding complex systems-on-chip (SOCs) that contain billions of logic gates. The increasing difficulty in profitably yielding SOCs, notwithstanding time-to-market and time-to-volume requirements on the foundries, has never been higher. As a result, rapid root-cause identification of logic failures is fundamental to the foundry and fabless business models.

With billions of transistors integrated on a typical SOC in advanced technologies, the diversity of random logic design polygons and their topological neighborhoods is immense. Because only a tiny fraction of these topologies is captured in the scribe-line macros, all the design-process systematics causing logic fails cannot be captured by analyzing (e.g., failure analysis, or FA) only scribe-line structures. Systematic defect-identification techniques based on analyzing inline wafer-inspection data are limited to only those defects that can be detected using scanning electron microscopy, e-beam, or other optical inspection methods. Layout-aware scan diagnosis enables localization of failure locations with much higher precision, meaning a smaller portion of the physical layout is provided as the target for FA. Most advanced layout-aware scan diagnosis software from reputed electronic design automation vendors further provide several extra FA guides, such as bounding boxes that highlight only the suspect layout polygons. This bounding box information can be fed into layout navigation tools such as Camelot to automatically drive FA tools to within-die physical locations. However, scan diagnosis resolution has always been challenging, meaning that the defect in the logic circuit cannot always be pinpointed to its physical location and the manufacturing process layer. Volume scan diagnosis techniques allow statistical analysis of layout-aware scan diagnosis results from multiple failing ICs, thereby mitigating the inherent diagnosis noise and improving the chances of success in identifying the root cause in FA. However, building a failure Pareto based on FA from multiple chips is not always the fastest option.

> "THERE IS A COMPELLING CASE FOR THE NEED FOR A FAST, FLEXIBLE, AND SCALABLE INFRASTRUCTURE THAT ENABLES BRINGING VARIOUS TYPES OF FAB MANUFACTURING PROCESS, TEST, AND DESIGN DATA TO ENABLE RAPID FA, LEADING TO FAST ROOT-CAUSE IDENTIFICATION."

The fab environment provides access to a large variety of data sources throughout the flow of wafer manufacturing process and test. From wafer manufacturing, these data types include, but are not limited to, lot logistics data (e.g., equipment, chamber, wafer slot position, q-time), inline measurement data (e.g., critical dimensions, overlay for all important processing layers), inline defect-inspection data, and electrical test data from inline scribe-line macros. From wafer and packaged modules test, data types include sort/bin test results (i.e., yield data), SRAM bitmap data, scan diagnosis data, statistical scoring results from volume diagnosis, and so on. It is possible, yet not always feasible, to store all these wafer-based data types in a common database inside the foundry. Somewhat orthogonal to wafer processing and test data

is all the design-related data (e.g., standard cell/core/memory usage, statistics and physical locations, transistor types and configurations, design-for-manufacturing scoring results, etc.) that are typically stored in separate databases. Another vital piece of information available to foundries is the historical yield-learning information, such as systematic defect signatures, FA reports, process or design fixes on prior products, and technologies. It is usually not practical to store such historical yield-learning information in easily retrievable databases along with other aforementioned data types. In most cases, just a simple lookup and correlation of scan diagnosis data with wafer-processing data, coupled with access to historical FA results, can serve as a surprisingly better filter than more complex statistical noise-reduction techniques used in volume diagnosis.

There is a compelling case for the need for a fast, flexible, and scalable infrastructure that enables bringing various types of fab manufacturing process, test, and design data to enable rapid FA, leading to fast root-cause identification. We built such a flexible infrastructure using the Python programming language and extensively leveraging open-source analysis engines. Our infrastructure brings together all the aforementioned data types. We routinely use this infrastructure and have (1) significantly reduced wasted FA requests by focusing only on high-yield-impacting failure types and not repeatedly submitting FA requests for known failure types, and (2) significantly improved the precision of the locations we request our FA teams to focus on, which has resulted in rapid root-cause identification.

ABOUT THE AUTHORS

Rao Desineni is currently a Distinguished Member of the Technical Staff/Director of Design Enablement at GLOBALFOUNDRIES, where his responsibilities include plug-in developer's kit validation, digital design reference flows, and design for test. Prior to joining GLOBALFOUNDRIES, Dr. Desineni was with IBM for six years in the role of integrated circuit yield manager for IBM's 300 mm manufacturing fab. He received his Ph.D. and M.S. degrees in electrical and computer engineering from Carnegie Mellon University in 2006. Dr. Desineni has broad research interest in the areas of chip design, manufacturing, and test. He currently holds 7 U.S. patents and has more than 30 research publications in IEEE and ASM International refereed conference proceedings and journals.

Yan Pan is a Product Diagnostics Engineering Manager at GLOBALFOUNDRIES' Fab 8 in Malta, N.Y. His work covers scan diagnostics, layout analysis and statistical volume diagnosis, and electrical fault isolation for advanced technologies at Fab 8. In addition, he leads an effort at Fab 8 to develop volume data analysis infrastructure to identify and resolve systematic yield issues using fab process, test, yield, and product design data. Dr. Pan received his Ph.D. and M.S. degrees in computer engineering from Northwestern University, Evanston, Ill., in 2011 and 2010, respectively. He holds 3 patents and has published more than 20 papers from his work at Northwestern and GLOBALFOUNDRIES.

NOTEWORTHY NEWS

ANADEF 2018

The 16th ANADEF Workshop will be held **June 5 to 8, 2018,** at Belambra Business Club, Seignosse-Hossegor (Landes), France. The conference addresses new issues related to the latest technological developments in electronic component failure analysis, presented through tutorials, plenary sessions, micro-workshops, as well as participation by equipment manufacturers and suppliers.

ANADEF, a French nonprofit scientific society established in 2001, meets biennially to bring together industry experts and mechanism scientists concerned with the prevention, detection, and failure analysis of electronic components and assemblies.

For more information, visit anadef.org.

ABOUT THE COVER

a) "Land of Delineation." Delineated silicon imaged with differential interference contrast microscopy. *Photo by Eric Cattey, NXP Semiconductors, Second Place Winner, Color Images.*

b) Ribbon of titanium. Peeling via liner due to residue on wafer postetch. *Photo by Lori Sarnecki, Fairchild Semiconductor, Second Place Winner, Black & White Images.*

c) Scanning electron microscopy image of a chip inductor lifted bond wire. The lifted wire was found after solder reflow and conformal coating. The bond wire lifted cleanly off the pad, with conformal coating observed along the bond interface. This indicated that the failure occurred prior to or during the conformal coating process. The temperature profile of the solder reflow process may have exceeded the required limit. False color was used to take advantage of the charging effect from the conformal coating. *Photo by Luigi L. Aranda, Raytheon, Second Place Winner, False Color Images.*

d) Warning: Psychedelic images may appear after extensive microscopic analysis! Visible light analysis of samples with very thin remaining silicon requires perfectly planar sample preparation. In this image, solder balls create interference patterns during VIS (660 nm) laser scanning microscopy of a cracked device. *Photo by Philipp Scholz and Heiko Lohrke, Technische Universität Berlin, Third Place Winner, Black & White Images.*

e) Optical image of broken bond wires on a field-effect transistor upon decapsulation. The majority of the bond wires were found to be fractured. *Photo by Richard Park, Raytheon, Third Place Winner, Color Images.*

f) Scanning electron microscopy image of a gold-germanium braze joint/substrate attach. False color was used to enhance the image, which resembles Santa Claus. *Photo by Andrew Ozaeta, Raytheon, Third Place Winner, False Color Images.*

All images from the 2016 EDFAS Photo Contest.

Visit the Electronic Device Failure Analysis Society website edfas.org

ELECTRONIC DEVICE FAILURE ANALYSIS™

A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS

INDEX OF ADVERTISERS

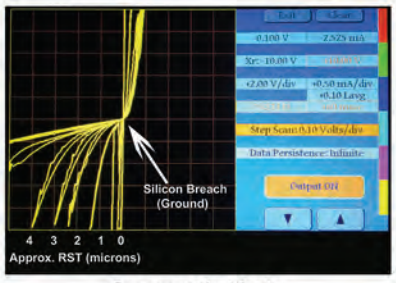
For advertising information and rates, contact:
Erik Klingerman, National Account Manager; tel: 440.840.9826;
e-mail: Erik.Klingerman@asminternational.org.
Current rate card may be viewed online at
asminternational.org/mediakit.

ULTRA THINNING

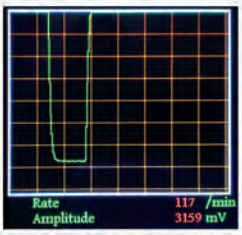
Converging Sample Prep & Analytical Methods

PEEC is a patent-pending system upgrade that uses electronic data, gathered from ASAP-1® IPS' polishing tip, to provide REALTIME through-silicon characterization of the device under test (DUT) – thus achieving a specific remaining silicon micron thickness (RST) in the low single digits, and below. PEEC is suitable for dies which have already been thinned below 20 microns and offers PARAMETRIC, PLOT and OSCILLOSCOPE modes to achieve a higher level of confidence than traditional "cut-image-then-cut-some-more" techniques, by removing the need to continually transfer the part between polisher and microscope. An Auto-Trip can be set to turn off the thinning process at a specific point.

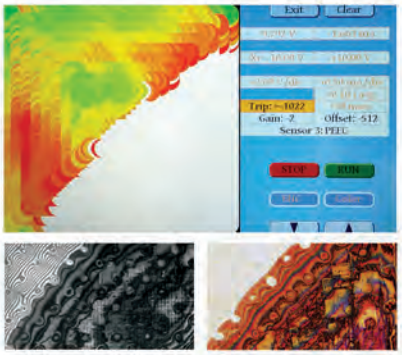
PEEC PROVIDES THE ANALYTICAL TECHNIQUES... YOUR DEVICE PROVIDES THE ANSWER!



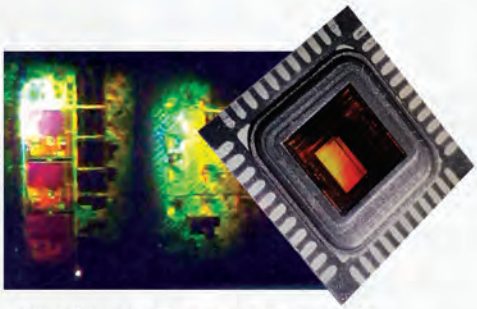
Parametric Mode



'Soft' Oscilloscope Mode



NIR and VISIBLE Images show the same position on the Plot screen for silicon breach.



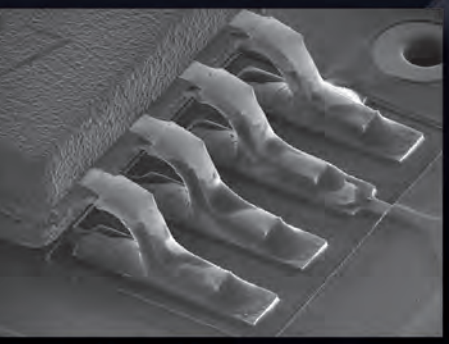
Ultrathinned silicon dies at <2um RST.
Imaged with visible light, showing circuitry.

ULTRA TEC MANUFACTURING, INC.

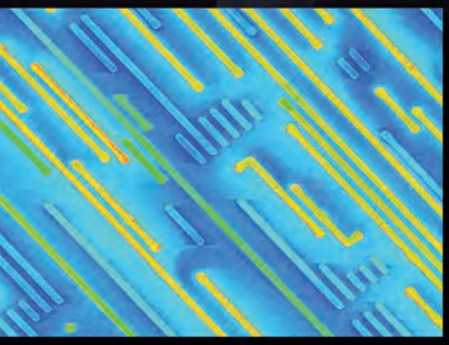
Toll Free (US) 1-877-542-0609
Tel: 1-714-542-0608 Fax: 1-714-542-0627
e-mail: info@ultratecusa.com
www.ultratecusa.com

UNLOCK THE ANSWERS

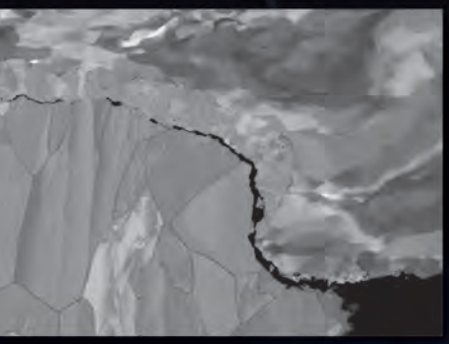
TO YOUR FAILURE ANALYSIS QUESTIONS WITH



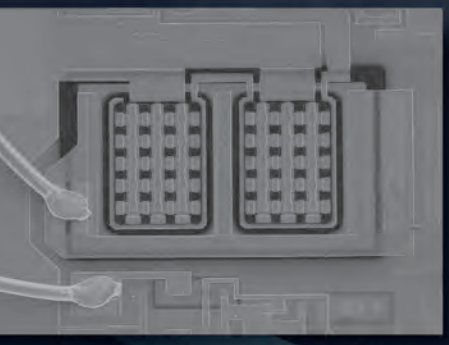
SEM Image of Semiconductor Device



Passive Voltage Contrast (PVC)
image of semiconductor device



Backscatter Electron (BSE)
image of Wire Bond Cross Section



Electron Beam Induced Current (EBIC)
Image of Semiconductor Device

SMART
FLEXIBLE
POWERFUL

SEM

Questions about...

- *Fatigue?*
- *Corrosion?*
- *Fracture?*
- *Delamination?*
- *Layer Integrity?*
- *Interfaces?*

Come see how JEOL high resolution, analytical Scanning Electron Microscopes and precision Cross Section Polishers help you get answers.

Visit jeolusa.com/jeolfa

JEOL
Solutions for Innovation

salesinfo@jeol.com