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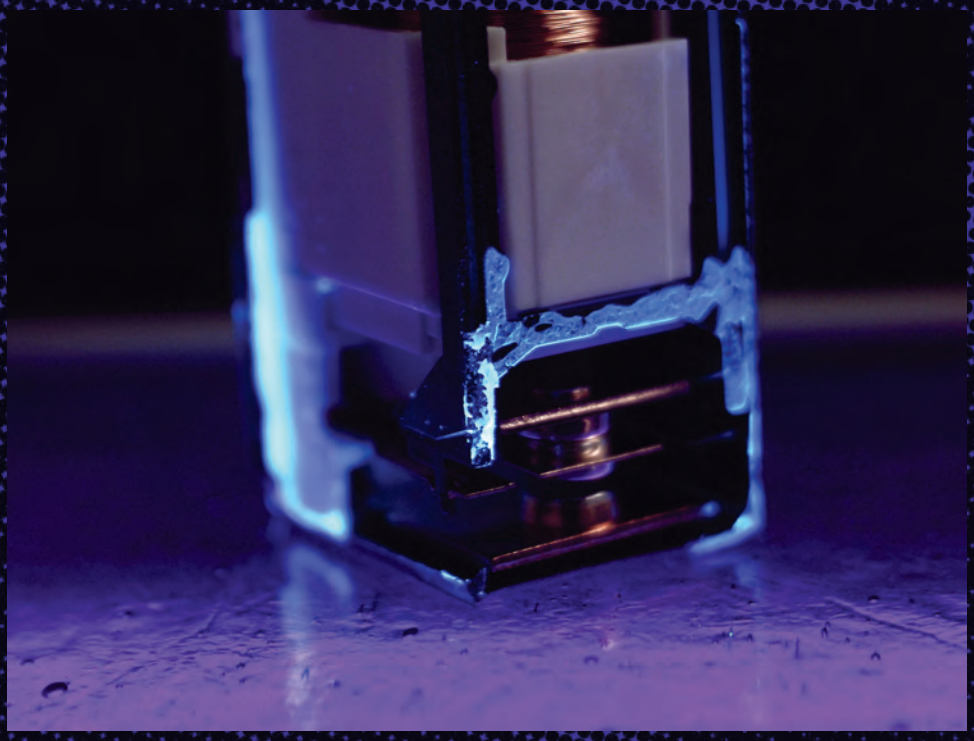

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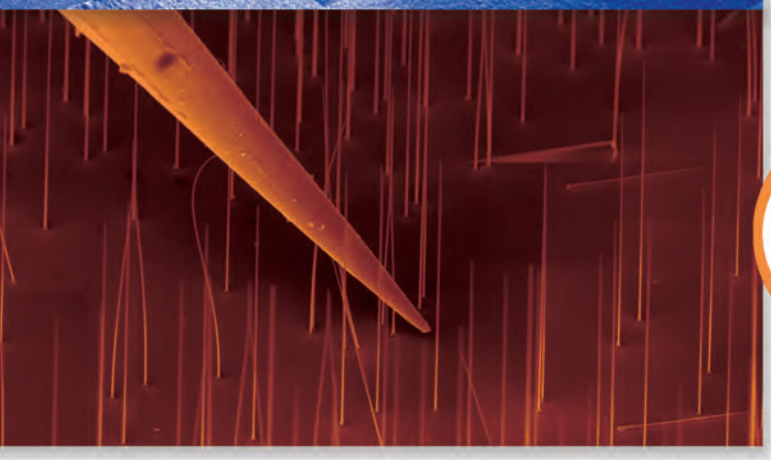

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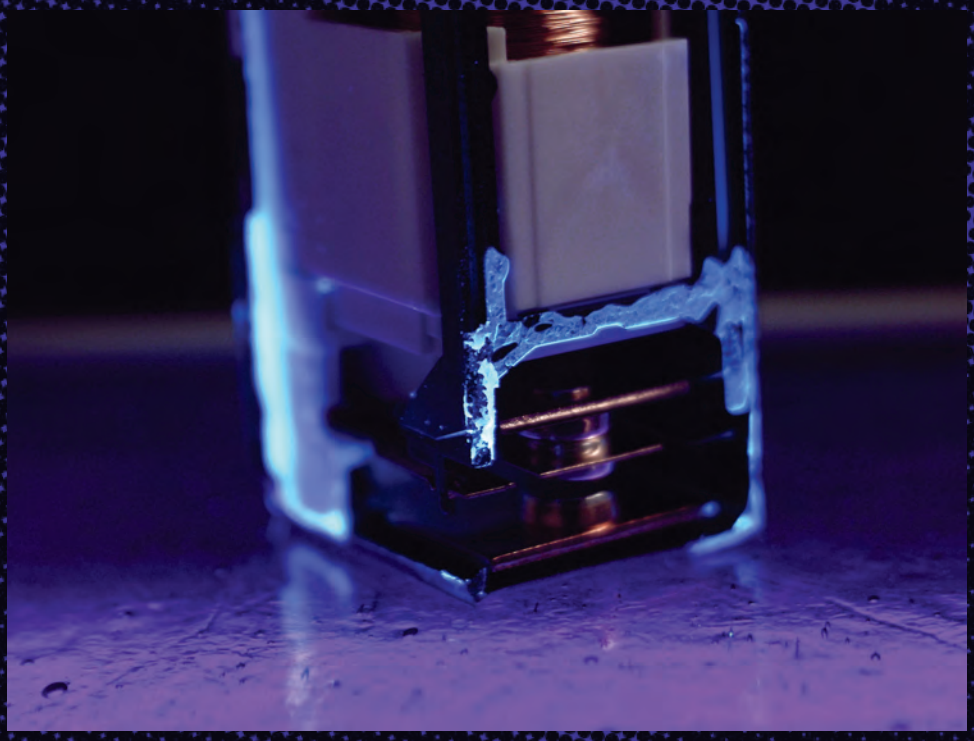

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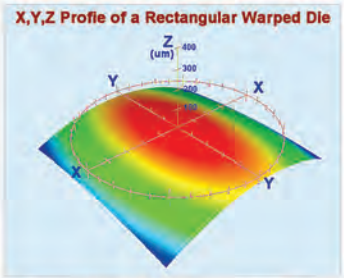

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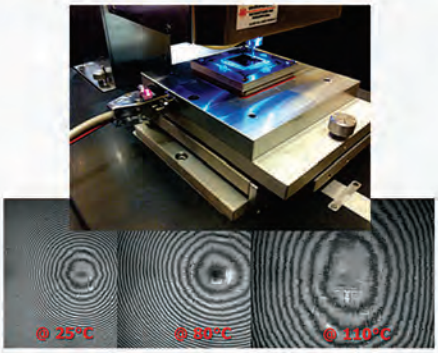

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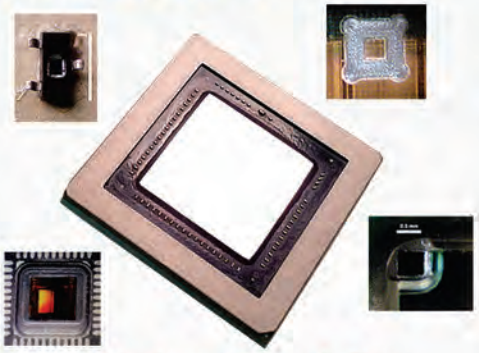

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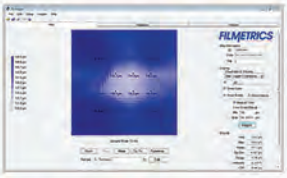

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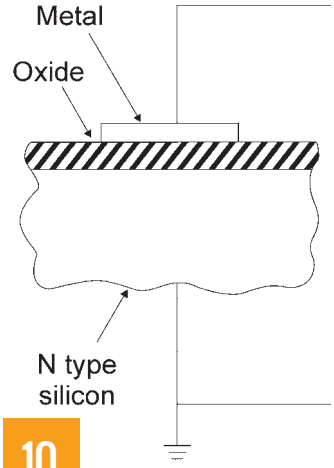

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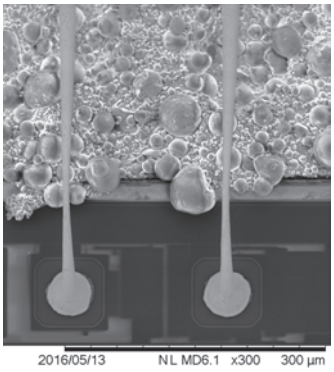

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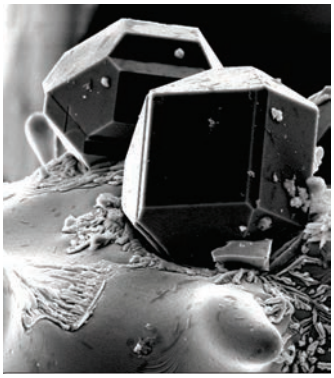

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ABOUT THE COVER

Conformal coat adhered the actuation arm to the lid, preventing the relay from switching. *Photo by Jordan Hendricks, Hi-Rel Laboratories, First Place Winner in Color Images, 2016 EDFAS Photo Contest.*

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ELECTRONIC DEVICE FAILURE ANALYSIS™
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PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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The ever-changing semiconductor industry and the diversity and dynamics of the electronic failure analysis community require the leaders of the Electronic Device Failure Analysis Society (EDFAS) to reassess value propositions and realign accordingly the directions we are heading on a timely basis.

We just finished our Board of Directors' face-to-face meeting during the 2016 International Symposium for Testing and Failure Analysis (ISTFA) in Fort Worth, Texas, where we defined our EDFAS strategic objectives. As shown below, our strategic objectives are centralized on "strengthen our member resources and grow," with focuses on three major areas: membership growth, technical excellence, and strategic collaboration and partnership.

EDFAS Strategic Objectives

Strengthen Our Credential and Grow

☐ **Membership:**

- Improve EDFAS brand credential and awareness by communicating through global networks
- Strengthen EDFAS forward-looking "product roadmap" to bring services and items of value to members and make them easily accessible through website and social media
- Develop a tailored membership model to encourage "new-career" and international professionals

☐ **Technical Excellence:**

- Ensure ISTFA is the premier conference and exhibition for the global electronic failure analysis industry
- Enhance *EDFA* magazine and desktop reference technical content as the "go-to" sources for global electronic failure analysis industry
- Establish EDFAS technical leadership through education beyond just the means of ISTFA conference

☐ **Strategic Collaborations and Partnership:**

- Establish a FA technology roadmap by collaborating with semiconductor and equipment manufacturing institutes

(continued on page 24)

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FAILURE ANALYSIS ON SOLDERED BALL GRID ARRAYS: PART I

Gert Vogel, Siemens AG, Digital Factory Division, Control Products, DF CP QM SQA 5
gert.vogel@siemens.com

Ball grid arrays (BGAs) are widely used on complex printed circuit board assemblies (PCBAs). Ball grid arrays are a type of surface-mount package, where it is not possible to directly visually inspect solder connections because they are hidden as an array of small solder balls underneath the devices. X-ray imaging can be used to automatically control the balls regarding soldering faults, but this only provides information about failure types that lead to a deformation of the balls, such as electrical short circuits or voids in the soldered balls.

A detailed analysis of these failures—and also other types of failures that are only accessible by electrical measurements—can usually be conducted only through destructive physical analysis, which involves cross sectioning solder joints. However, BGAs can have more than 1,000 solder balls, and not every type of failure can be identified by taking a cross section.

This article demonstrates new approaches to failure analysis on BGA balls as well as the related failure analysis on printed circuit boards (PCBs).

INTRODUCTION

Failures of BGAs on PCBAs are primarily related to the solder connection and not to a problem at the silicon level.

There are failures that can be measured electrically, such as short circuits or open circuits in the array of solder balls, as well as failures found by performing an x-ray inspection. For example, voids do not represent an immediate threat but are a long-term quality risk. (A failure is defined as a void percentage of more than 30% of the ball area in the x-ray image, in accordance with IPC-A-610, "Acceptability of Electronic Assemblies.")

Voids such as these in the solder joints of BGAs are very aggravating because they normally cannot be repaired by simply resoldering; even replacing an expensive component with a new one is not always successful. A recourse against the supplier is usually futile because many factors may be responsible for these types of failures. In most cases, the supplier is right. Even if deep oxidized needle indents in a singular instance can be responsible for voids in BGA balls, the balls are not normally responsible for these types of failures.

"THIS ARTICLE DEMONSTRATES NEW APPROACHES TO FAILURE ANALYSIS ON BGA BALLS AS WELL AS THE RELATED FAILURE ANALYSIS ON PRINTED CIRCUIT BOARDS (PCBs). "

FAILURE ANALYSIS OF SOLDER JOINTS THAT CANNOT BE VISUALLY INSPECTED

A further complication when analyzing failed BGA balls is that the solder joints cannot be visually inspected. Therefore, obtaining information about the location of an open or short circuit is only possible by making electrical measurements or by performing an x-ray inspection.

Experience shows that the PCB is predominantly the main source relating to problems involving soldering of BGA balls; however, the solder paste or the soldering process itself can also be responsible for problems. Process problems such as oxygen intrusion during reflow can lead to so-called "champagne voids," which are many small voids on the interface between the solder material and the pad metallization (Fig. 1). The inadvertently added oxygen consumes a high amount of the reducing organic acids from the flux in the solder paste, which was balanced for use under nitrogen atmosphere. If all of the acid is consumed, a web of remaining tin oxide, originating from the grain boundaries of the solder balls, blocks the escape of the gas bubbles that develop. Such a root

cause can only be revealed by thoroughly controlling all of the parameters of the soldering process. Another clue is the optical appearance of the solder balls after a second reflow process, which is manifested by a creased skin of tin oxide (Fig. 2).

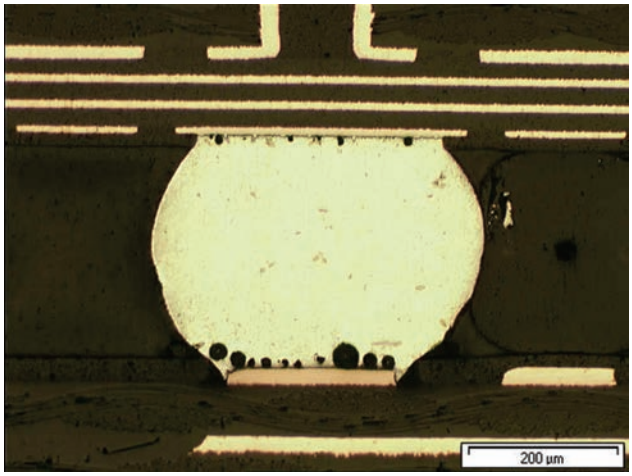

Fig. 1 **Cross section through a BGA ball with so-called "champagne voids"**

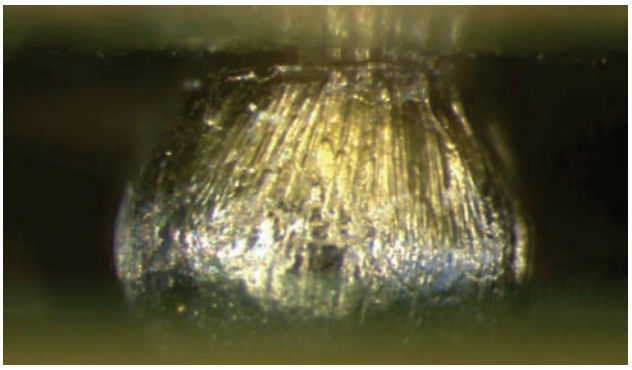

Fig. 2 **BGA balls with champagne voids manifest a creased skin after a second reflow.**

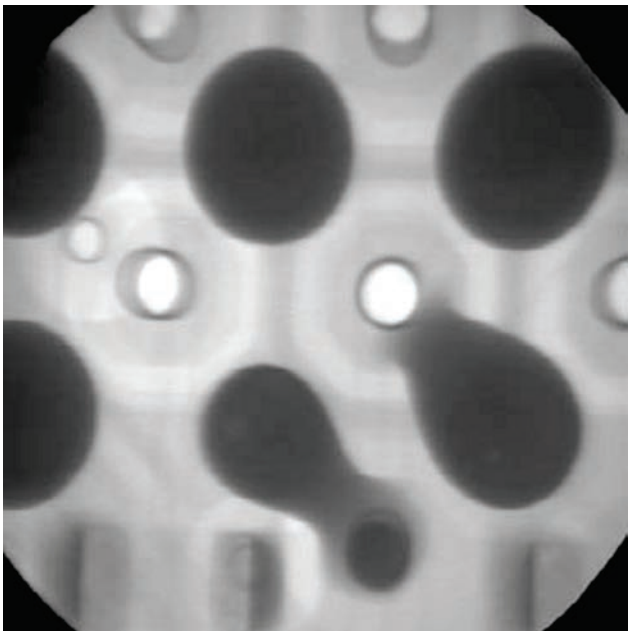

Fig. 3 **X-ray image of solder faults at BGA balls**

With several special preparation techniques, many different sources of voiding can be clarified. The goal of the analysis is always to clarify the root cause of the failure so that it can be eliminated in the future. If the root cause has been clearly identified, then an additional benefit is that it may be possible to make a claim against the supplier.

ELECTRICAL FAILURES WITH EYE-CATCHING X-RAY OBSERVATIONS

Even if electrical shorts are easily detected by performing an x-ray analysis, the determination of the root cause can still be very complicated. The following example shows very clearly the short circuit between BGA balls and adjacent through-holes in the x-ray image (Fig. 3) as well as in the cross section (Fig. 4); however the root cause must be searched for in the PCB. A bad immersion tin rework underetched the solder resist around openings. It became brittle and flaked off, exposing bare copper that facilitated the flow of liquid solder across the clearance to the adjacent contacts (Fig. 5).

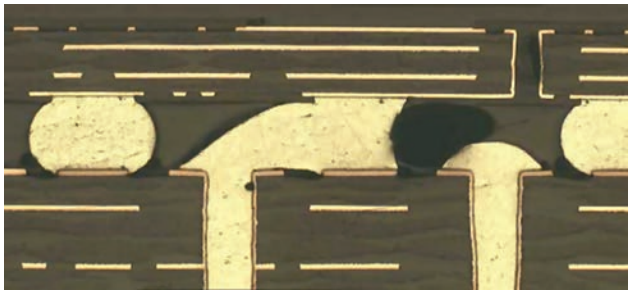

Fig. 4 **Cross section of the solder faults from Fig. 3. Short circuits caused by flowing solder as a result of missing solder resist**

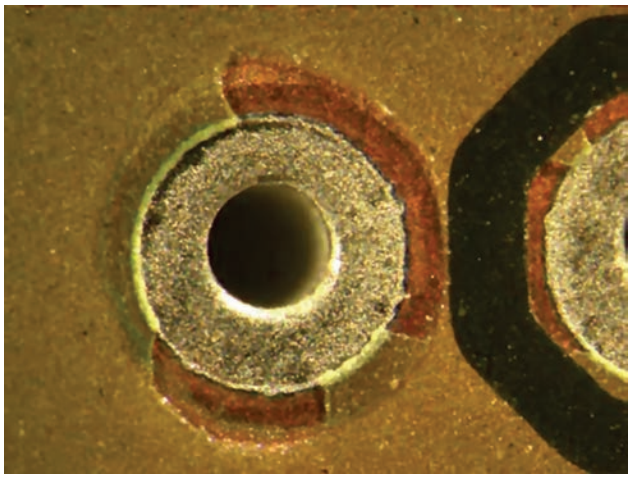

Fig. 5 **Microscopic inspection of the surface of the PCB reveals faulty solder resist. Underetched films broke off, caused by a bad immersion tin rework.**

PLANE PARALLEL POLISHING OF A BGA TO OBTAIN JUST THE BALLS

If x-ray analysis and optical microscopy provide no clues for why there is an open circuit between BGA balls and the PCB, if different sizes of BGA balls are visible, or if the BGA is sensitive to coolant spray (intermittent open), then a more drastic approach may be advisable than just a simple cross section through some of the solder joints. If you want to analyze those joints, and something prevents you from looking at them, then remove anything that hinders you. This means grinding and polishing away the complete BGA, leaving only the balls (Fig. 6). After this procedure, one can use a needle to verify whether the solder joint is mechanically stable, and every ball can also be inspected from every direction (Fig. 7). A cross section can still be obtained through the PCB and the solder ball.

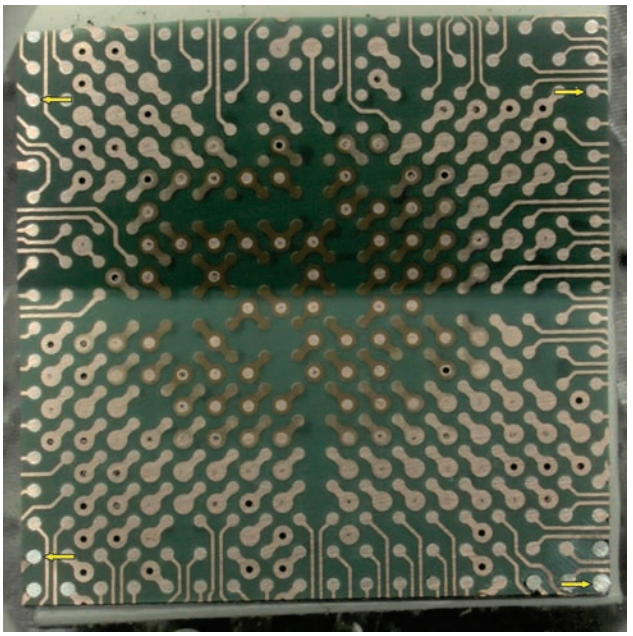

Fig. 6 **Removal of the body of the soldered BGA by polishing it down from the top of the BGA. Preparation by plane parallel grinding of the BGA shows some warpage in the soldered BGA. On the left, the PCB of the BGA has already been polished down to the silvery, shining top of the first balls.**

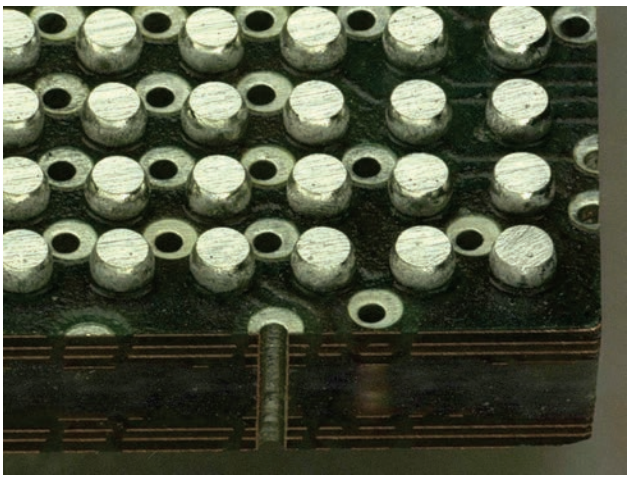

Fig. 7 **After exposing all of the balls and blowing away the rest of the solder resist, the balls can be inspected from all sides. No soldering problems were identified.**

The grinding down and polishing of a BGA with an area of several square centimeters is not as complicated as it may appear. It can be done by hand with an accuracy of better than 10 µm, because a multitude of copper layers in the BGA help the operator keep in parallel. As soon as the first shiny, silvery small dots appear, one must be very careful, because the last layer of the BGA has been reached. The solder resist around the solder balls cannot be polished away but must be blown off.

The solder balls of the BGA in Fig. 8 manifested different diameters when performing the x-ray inspection. Preparation by grinding down the BGA reveals the root cause: There are no flux residues around the balls having a smaller diameter. This means there is only the solder material of the BGA ball but no printed solder paste, probably because the stencil was dried out and clogged.

TYPICAL ERROR PATTERN: COLD JOINT

An electrical open circuit was found in the next case. An x-ray examination showed no abnormalities. The BGA was polished down, and just before blowing off the solder resist, a lost solder ball was identified (Fig. 9). Detailed inspection showed that two balls dropped away. The solder pads showed no flux and no solder paste (Fig. 10).

(continued on page 8)

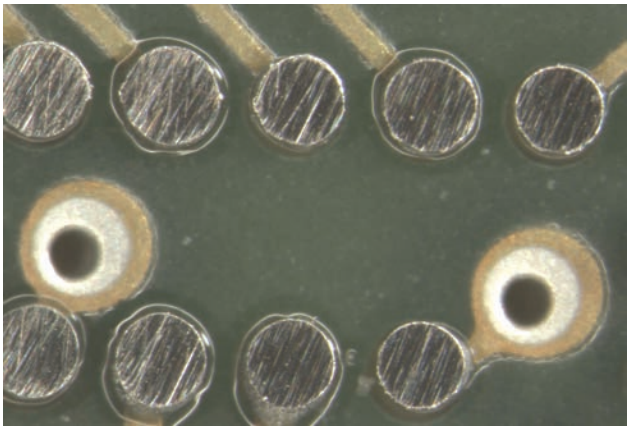

Fig. 8 **In this case, the root cause for varying sizes of the solder balls can easily be seen. Around some balls there are no residues of flux. These balls also have a smaller diameter, which means that no solder paste was printed at these locations.**

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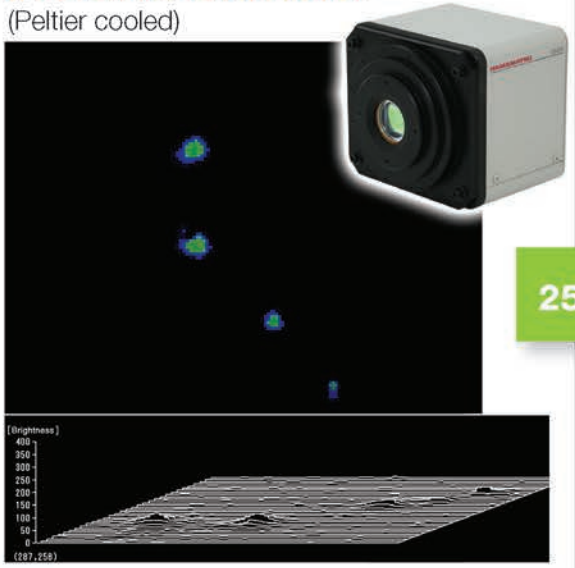

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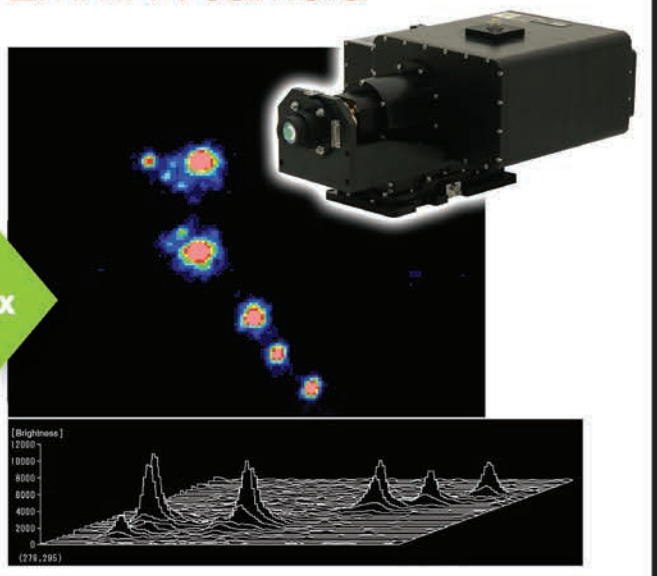

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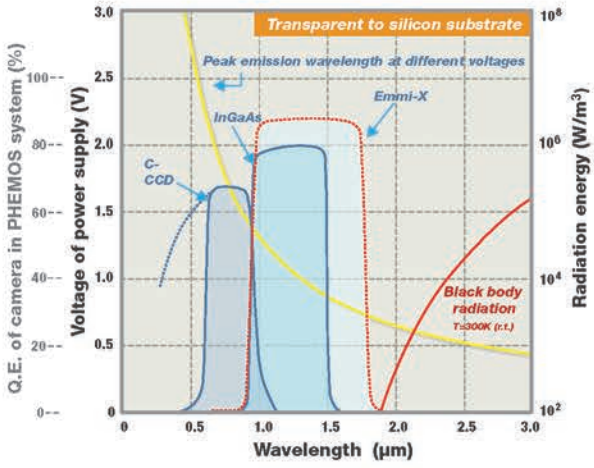

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FAILURE ANALYSIS ON SOLDERED BALL GRID ARRAYS: PART I *(continued from page 6)*

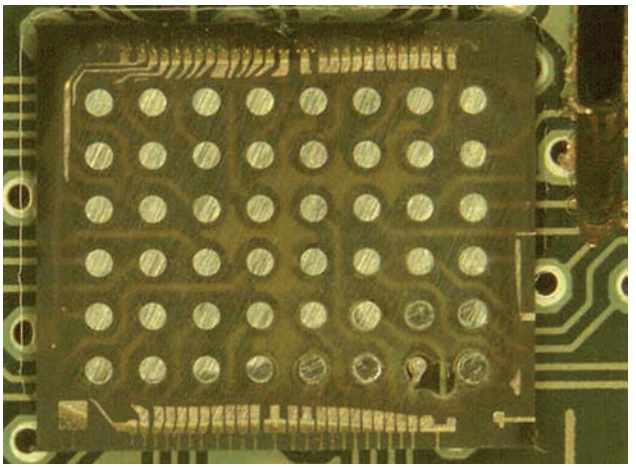

Fig. 9 **After grinding down the BGA and before blowing away the residue of the solder resist from the bottom of the BGA, it was discovered that one ball had dropped off.**

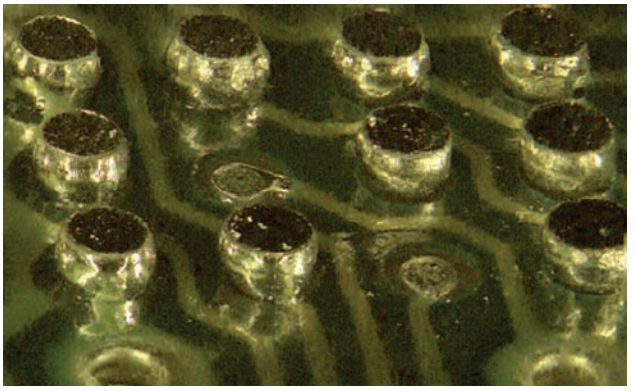

Fig. 10 **After blowing away the residue of the solder resist, two missing balls can be seen.**

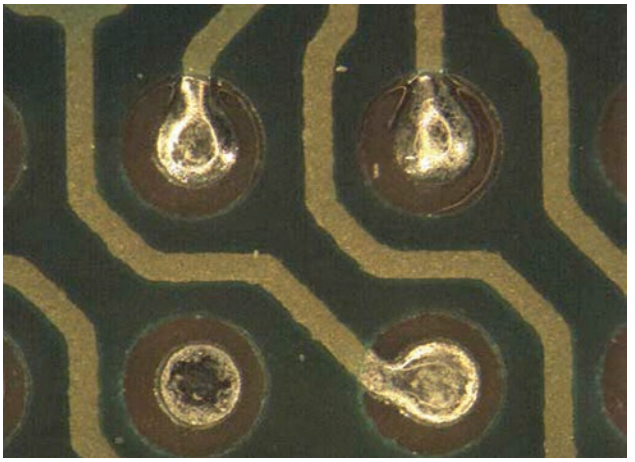

Fig. 11 **The faulty solder print can also be seen on a printed pattern with the same geometry next to the defective BGA.**

The difference from the BGA in Fig. 8 is that the molten solder ball did not wet the surface of the PCB land. The faulty solder print could also be identified next to the defective BGA on a bare printed pattern without an assembled BGA (Fig. 11). Once again, the root cause of the failure was a dried-out, clogged stencil while printing the solder paste.

SUMMARY

Based on a number of case studies, it was shown that failure may originate at a number of steps in the manufacturing process, for example, from the solder paste printing process or from the soldering process itself. The stencil printing of the solder paste is often a critical process, but more often, the root cause is faulty PCBs.

Cross sections of soldered BGAs are common for failure analysis. One new approach is presented as an additional method in the course of finding the root cause of failures. Grinding away the corpus of the BGA until the soldered balls are still left on the PCB can provide insight into the failure mechanism.

In the case of perfect solder connections, grinding the PCB from the backside is another approach, which will be discussed in Part II of this article in the May issue of *EDFA*.

ABOUT THE AUTHOR

Gert Vogel studied physics in Stuttgart. He has been with Siemens for more than 30 years. Dr. Vogel was a semiconductor technologist in Siemens' DRAM production in Munich and Regensburg for seven years. He then moved to Siemens Amberg where, among other topics, he is a specialist in failure analysis of electronic components on printed circuit board assemblies. He led a tutorial, "Avoiding Flex Cracks in Ceramic Capacitors," at ESREF 2015. This was followed by a tutorial, "Creeping Corrosion of Copper on Printed Circuit Board Assemblies," at ESREF 2016.

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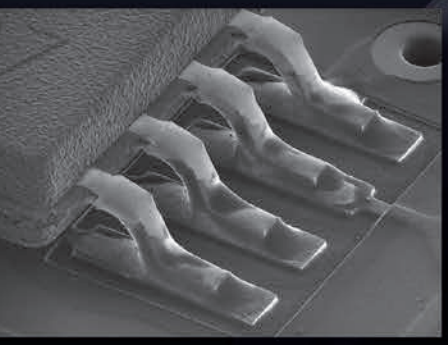
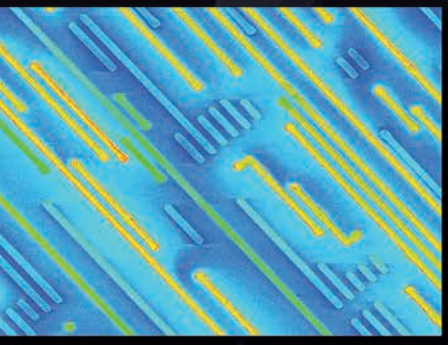
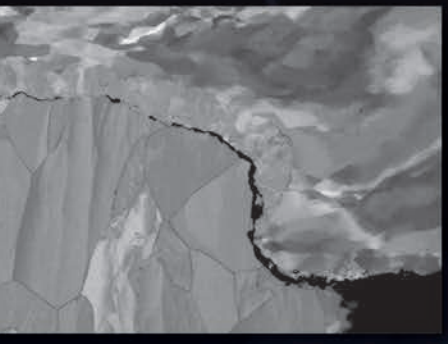


SEM Image of Semiconductor Device



Passive Voltage Contrast (PVC)
image of semiconductor device



Backscatter Electron (BSE)
image of Wire Bond Cross Section

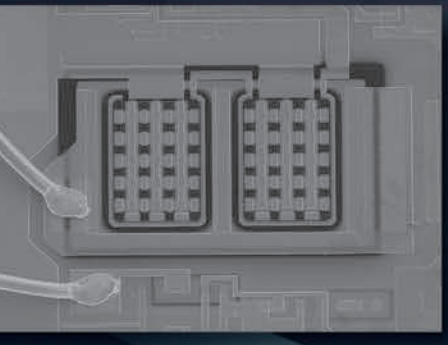


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Image of Semiconductor Device

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TRAPS AND CHARGES

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Important oxide characteristics are skipped over briefly in basic descriptions of MOS operation. Oxide is not even mentioned in descriptions of bipolar devices. In fact, oxide and alternate insulators are critical to semiconductors. Identifying, avoiding, or eliminating inherent problems was, and still is, a major focus for process development.

At the time of the first lunar landing, mobile charges in oxide were an important factor that limited reliability. Today, modern processes and device design have largely eliminated mobile charge failures. However, the mobile charge failure mechanism remains and could reappear any time our defenses lapse. Mobile charge is designated Q_m.

Oxide traps, however, are more important than ever. Q_f, Q_{it}, and Q_{ot} are designations for three types of oxide traps.

MOBILE IONS

Sodium and potassium ions have a positive charge and move readily in silicon dioxide under influence of an electric field. The electric charge of mobile ions has maximum effect when located near the underlying silicon.

Capacitance-voltage (CV) plotting is used during fabrication to detect and measure the existence of mobile ions. CV plotting is also a good way to understand the behavior of mobile ions in oxide. A simple capacitor is shown in Fig. 1(a), while typical CV plots are shown in Fig. 1(b). The plots show capacitance corresponding to different direct-current voltage applied to the metal dot. At sufficiently negative applied voltage, electrons are repelled from the surface of the silicon, causing a *P*-type inversion layer. Measured capacitance is low because the effective thickness of the capacitor is the oxide thickness plus the inversion layer thickness. At higher applied voltage, the inversion layer disappears. The effective insulator thickness is equal to the oxide thickness alone, and the capacitance increases correspondingly.

Sodium ions have mobility in oxide even at room temperature. In the absence of an applied field, ions in the oxide will spread evenly through the oxide. Mobile ions

"TODAY, MODERN PROCESSES AND DEVICE DESIGN HAVE LARGELY ELIMINATED MOBILE CHARGE FAILURES. HOWEVER, THE MOBILE CHARGE FAILURE MECHANISM REMAINS AND COULD REAPPEAR ANY TIME OUR DEFENSES LAPSE."

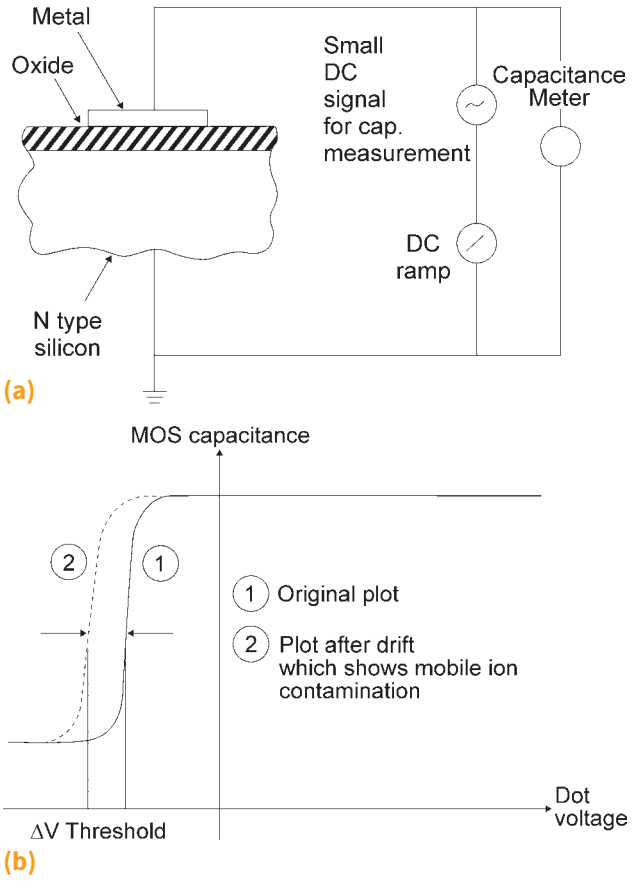

Fig. 1 **(a) Simple capacitor. (b) Two CV plots of metal oxide silicon structure. Plot 1 taken on sample as-fabricated; mobile charge is distributed throughout oxide. Plot 2 taken after high-temperature drift; mobile charge is focused at oxide/silicon interface.**

diffuse away from regions of high concentration. The like charge of mobile ions causes them to repel each other. The original plot in Fig. 1(b) was taken while mobile charges were evenly distributed. The step increase in capacitance identifies the threshold voltage required to produce the inversion layer.

Plot 2 in Fig. 1(b) was taken after a positive-voltage high-temperature step to drift any positive ions down to the silicon surface. Only a few seconds at 300 °C are required to accumulate near the surface of the silicon. After drifting ions toward the silicon, the capacitor was allowed to cool under bias. Plot 2 was taken while ions were focused near the silicon surface, where their effect is at maximum. A greater negative voltage must be applied to overcome the positive mobile ion and cause inversion. The threshold voltage has shifted.

The difference in threshold voltage is a measure of mobile ions present. The randomly uniform distribution of mobile ions can be restored by baking without bias at 300 °C for a few seconds or at 125 °C for 24 h.

MOBILE IONS IN *PNP* TRANSISTORS

Failures of very early *PNP* devices illustrate more characteristics of mobile ions. Actions to avoid *PNP* failures verify our conclusions. Figure 2 is a cross section of a 1970 transistor. In normal operation, the base is biased at a voltage higher than the collector voltage. An electric "fringe" field exists in the oxide above the base/collection junction. Mobile ions in the vicinity move away from the base toward the collector. In time, mobile ions concentrated at the silicon surface attract electrons and invert the silicon surface. As a result, the base spreads out into the previous collector area. The electric fringe field moves to the new junction and expands the inverse further. Figure 3 shows the expanded base. At this point, transistor parameters do not change drastically. The new junction adds a small amount of leakage current. Breakdown of the new diode is usually higher than the original collector/base diode.

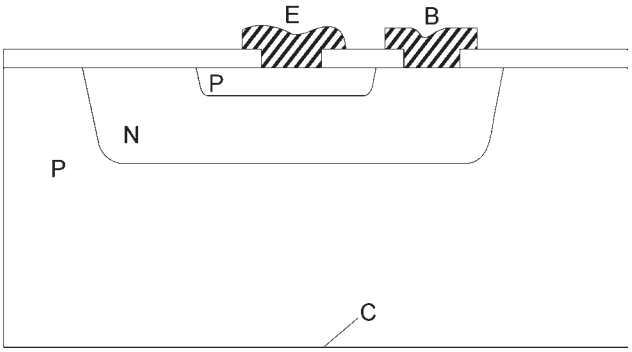

Fig. 2 **Schematic cross section of basic *PNP* transistor**

However, the inversion ultimately reaches the edge of the silicon chip. Current flows directly from base to collector through the inversion layer. The edge of the chip provides a leakage path. The collector/base I/V characteristic becomes a classic channel current.

A first attempt to avoid channel current was to add a P^+ "channel stop." The idea was that the *P* ring would be too highly doped to allow inversion. In fact, the edge of the heavily doped *P* ring did invert. The depth of the inversion was so shallow that electrons simply tunneled through[1] (Fig. 4).

A successful remedy was to add a metal ring contacted to the *P* ring. The metal and the silicon directly below are at the same voltage. No electric field exists under the ring. Lacking an electric field, the inversion cannot expand under the metal (Fig. 5).

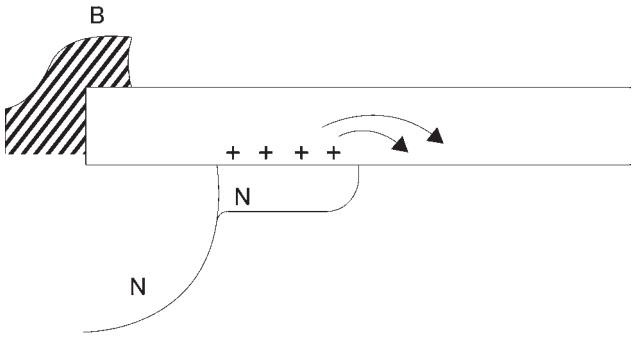

Fig. 3 **Schematic cross section showing inversion induced by mobile charge. Electric fringe field is associated with the new junction edge.**

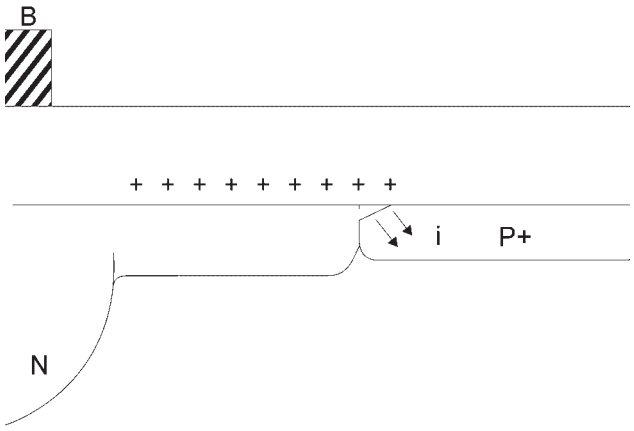

Fig. 4 **Schematic cross section showing tunnel current at edge of ineffective P^+ channel stop. The inversion cannot proceed, but the leakage path is established.**

MOBILE IONS IN ICs

The following three corrective actions have made such failures rare:

- Cleaner fabrication minimizes mobile ions.
- Processes include phosphorus glass, which "getters" mobile ions. That is, phosphorus glass effectively locks mobile ions safely away from critical oxide.
- Nitride and metal elements act as barriers to mobile charge. Mobile ions cannot penetrate nitride films.

While steps to avoid IC failure are overwhelmingly successful, it is clear that under unique conditions, mobile ions could cause fatal leakage between isolated *n*-wells or threshold shifts in MOS transistors. Mobile ions must be considered a possible cause for bake-recoverable failures. Look for cracks or misalignments that defeat steps to control mobile charge.

OXIDE-TRAPPED CHARGES

Three categories of charges are associated with traps or oxide defects:

- *Fixed charge (Q_f):* Incomplete oxidation of silicon leaves a positive charge by failures of very early *PNP* devices approximately 2 nm above the interface to the silicon. Crystal structure makes the fixed charge lower for 100 silicon material than for 111 material. (Q_f was labeled Q_{ss} in early publications.)[2]
- *Interface charge (Q_{it}):* Q_{it} is similar to Q_f if located at the interface to the silicon, and it can be either positive or negative. Electrons and hydrogen can be trapped at these locations. This charge is sensitive to oxidation details, such as temperature and the presence of oxygen. A hydrogen anneal is often used to minimize charge. Process variations to achieve a high-k dielectric, such as addition of hydrogen and hafnium, also affect Q_{it}.
- *Trapped oxide charge (Q_{ot}):* A broken silicon-oxygen bond can occur anywhere in an oxide film. Traps can be created during oxide growth or at any later time. High-energy events such as radiation, plasma processing, hot carrier injection, and simple oxide current can create oxide traps, which present a preferred path for oxide current. Thus, traps are involved in time-dependent dielectric breakdown and electrostatic discharge failure.

OXIDE FAILURE

As suggested previously, gate oxides are susceptible in many ways to failure or degradation due to an excess of oxide traps. Gate leakage or threshold changes can cause function failures, timing failures, and many other failures.

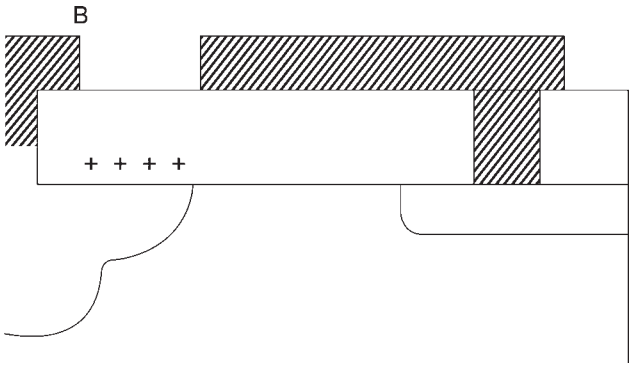

Fig. 5 Schematic cross section showing successful channel stop. Electric field is eliminated by guard ring.

Identifying the cause of failure depends on identifying exactly what failed, when it failed, and under what circumstances. A considerable amount of data may be required to conclude the cause of failure. More than a single failure is required to accomplish this.

Plasma etching is known to damage oxides.[3] Voltage is built up due to unequal exchange of positive and negative ions. The degree of charging is a function of processing variables. Circuit layout is critical. Layout controls the exposure of gate oxides to damaging discharge current. The key to analysis may be the observation that damaged oxide is, or is not, connected to material that acts as an antenna for charge. Design rules limit the amount of poly or metal allowed to act as an antenna for gate oxide.[4] Diodes are often added solely to protect gate oxide by shunting plasma-induced current away from vulnerable oxide.

Gate oxides are degraded by current flow from any cause. Excess voltage can be caused by circuit configuration or external probing. In addition, excess voltage can be caused by reactive ion etch during decapsulation for failure analysis.

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ABOUT THE AUTHOR

David Burgess is a failure analyst and reliability engineer. He developed techniques and taught in those areas at Fairchild Semiconductor and Hewlett-Packard. He is the founder of Accelerated Analysis, a manufacturer and distributor of specialty failure analysis tools. David is the co-author of *Wafer Failure Analysis for Yield Enhancement*. A graduate of Rensselaer Polytechnic Institute and San Jose State University, he is a member of EDFAS and has served on various ISTFA committees. David is a Senior Life Member of IEEE and was General Chairman of the 1983 International Reliability Physics Symposium (IRPS).

NOTEWORTHY NEWS

2017 FIB/SEM WORKSHOP

The tenth annual FIB/SEM Workshop will be held on **Thursday, March 2, 2017,** at the National Institute of Standards and Technology (NIST) in Gaithersburg, Md. It features a full day of technical content and plenty of opportunities for informal discussion with your FIB colleagues.

For more information, contact the following organizers: Nabil Bassim, bassimn@mcmaster.ca; Ken Livi, klivi@jhu.edu; or Keana Scott, keana.scott@nist.gov.

NOTEWORTHY NEWS

2017 IRPS CONFERENCE

The IEEE International Reliability Physics Symposium's (IRPS) annual conference will be held **April 2 to 6, 2017,** at the Hyatt Regency in Monterey, Calif.

The IRPS technical program includes technical sessions, keynote and invited talks on emerging issues, tutorials, workshops, an evening poster session, a year-in-review seminar, panel discussions, and equipment demonstrations. Special attention is given to the reliability of advanced CMOS scaling, new materials introduction, new processes or integration strategies, and/or fundamentally new device architectures. Attendees returning from the IRPS will be better equipped to solve critical reliability problems and develop effective qualification procedures that affect their companies' bottom line.

The IRPS Conference is sponsored by the IEEE Reliability Society and IEEE Electron Device Society. For more information, visit the IRPS website at irps.org.

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AN EVALUATION OF CORROSION INHIBITORS FOR USE IN ACID DECAPSULATION OF SAMPLES WITH SILVER BOND WIRES

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BACKGROUND

In previous literature on decapsulation of integrated circuits with silver bond wires,[1] a 2.2% Lugol's solution (potassium iodide and iodine in water) was mixed in bulk with fuming nitric acid and used as an etchant in both hand decapsulation and with an automatic decapsulation system. The freshly mixed etchant worked well, but after 30 to 45 min, the bond pull strength dropped off, reaching zero at 2 h. The bond pull tests showed peak forces at approximately the 1:30 mix ratio, with the pull force dropping off at both higher and lower ratios.

The mechanism of protecting the silver wires has been assumed to be the result of a coating of silver iodide that forms on the wire.[1] This could either be the result of a reaction between silver nitrate and potassium iodide:

$$Ag + 2HNO_3 \rightarrow AgNO_3(s) + NO_2(g) + H_2O:AgNO_3 + KI \rightarrow KNO_3(aq) + AgI(s)$$

or the direct reaction between silver nitrate and iodine:

$$2AgNO_3(s) + I_2 + 4H^+ \rightarrow 2AgI(s) + 2NO_2(g) + 2H_2O$$

Both cases will produce a porous silver iodide coating that is not very soluble in fuming nitric acid. It should be noted that silver nitrate is only slightly soluble in fuming nitric acid but is highly soluble in water. Because water is produced during the digestion of the encapsulant, it may be locally in high concentrations.

The characterization of the iodine transport and reaction on the wire is necessary to optimize reagent concentrations at these active surfaces and to stabilize the process results in relationship to the age of the etchant. An etchant is needed, or a means of mixing at the point of use, that provides optimum and repeatable wire protection without shelf life concerns.

IODINE TRANSPORT

The addition of Lugol's solution to fuming nitric acid introduces iodine as iodide (I^-) and tri-iodide (I_3^-). The introduced iodine will react with the nitric acid, creating additional species. The possibilities are dissolved elemental iodine created by the oxidization of I_3^-, iodide (I^-), and iodate (IO_3^-). Upon contact between the fuming nitric acid and the Lugol's solution, I_3^- oxidizes to I_2, which is further oxidized to iodic acid:

$$I_2 + 10HNO_3 \rightarrow 2HIO_3 + 10NO_2 + 4H_2O$$

A second reaction takes place between the iodic acid and iodide:

$$IO_3^- + 5I^- + 6H^+ \rightarrow 3I_2 + 3H_2O$$

The iodine created is oxidized to iodic acid, and the cycle continues until the only species left is iodate. At the mix ratios in Ref 1, iodate will be at a concentration of 0.438 mol/L of acid, and NO_2 will be five times higher. This produces enough NO_2 to generate a definite yellow color to the mixture. The reactions also create a lot of water, approximately 4 mol of water for each mole of iodine. In total, the water content of the Lugol's solution and the water from the reactions will add approximately 4% water to the etchant.

Some literature indicates that the solubility of iodine in nitric acid is fairly high.[2,3] One paper suggests that

(continued on page 16)

> "IT MAY BE POSSIBLE TO OBTAIN BETTER WIRE PROTECTION WITH LOWER IODINE CONCENTRATION, BUT THE REACTIVITY WITH THE WIRES AS SHOWN AT HIGHER CONCENTRATIONS MAY INDICATE A VERY LIMITED PROCESS RANGE AND LACK OF STABILITY."

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14 nm device with spacing
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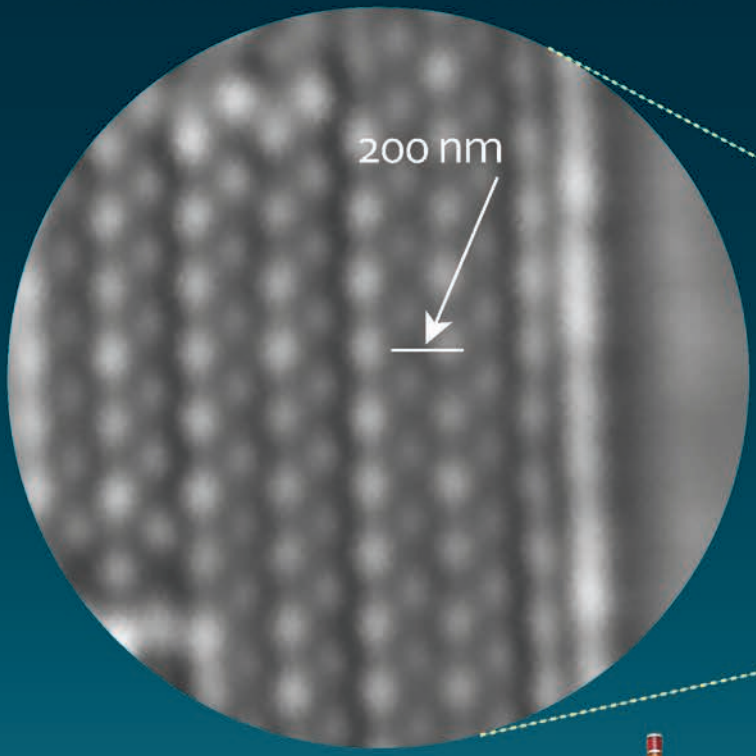

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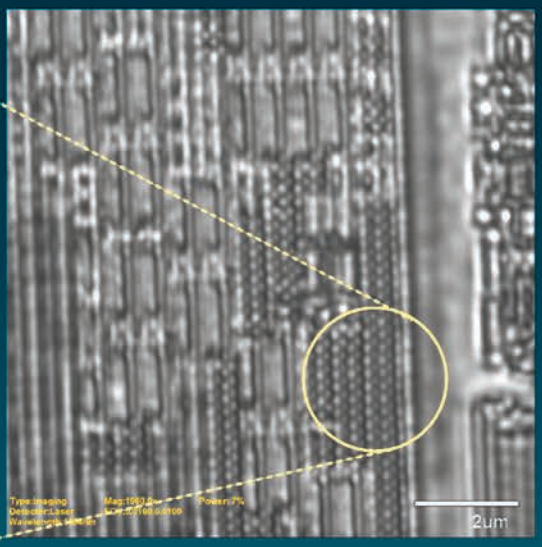

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AN EVALUATION OF CORROSION INHIBITORS FOR USE IN ACID DECAPSULATION *(continued from page 14)*

iodine concentrations of up to 0.024 mol/L are possible for 100% nitric acid.[2] The same authors indicate that it can take many days for nitric acid/iodine solution to equilibrate in concentration. This observation makes prior data, such as in Ref 3, questionable in absolute values but valid for relative values. The long time required to dissolve iodine has been observed in our work, with some solutions requiring several days for all of the iodine to go into solution. This long time frame indicates that little iodine is actually dissolved in the nitric acid during the 2 h shelf life observed in Ref 1, eliminating direct dissolution as a transport mechanism.

The oxidization of iodine to iodate by concentrated nitric acid is well known, as is the reaction of iodide with iodate in an acidic environment. This indicates iodate as the primary iodine-transport mechanism shortly after the etchant is mixed. Because the solubility of iodic acid in 98% nitric acid is very low, the iodic acid may be transported as a suspension as well as a solute.

EVALUATION OF ETCHANT COMPOSITION OVER TIME

To create a process that is not subject to solution shelf life considerations, it is necessary to understand what changes over time in the etchant described in Ref 1. This was done by mixing according to Ref 1 and evaluating the solution over time intervals for contained iodate and iodine. The iodine test does not discriminate between dissolved or suspended particles. Because iodine evaporates from iodine and tri-iodide solutions, a fresh 2.2% Lugol's solution was made up immediately before performing the tests. One milliliter of the solution was placed into a graduated cylinder, and 30 mL of 98% fuming nitric acid was added. The mixture turned yellow and was stirred manually for a few seconds. Samples were periodically taken as close to the surface as possible. When sampled, two samples were taken. One was diluted to 1 molar HNO_3, and the other was diluted and neutralized to a pH of approximately 7.5. The neutralized samples were titrated to determine iodine content. The diluted samples were evaluated for iodate. The concentration difference required the use of different solutions for the titrations. A high concentration of thiosulfate was required for the iodate samples, and a very low concentration for the iodine samples. Any undissolved iodate entrained with the sample will dissolve in the water used for dilution. This may match the characteristics of the etchant as it is pumped from the source bottle. Because the iodate precipitates and settles, less will be entrained in the etchant. The starting assay indicated that all iodine introduced is converted to iodate. The assay also indicated no detectable dissolved iodine. Over time, as the iodate precipitate settled to the bottom of the acid mix, the concentration of iodate decreased, while dissolved iodine remained undetectable. After 12 h, the acid solution was clear, and little iodate was detected. After hours, small amounts of iodine were detected. This indicates that the presence of iodate is a function of time and the settling rate of the iodic acid. Because the iodate is not soluble in fuming nitric acid, it readily precipitates out, producing the limited life observed in Ref 1. The iodine-transporting compound does not decrease in efficacy; it simply settles out.

EVALUATION OF WIRE PROTECTION FROM DISSOLVED IODINE

To determine if dissolved iodine could contribute to the preservation of silver bond wires, a test was devised that used only dissolved iodine. A volume of 70% nitric acid was placed on a stirring hot plate set at 30 °C. An excess of iodine was added, and the acid was left for approximately 36 h. The solution took a strong red-orange color. This solution was used as the inhibitor source for etching four parts with an I53 connected to an Elite Etch-Cu. (The I53, manufactured by RKD Engineering Corp., is a patent-pending syringe pump configured to introduce small quantities of a corrosion inhibitor into the acid stream of an automatic decapsulation system. The Elite Etch-Cu, model 7100, is an automatic dual-acid decapsulator manufactured by RKD Engineering Corp.) The first part was etched for 120 s with a ratio of 20:1. The etch results indicated that a longer etch time was needed. The remaining three parts were etched for 150 s with acid-to-inhibitor mix ratios of 15:1, 25:1, and 30:1. The results are shown in Fig. 1 to 3.

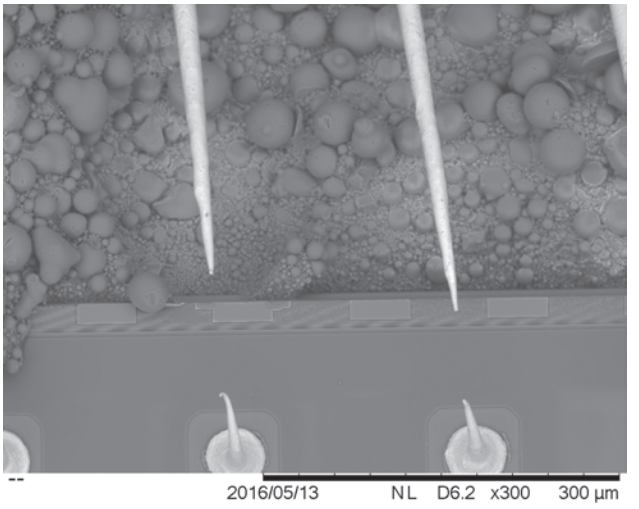

Fig. 1 150 s etch with 15:1

Over a 2-to-1 range in iodine concentration, the process changes from elimination of wires to varying degrees of wire thinning. It can be seen that iodine dissolved in 70% nitric acid provides some protection at the mix ratios tried. The measured iodine content of the solution was 0.00372 mol/L. This results in iodine concentrations of 0.00025, 0.00015, and 0.00012 mol/L at the mix ratios used above. It may be possible to obtain better wire protection with lower iodine concentration, but the reactivity with the wires as shown at higher concentrations may indicate a very limited process range and lack of stability.

EVALUATION OF WIRE PROTECTION FROM DISSOLVED IODATE

A saturated solution was made of potassium iodate in deionized water. The concentration is highly temperature dependent but was approximately 0.3 normal. This is approximately 30 times the measured iodate concentration established in the evaluation of the etchant used in Ref 1. This solution was used as the corrosion-inhibitor source for an I53 connected to an Elite Etch-Cu. The samples decapsulated were the same type as used in Ref 1, but a slightly different recipe was used, as shown in Table 1.

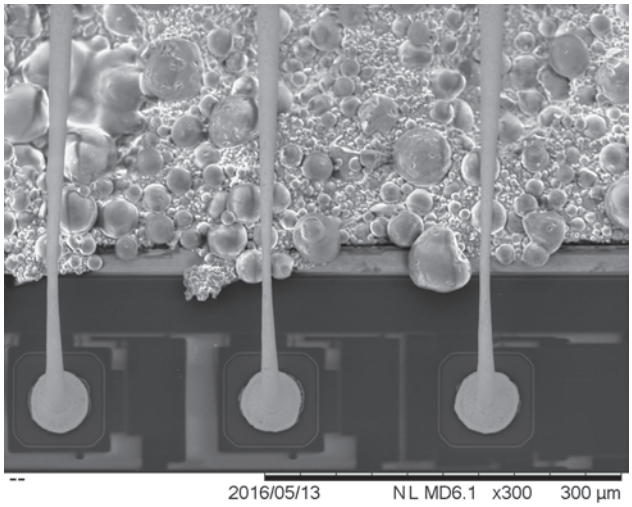

Fig. 2 **150 s etch with 25:1**

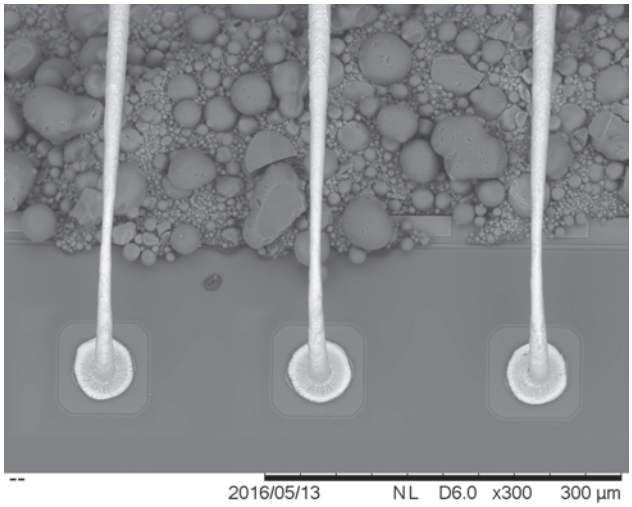

Fig. 3 **150 s etch with 30:1**

Table 1 Silver wire decapsulation recipe

Etch temperature	30 °C
Heat-up time	120 s
Etch time	120 s
Etch volume	3 mL/min
Rinse time	0 s
Etch mode	Pulsed HNO_3 + INH
Ratio	30:1 (acid:inhibitor)

As can be seen from Fig. 4, this process effectively prevents wire damage from the fuming nitric acid used for decapsulation.

Approximately 72 h later, the same solution and recipe was used to decapsulate another sample. The results shown in Fig. 5 demonstrate that the solution is stable over this time frame. The premixed etchant used in Ref 1 lost effectiveness in less than 2 h.

Due to the sensitivity of the solution concentration to temperature and its limited solubility at any temperature, solutions were investigated using iodic acid. In addition to much higher possible concentrations in water, iodic acid is somewhat soluble in dilute nitric acid, depending on the HNO_3 concentration. The addition of nitric acid to the solution reduces the amount of water introduced, minimizing metal loss and increasing the efficacy of the etchant. Two solutions were made up. The first solution

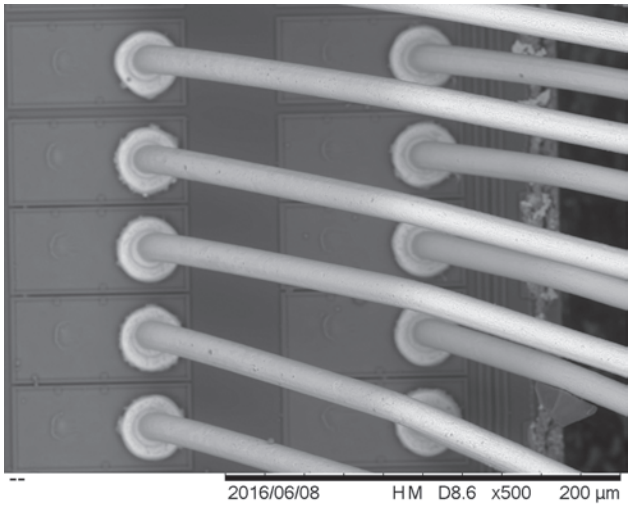

Fig. 4 **Etched with potassium iodate**

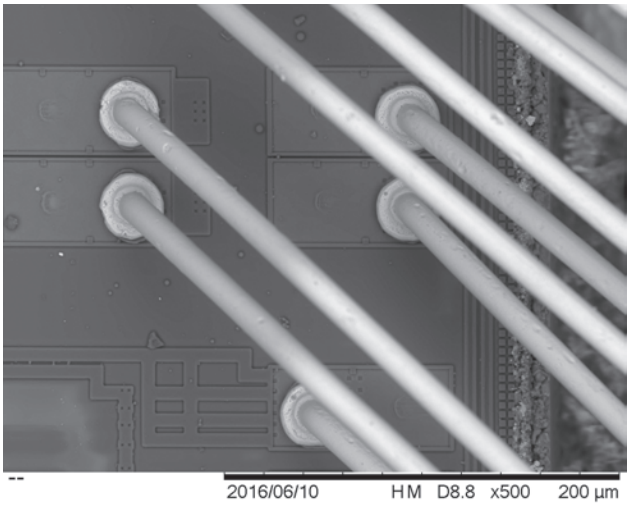

Fig. 5 Same recipe 72 h after Fig. 4

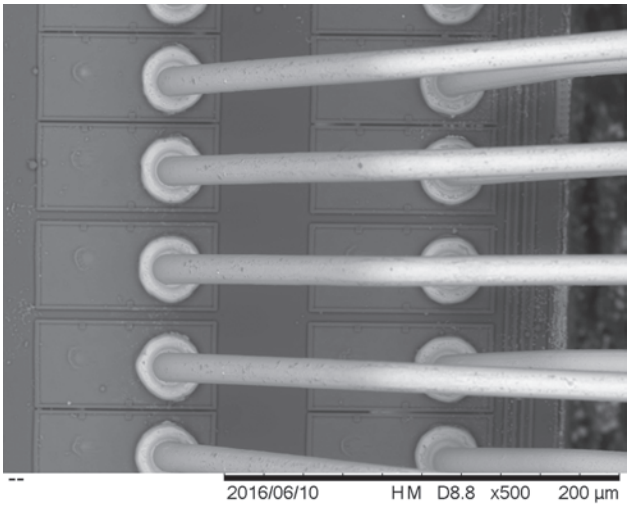

Fig. 6 20:1 iodic acid

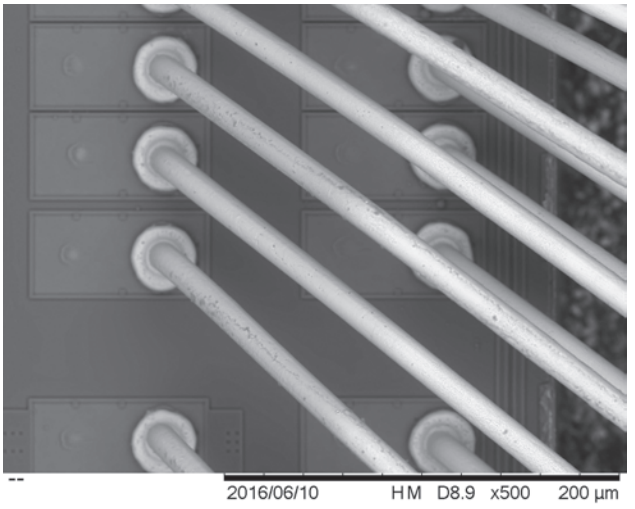

Fig. 7 30:1 iodic acid

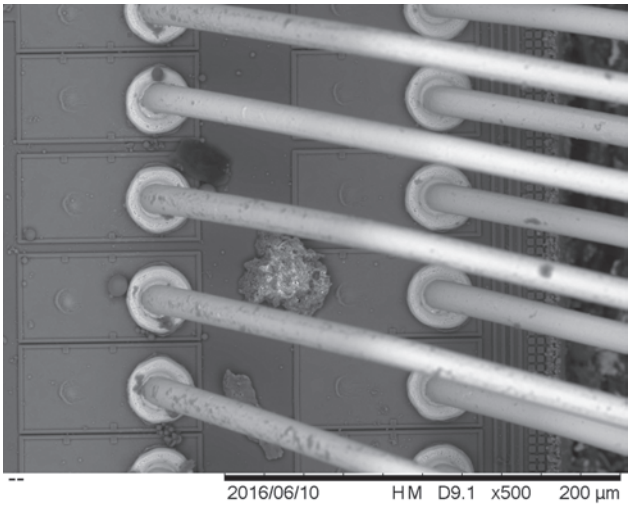

Fig. 8 40:1 iodic acid

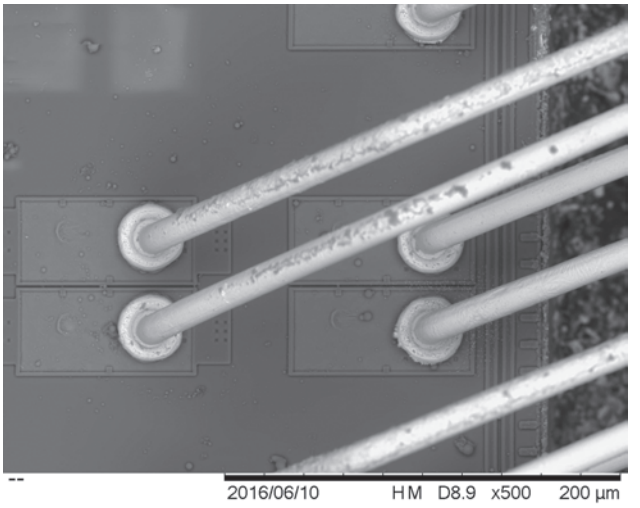

Fig. 9 20:1 iodic acid in dilute nitric acid

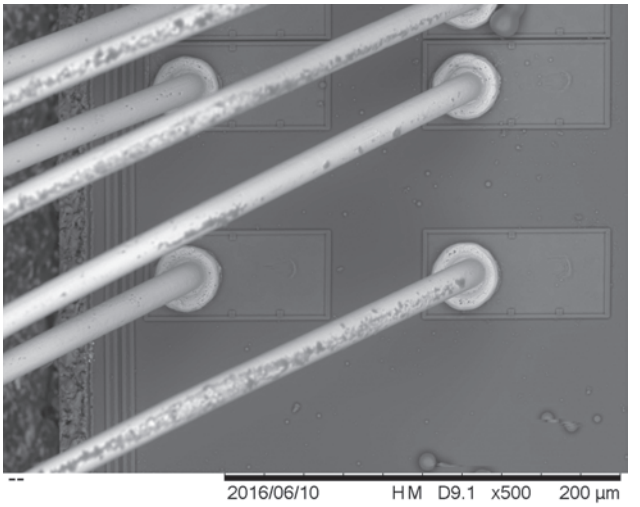

Fig. 10 30:1 iodic acid in dilute nitric acid

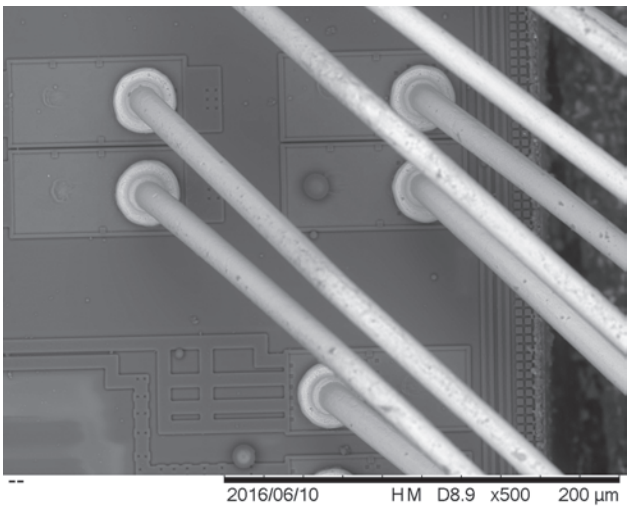

Fig. 11 **40:1 iodic acid in dilute nitric acid**

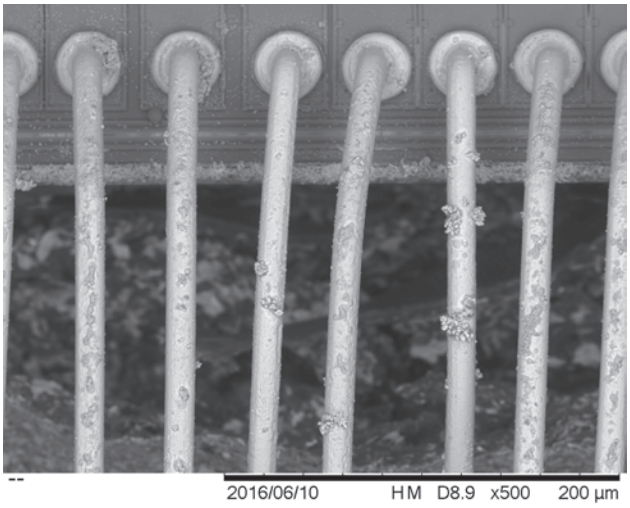

Fig. 12 **Etched using iodic acid at 50 °C**

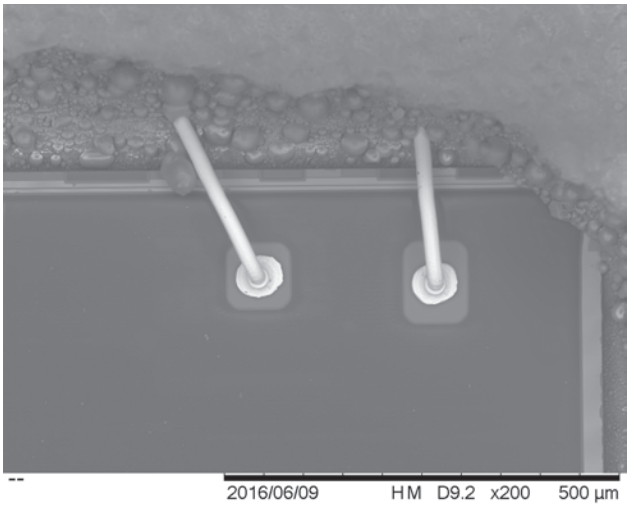

Fig. 13 **Etched using iodic acid with 360 s etch time**

was 0.3 normal HIO_3 in water. The second was 0.3 normal HIO_3 in 50% HNO_3. The etch results, at different fuming nitric acid to corrosion-inhibitor mix ratios, are shown in Fig. 6 through 11.

All electron micrograph images were taken with the Hitachi High Technologies TM-3030Plus tabletop scanning electron microscope. No sample preparation was used, to negate the possibility of any sample-preparation artifacts. As can be seen, there is no detectable difference in wire quality. Along with the increasing amount of etch debris with lower amounts of introduced water was a corresponding increase in the size of the etched cavity. As the encapsulant-removal rate increases, so does the debris load of the etchant and the greater the amount left on the wires and die surface.

DISCUSSION

The data presented in Ref 1 indicate a fairly narrow range of process parameters that produce undamaged silver bond wires. Bond pull strengths dropped with increasing etch time, higher and lower mix ratios, higher etch temperatures, and greater age of the premixed etchant.

Using a corrosion inhibitor that was directly injected into the fuming nitric acid flow path in an automatic decapsulator significantly increases the available range of process parameters. Varying the etchant-to-inhibitor ratio by a factor of 2 produced no detectable difference in wire quality. The inhibitor has a nearly infinite shelf life.

Initial evaluations of effects from increased etch times and higher etch temperatures indicate significant increases in the useful range of these parameters as well, as shown in Fig. 12 and 13.

All of the parts shown in the figures use silver alloy wire. It has been found in additional evaluations that pure silver wires require a higher-concentration inhibitor solution. An iodic acid solution at 1.0 M concentration reproduces the results shown with pure silver bond wires.

CONCLUSION

Silver bond wires can be protected from damage during acid decapsulation by the injection of a corrosion inhibitor into the acid stream. The use of a 0.3 M iodic acid solution provides protection of silver alloy wires over a wide range of process parameters, including etch time, etch temperature, and the amount of inhibitor injected. Additionally, a 1.0 M iodic acid solution will provide the same protection for pure silver wires. This solution also has a very long shelf life and is relatively safe.

Mixing corrosion inhibitors directly into the bulk acid used for decapsulation may produce similar results, but the mixture has a limited lifetime due to solubility limitations and slow reactions between the etchant and inhibitor. Bulk mixing may also precipitate materials that will damage the fluid pump inside an automatic acid decapsulator. "On the fly" mixing of the inhibitor and etchant requires a mixture lifetime of only a few seconds to be effective, and there are no particulate concerns.

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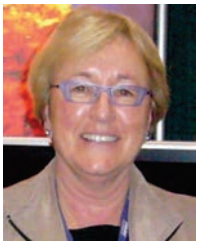
3. J.S. Carter: *J. Chem. Soc.,* 1925, *127,* pp. 2861-65.

ABOUT THE AUTHORS

Kirk Martin has 40 years of experience in designing and building specialized equipment for all aspects of the semiconductor industry, from crystal growth through final test and failure analysis. In 2005, he became a founder of RKD Engineering, which designs and builds equipment for semiconductor failure analysis and sample preparation. Kirk has patents in the fields of sample preparation, chemical vapor generation, fluid handling, and electrostatic discharge detection and mitigation. His previous positions include Vice President at Nisene Technology Group; Director of Advanced Products at Texas Materials Labs, a manufacturer of specialty semiconductor materials; and Vice President at Automated Technology, Inc., a manufacturer of front-end test and measurement systems.



Nancy Weavers has 30 years of experience in applications in the semiconductor and test equipment industries. She started at National Semiconductor in 1982. In 2006, she became the Chief Executive Officer of Left Coast Instruments, a semiconductor test equipment and electron microscope imaging sales and marketing company. She sits on the Board of Advisors for the San Joaquin Delta College Electron Microscopy Program. Previously, she was a Vice President at Nisene Technology Group.

NOTEWORTHY NEWS

MICROSCOPY & MICROANALYSIS 2017 MEETING

The Microscopy & Microanalysis (M&M) 2017 meeting will be held **Aug. 6 to 10, 2017,** in St. Louis, MO, with a theme of "Anniversaries." The Scientific Program features the latest advances in the biological, physical, and analytical sciences as well as techniques and instrumentation along with special anniversary lectures. A special symposium will celebrate 50 years of atom probe tomography. Complementing the program is one of the largest exhibitions of microscopy and microanalysis instrumentation and resources in the world. Educational opportunities include a variety of Sunday short courses, tutorials, evening vendor tutorials, pre-meeting workshops, and in-week intensive workshops. The opening reception offers an opportunity to meet new people in the field and renew old acquaintances, and the Monday morning Plenary Session features showcase talks from outstanding researchers as well as recognition of the major Society and Meeting award winners. There will be other important awards conferred during the meeting, including daily poster awards to highlight the best student posters in instrumentation and techniques as well as biological and physical applications of microscopy and microanalysis.

M&M is co-sponsored by the Microscopy Society of America and the Microanalysis Society and, for the first time, by the International Field Emission Society. For more information, visit microscopy.org/MandM/2017.

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ANADEF 2016 WORKSHOP REPORT

Alain Wislez, ANADEF Workshop President, Thales Group
alain.wislez@thalesgroup.com

The ANADEF 2016 Workshop attendees

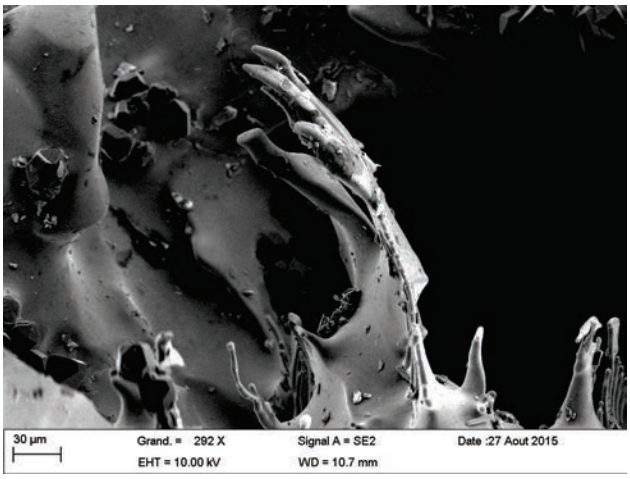
The 15th ANADEF Workshop (failure analysis and failure mechanisms of electronic components) was held June 7 to 10, 2016, at the sea resort Les Tuquets in Seignosse, France, near the famous surfing spot of Hossegor on the Atlantic Ocean. The workshop is organized by ANADEF, the French Failure Analysis Society, which meets biennially in a unique, friendly, and intergenerational spirit. Training and sharing of experiences and skills on solved and unsolved failure analysis (FA) case studies, techniques, and tools as well as trends and the future of FA are presented in a warm, friendly, and informal but professional manner that includes extended after-dinner exchanges.

As a record-setting year, the ANADEF Workshop gathered 152 people from a wide industrial and university

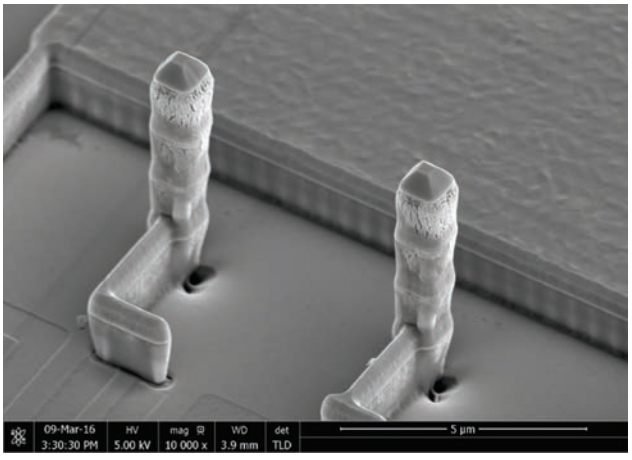
The sea resort Les Tuquets

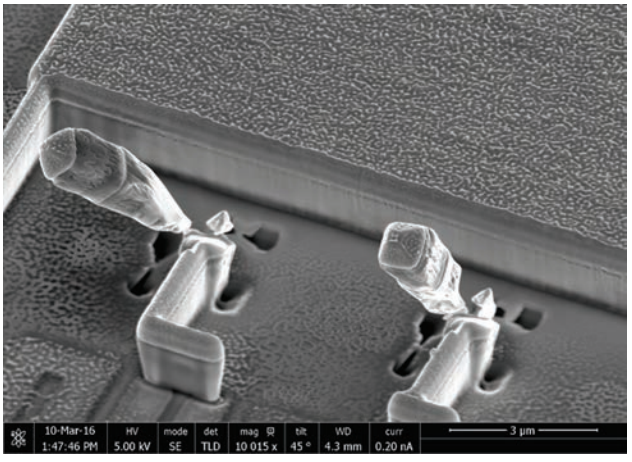
“Oasis Cristallin,” first prize in the ANADEF Photo Contest

background: IC manufacturers, energy, aeronautics, space, defense, automotive, tool and equipment suppliers, and FA lab providers. Almost 50% of the attendees were newcomers, which presented an opportunity to enlarge the ANADEF network.



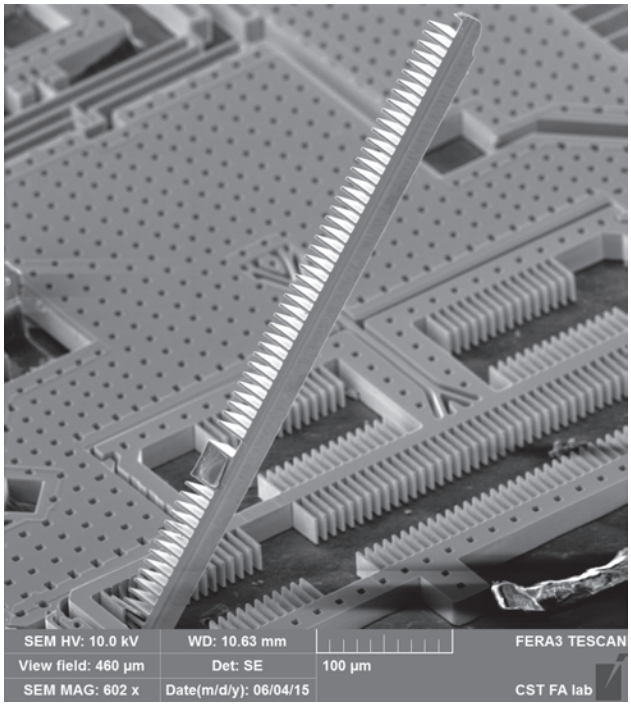
"Iron Hand," second prize in the ANADEF Photo Contest



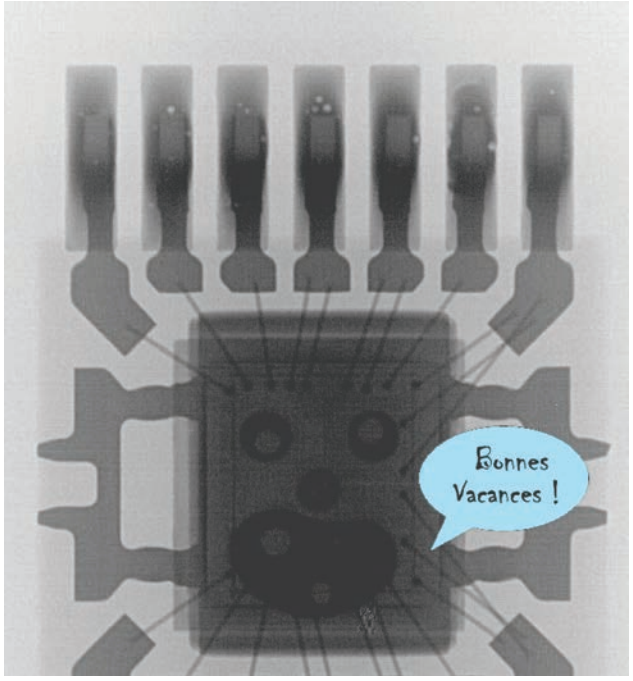


"Twin Towers 1 and 2," third prize in the ANADEF Photo Contest

Because most attendees were beginning and mid-career technical scientists involved in FA who wished to advance their careers, a professional education program was again provided for technicians, engineers, and post-graduates. The program was given by industry experts, all of whom were ANADEF members.



"Stairway to Heaven," technical prize in the ANADEF Photo Contest

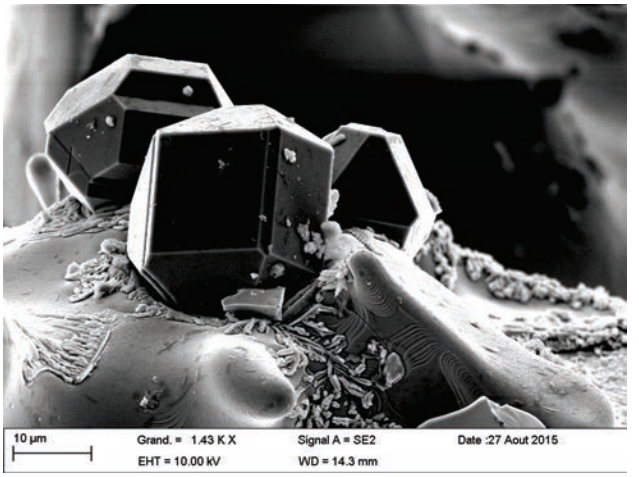


"Happy X-Rays," unusual prize in the ANADEF Photo Contest

The 2016 FA courses addressed many of the usual topics, such as packaging, power electronics components, highly integrated circuits, physical-defect-based reliability approach, printed circuit board and bonding processes, as well as many new topics, such as optical, light-emitting diodes, and laser components; thermal characterization; how to manage dynamic reliability; and helpful tools for FA.

A high-quality FA photo contest created competition among all the participants. More than 60 photos were submitted for the photo contest, with six being selected as the winners.

The sea resort Les Tuquets and its environment as well as the organization of the event widely favored exchanges between attendees at all levels, even after the days' programs. This was a unique opportunity to share FA expertise and to deepen the discussion of topics presented during the sessions as well as business, technical trends, and so on.



"Single Crystals of Silicon," aesthetics prize in the ANADEF Photo Contest

Since 1988, the ANADEF event has been held biennially. The next workshop is scheduled for 2018. For more information, visit anadef.org.

GUEST EDITORIAL

CONTINUED FROM PAGE 2

- Partner with other international conferences and organizations to co-host or share contents
- Seek opportunities with educational institutes such as universities to extend EDFAS education offers

What does EDFAS mean to you as a member? Where do you derive the most value? To grow our members, first and foremost, we need to strengthen EDFAS brand promises globally, then we need to strengthen our "product roadmap" and make it accessible to our members. Finally, we need to reform our membership structure to accommodate emerging needs, such as new-career and international electronic failure analysis professionals.

When we joined EDFAS many years ago, it was the technical content that attracted us. Today, we are still going strong! Stronger than ever, as demonstrated by many years of successful ISTFA conferences and exhibitions, with many years of effort from many individuals under the leadership of the EDFAS Board of Directors. We need to keep it going! We need to sustain our technical excellence by ensuring the premier status of ISTFA, enhancing *EDFA* magazine and *Microelectronic Failure Analysis Desk Reference* impact, and establishing an educational model beyond what we are already getting through ISTFA.

How can we do this? We need to reach out; we need to collaborate and partner with many related organizations and institutes, such as semiconductor and equipment manufacturing companies, to establish a strong electronic device failure analysis technology roadmap, co-host or share technical content with other international conferences or organizations, and seek additional educational opportunities through partnership with educational institutes such as universities. By empowering these, we can make an impact on the industry we reside in, build a knowledge pipeline benefitting our members, and, most importantly, we can grow organically as a Society.

EDFAS is built on volunteerism. The EDFAS Board fully understands we cannot achieve our strategic objectives without help from our volunteers. We would like to use this opportunity to ask each of you today to look inside yourself and find how you can best promote your profession and do a little bit of good for your professional society. We need volunteers on all EDFAS committees to keep our strategic objectives on track. We need volunteers for the local chapters. We need authors to write papers to present at the conference. There is no end to the ways you can get involved, and we challenge you to find those ways and get involved! We look forward to seeing you at ISTFA 2017 in Pasadena, California.

ASM FELLOWS 2016

EDFAS MEMBERS NAMED ASM FELLOWS

The Electronic Device Failure Analysis Society (EDFAS) is proud to announce that three of its members were named to ASM International's 2016 Class of Fellows: **Lee Knauss, Philippe Perdu,** and **David Vallett.** In 1969, ASM established the Fellow of the Society honor to provide recognition to members for their distinguished contributions to materials science and engineering and to develop a broad-based forum of technical and professional leaders to serve as advisors to the Society. This year's awards were presented at ASM's annual Awards Dinner on Tuesday, October 25, 2016, in Salt Lake City during Materials Science & Technology 2016.

Dr. Lee Knauss, FASM, Chief, Technology Transition, IARPA, Washington, D.C., was recognized "for the development and advancement of magnetic current imaging fault isolation techniques used in microelectronics failure analysis."

Dr. Philippe Perdu, FASM, Microelectronic Senior Expert, CNES, Toulouse, France, was recognized "for outstanding leadership and technical contributions toward the development of novel defect localization and failure analysis techniques applied to microelectronics and microsystems devices."

Mr. David Vallett, FASM, Owner, PeakSource Analytical LLC, Fairfax, Vt., was recognized "for sustained outstanding technical contributions, leadership, dissemination of knowledge, and education in microelectronic IC fault isolation and failure analysis technology and magnetic imaging applications, and for articulating and publicizing major analytical technology hurdles and challenges throughout the industry."

EDFAS congratulates these gentlemen on achieving the distinguished honor of ASM Fellow. They join Larry Wagner (2010), Ed Cole (2013), Bill Vanderlinde (2014), and Tom Moore (2015) as EDFAS members selected for this honor.

EDFAS Vice President Lee Knauss, FASM (left), was onsite to receive his award during MS&T16 in Salt Lake City. He was congratulated by Ed Cole, FASM (middle), and EDFAS President Zhiyong Wang (right).

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ISTFA 2016—WOW!

Martin Keim, ISTFA 2016 General Chair
Mentor Graphics Corporation
Martin_Keim@Mentor.com

EDFAS luncheon and general membership meeting

ISTFA, our yearly International Symposium for Testing and Failure Analysis, came to a close in Fort Worth, Texas, on November 10, 2016, and what a great Symposium it was! ISTFA grew on all fronts—bigger and better than in previous years. With 795 total attendees, counting the Symposium and Expo, ISTFA 2016 had more participants than ISTFA 2015 and enjoyed an 11% growth over ISTFA 2014. Also, the Expo grew in numbers, with 75 companies displaying their goods and services, including three companies that had never exhibited at ISTFA. To keep up with the demand, twelve booth spaces were added in the middle of the year; nonetheless, the Expo floor was sold out. The Technical Program grew larger, too, with a third parallel track added to the Monday afternoon schedule.

BIGGER, YES, BUT BETTER?

Growing numbers are only one indication of a good Symposium. Growing numbers show that you valued your experience in previous years, so you came back. The numbers show that ISTFA is a good place to publish your work and that companies on the Expo floor value coming to ISTFA, meeting you, establishing new contacts, and setting up or closing business deals. But how did ISTFA 2016 do on the quality of the program compared to previous years, so you will plan on attending ISTFA in 2017? Well, as General Chair I am naturally somewhat biased in saying that we did well, offering you a great, high-quality program. There is evidence to back up this statement. During ISTFA, I took every opportunity to talk with you, the attendees, about what you thought of this year's event, of ISTFA in general, and what we can do better. The feedback I received was overwhelmingly positive. For example, if one of the "biggest" negative comments I heard was that we forgot to provide a return basket for the poster voting forms, then I am confident in saying we had a very good Symposium!

As in previous years, the Organizing Committee tried to improve the Symposium and the Technical Program, in particular. Of the many changes implemented, there are three I would like to mention here, and I ask for your feedback (e-mail me at Martin_Keim@Mentor.com). The first change was the new program element of invited talks. Eight presenters were selected by the Session Chairs in cooperation with the Technical Program Chair for the purpose of kicking off a selected session and providing a framework, food for thought, an outlook, or similar context. How did you like these invited talks? Did they add value?

General Chair Martin Keim and the ISTFA 2016 Organizing Committee

The second change was increasing the number of paper presentations by adding a third parallel track on Monday afternoon. To be honest, we did not plan for this but were overwhelmed by the huge influx of high-quality paper submissions. Thank you! Many more papers made the cut of the predefined threshold of acceptance. We had the option of either cutting very good contributions and keeping the traditional two-track outline, or accepting papers based on their merits and expanding the program by adding a third track. We chose the latter.

The third change was a more thorough incorporation of the ISTFA theme. This year our theme was "The Next Generation," and it was featured in the excellent keynote presentation, "How to Educate the Next Generation IC Debug/FA Engineer at Academia," by Prof. Christian Boit and Dr. Philipp Scholz from the Technische Universität Berlin. Not only did the keynote speech show that it is quite possible for academia to educate students who are

(continued on page 30)

Local Student Poster Session participants from the University of Texas at Arlington with their advisor, Prof. Dereje Agonafer, and Dr. Felix Beaudoin, ISTFA 2016 Attendee Chair

ISTFA SPONSORS

On behalf of the Electronic Device Failure Analysis Society (EDFAS) and the organizers of ISTFA 2016, we appreciate your generous sponsorship contribution and recognize your continued commitment in making the ISTFA Conference and Exposition an outstanding event!

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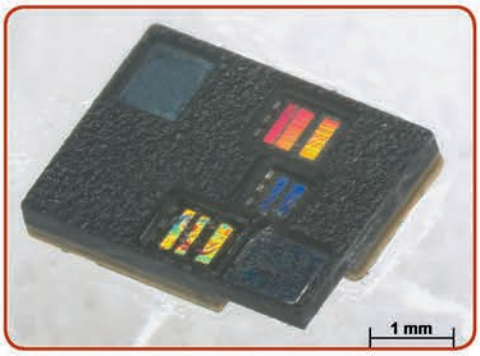
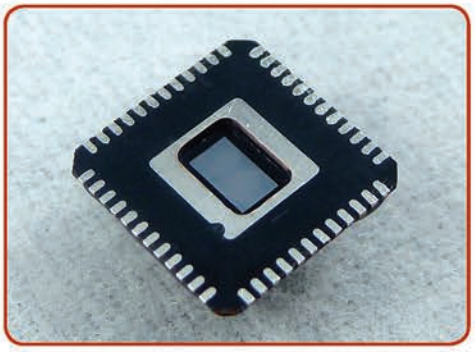
Small Device Preparation





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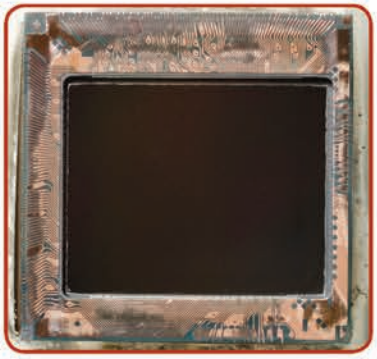

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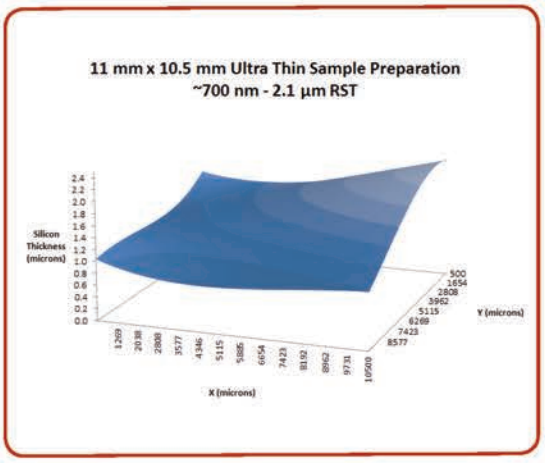

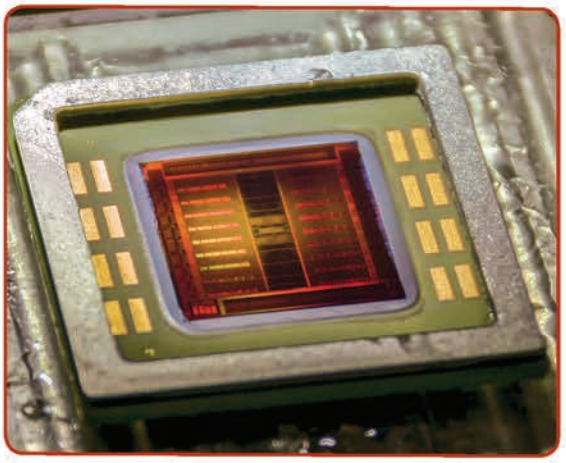

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ISTFA 2016–WOW! *(continued from page 27)*

ready for their FA job, but it also provided a recipe for other universities on how to set up such a program. Next, the theme was at the center of the Panel Discussion, which quickly turned into a very interactive discussion among the audience and panelists. It was a pleasure to observe the passion, drive, and engagement of every participant. You will find a summary of the Panel Discussion on page 33 in this issue. Finally, the Student Poster Session featured ten contributions from two local universities: the University of Texas at Arlington with nine posters, and Rice University with one poster. I observed great interactions between the presenting students and the attendees, who were interested to learn about the students' research, which, by the way, is outstanding.

Other constants of the program returned to ISTFA 2016: two short courses were held on the Saturday before ISTFA; twenty tutorials were offered, including two new ones; four User Groups were held; and a sold-out Tools of the Trade Tour featured eleven companies.

DONE BY VOLUNTEERS

Of course, creating such a program involves hard work by many people, nearly all of whom are volunteers. These volunteers spend tremendous hours of their free time in various roles, all toward the goal of creating an outstanding Symposium. I cannot thank them enough for their hard work, but I can recognize them here: Vice General Chair Sam Subramanian (NXP Semiconductors), Past General Chair James Demarest (IBM), Technical Program Chair Efrat Moyal (LatticeGear), Attendee Chair Felix Beaudoin (Globalfoundries), Audio/Visual Chairs David Grosjean (Butterfly Network) and Zhigang Song (Globalfoundries), Expo Chair Becki Watt (Mentor Graphics), Tutorial and Short Course Chairs Susan Li (Cypress Semiconductor) and Mayue Xie (Intel), Panel Chairs Frank Altmann (Fraunhofer CAM) and Kendall Scott Wills (KAB Global Enterprises), User Groups Chairs Rick Livengood (Intel) and Baohua Niu (TSMC), Local Arrangements Chair Becky Holdford (retired), and the Video Contest Chair Rose Ring (Qorvo). In addition to these Organizing Committee Chairs, there were 38 Tutorial and Paper Session Chairs as well as approximately 100 reviewers—all volunteers. The Organizing Committee was professionally supported by Kathy Murray, Lindy Good, and Christina Sandoval of ASM International and sponsored by EDFAS through its presidents Cheryl Hartfield and Zhiyong Wang.

The ISTFA Organizing Committee is always looking for new volunteers. If you would like to participate in organizing ISTFA or become a reviewer, please contact one of the ISTFA 2017 Organizing Committee members. You will find their contact information on the ISTFA 2017 webpage at istfa.org. If you have a suggestion for new tutorials or would like to create one, please go to the ISTFA 2017 webpage and submit your ideas.

NOT ALL WORK

ISTFA's Technical Program is taxing—a full program from early morning to early evening—so relaxing and mingling at the Social Event is a welcome break. This year's Social Event was held at Billy Bob's Texas, where we enjoyed good Texas BBQ, drinks, live music, and more. The highlight was a bull-riding event, where professional cowboys tried to stay atop a violently bucking bull for eight seconds. Great fun! Oh yes, someone must have told the band that the General Chair likes line dancing.

COME BACK FOR ISTFA 2017

In closing, ISTFA 2016 was a great success: an excellent Technical Program, a larger number of high-quality papers, and a growing number of attendees as well as companies displaying on the Expo floor. I invite you to come back for ISTFA 2017, which will be held November 5 to 9 in Pasadena, California.

EDFAS MEMBERSHIP

Whether networking at events or accessing information through *EDFA*, ISTFA proceedings, or journals, our members have the edge. Now it's time to introduce EDFAS to others in the industry who would like to take advantage of these career-enhancing benefits. Help us help the industry by expanding our membership and offering others the same exceptional access to information and networking that sets EDFAS apart. To reacquaint yourself with and introduce others to the EDFAS member benefits, visit asminternational.org/web/edfas/membership.

ISTFA2017

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"VLP... Demonstrating 110 nm Resolution in Common Laser Probing Applications"

Travis Eiles, Intel Corp.

ISTFA 2016 OUTSTANDING PAPER:

"Root Cause Analysis for Pin Leakage"

Zhigang Song, Globalfoundries

ISTFA 2016 BEST POSTER:

"Validation of DLS Data by LVP in Case of Marginal Failure"

Keonil Kim, Samsung Electronics System LSI Division

ISTFA 2016 STUDENT POSTER:

"Solder Ball Reliability Assessment of WLCSP through Power Cycling"

Bhavna Conjeevaram, University of Texas at Arlington

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2nd Eric Cattey, NXP Semiconductors

3rd Richard Park, Raytheon

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1st Nathan Wang, Maxim Integrated

2nd Lori Sarnecki, Fairchild Semiconductor

3rd Philipp Scholz and Heiko Lohrke, Technische Universität Berlin

Category III: False Color Images

1st Wentao Qin, ON Semiconductor

2nd Luigi L. Aranda, Raytheon

3rd Andrew Ozaeta, Raytheon

All winners received a recognition plaque or certificate and a one-year EDFAS membership. The winning entries will be featured on the cover of this magazine during 2017. They also may be viewed on the EDFAS website.

EDFAS 2016 VIDEO CONTEST WINNER

Congratulations to the following winner:

"ACETONEMENT aka: Where Did the Bond Wires Go?" by Timothy Hazeldine, ULTRA TEC

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A SUMMARY OF THE ISTFA 2016 PANEL DISCUSSION: NEXT GENERATION OF FA ENGINEER

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A failure analysis (FA) engineer's core business is to investigate and solve reliability problems of technologies for electronic applications by identifying process variations and root causes of defects and by suggesting corrective actions. An FA engineer must handle multiple FA techniques for defect localization, preparation, and physical analysis with continuously increasing complexity. In parallel, he needs sophisticated skills in communication because he often acts as an intermediary between different parties (fab, design, test, customer, etc.). Under these aspects, the ISTFA 2016 Panel Discussion was dedicated to the following topics:

- How is a typical FA lab organized? Which skills and levels of education are required for a future FA engineer?
- How does one go from being a specialist in a certain preparation or analysis method to being an experienced FA engineer ready for customer meetings?
- Which internal/external training programs are available (face-to-face or online)?
- Where does the money and time come from that is spent to become trained in FA?

The panel members were Professor Christian Boit, Technische Universität Berlin; James Cargo, Broadcom Ltd.; and Nebojša Janković, NXP Semiconductors. Each panel member has a long history of experience in FA work, education, training, and lab management.

The Panel Discussion was introduced by Nebojša Janković. He pointed out that a typical FA lab is organized by FA engineers as job owners being responsible for performing hands-on electrical FA and physical characterization, with the emphasis on software- and hardware-based device fault localization. Only highly specialized investigations are done by dedicated engineers. Standardized physical analysis steps are mostly done by a technician crew. Strong preference should be given to mixed-signal IC design, test, and layout understanding.

"AN FA ENGINEER SHOULD BE EDUCATED TO THE ACADEMIC LEVEL OF A MASTER'S OR Ph.D. DEGREE IN TECHNICAL SCIENCES AND THEN MUST SEEK CONTINUOUS LEARNING AND TRAINING."

Furthermore, an FA engineer should have experience with memory devices, especially nonvolatile options, as well as reverse engineering skills, including IC process technology knowledge. Responsibilities should include not only the use of existing and available equipment, techniques, and methods but also the development of new methods and techniques. An FA engineer should be able to work independently but also to cooperate with peer product, test, design, and process engineers as well as customers. In addition to technical skills, he must also be a good team player. An FA engineer should be educated to the academic level of a Master's or Ph.D. degree in technical sciences and then must seek continuous learning and training. With the experience and routine from internal customer meetings, he also strengthens the communication skills necessary to take care of end-customers' needs. This can be managed by additional coaching and mentoring on the job, focused on having an outside view and an end-customer's perspective. A typical beginner learns the first skills and tools internally on the job, being mentored and trained by an experienced FA engineer. External courses must follow for certain specialized methods and tools.

After the introduction, an intense open discussion began between the panelists and the audience. It was discussed that FA spans a large breadth of topics and educational disciplines, and almost no undergraduate programs are available at universities. Linking to

the keynote presentation, "How to Educate the Next Generation IC Debug/FA Engineer at Academia," Christian Boit mentioned that the educational concept begins with standard lectures on electronic circuitry, IC design, and semiconductor devices, followed by design verification and debug/FA. This educational concept is mature, proven, and ready to be integrated into electrical engineering curricula worldwide. Furthermore, he pointed out that an FA engineer has an exciting job and is in good hands within a great FA community. He said, "Being an FA engineer is like entering 'Hotel California': You can check in but cannot check out," meaning that one stays in touch with this topic over the long term, because the knowledge to make a quality FA engineer grows over many years.

James Cargo pointed out that FA labs must deal with a wide range of issues over the course of a year; as such, they must be staffed appropriately to handle the variation of work and the ever-shifting workload. The FA lab manager must allocate and balance the workload such that some time is set aside for training, which requires a long-term plan. An FA lab manager should continuously monitor the team's work and promote and encourage each FA engineer, considering his personal skills and personality.

One attendee also commented that spending money for continuous training and networking at conferences is important, while another mentioned that soft skills for communication and capacity for teamwork should be promoted.

The end of the session brought an in-depth discussion with a broad variety of perspectives and multiple contributions from FA engineers, lab managers, industrial customers, and members from academia. All reached the same conclusion: An FA engineer requires a high level of technical knowledge as well as high flexibility and communication skills.

EDFAS AWARDS

SEEKING NOMINATIONS FOR NEW EDFAS AWARDS

EDFAS is pleased to announce two new awards to recognize the accomplishments of its members. The awards will be given annually, with the inaugural EDFAS Lifetime Achievement Award and the EDFAS President's Award being presented at ISTFA 2017. Nominate a worthy colleague today!

EDFAS LIFETIME ACHIEVEMENT AWARD

The EDFAS Lifetime Achievement Award was established by the EDFAS Board of Directors in 2015 to recognize leaders in the EDFAS community who have devoted their time, knowledge, and abilities to the advancement of the electronic device failure analysis industry.

EDFAS PRESIDENT'S AWARD

The EDFAS President's Award shall recognize exceptional service to EDFAS and the electronic device failure analysis community. Examples of such service include but are not limited to committee service, service on the Board of Directors, organization of conferences or symposia, development of education courses, and student and general public outreach. While any member of EDFAS is expected to further the Society's goals through service, this award shall recognize those who provided an exceptional amount of effort in their service to the Society.

Nomination deadline for both awards is **March 1, 2017**. For rules and nomination forms, visit the EDFAS website at edfas.org and click on Membership & Networking and then Society Awards, or contact Joanne Miller at 440.338.5151, ext. 5513, joanne.miller@asminternational.org.

To learn more, visit asminternational.org/web/edfas/societyawards.

ISTFA '16 USER GROUP SUMMARIES

ISTFA 2016 SAMPLE-PREP/ 3-D PACKAGE-PREP USER GROUP

Moderators: Nathan Bakken, Intel Corporation, and Roger Stierman, RJ Stierman Consulting
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The Sample-Prep User Group hosted four technical presentations toward the development of new capabilities in the laboratory. The first presentation discussed scaling up focused ion beam (FIB) techniques to enable processes that would typically involve incompatible materials systems or excessive processing time. The next two presentations addressed methods to scale down existing mechanical and optical deprocessing techniques to meet new tolerance requirements. The final presentation described some fundamental changes in the backside silicon thermal models used to describe systems with remaining silicon thickness (RST) approaching zero. The session was concluded by an interactive discussion where the audience engaged with the panel of User Group authors. More than 85 people attended the Sample Prep/3-D User Group meeting, which was sponsored by Varioscale, Inc.

"Novel Sample Preparation Techniques for Semiconductor Process Technology Development and Advanced Packaging Analysis Using Plasma FIB" was presented by Surendra Madala of Thermo Fisher Scientific (FEI group). The presentation noted the issues with conventional FIB processing: extremely long time and excess heat generation for large areas and volumes, and depth of disturbed layers versus the shrinking features' sizes. Plasma FIB examples showing less damage and feature retention in reasonable times were shown for applications with dimensions up to many hundreds of microns.

"Using Microline Indentation to Precisely Downsize <100-µm-Thin Die out of the Package" was presented by Janet Teshima of LatticeGear. The difficulty of reaching a thin die's failure site was noted, especially die extracted from a package. The use of sacrificial silicon pieces, along with a microspot mechanical cleaving fixture, was shown to produce results with high yields. It was reinforced during the discussion session that the simple technique achieved high success rates. It was also noted that alignment accuracy depended on the alignment optics and could potentially continue to be scaled with the right microscope and/or reduction of the 10 µm diamond cleaving apex.

"Pulsed Laser Preparation of Uniform, Submicrometer Remaining Silicon over Active Circuits" was presented by Scott Silverman of Varioscale, Inc. A strategy to overcome the current uniform material-removal rate in a defined machining area by selectively blanking laser pulses was shown to enable contoured laser-assisted chemical-etched (LACE) surfaces. The ability to shape the etched surface was proposed to enable improved trench tolerances in addition to other capabilities. During the panel discussions, the minimum RST achievable by LACE as limited by circuit invasiveness in addition to machining accuracy was discussed. The author presented some theory to support paths to tens-of-nanometer RST with circuit invasiveness limited by careful control of the melt depth and average incident laser power, including preliminary results for ultraviolet 355 nm pulsed-laser sources.

"Submicron Prep Impact on Silicon Lateral Heat Dissipation, Junction Temperature, and FinFET Validation Thermal Management" was presented by Vladimir Vlasyuk of Intel. This presentation considered the heat diffusion from optical probing on devices thinned to sub-3-µm silicon. Air cooling was considered suboptimal; a liquid cooling solution provided better results. During the discussion session, the audience noted quite fervently that challenges facing sample prep are rapidly shifting from surface quality and machining acuity toward overcoming thermal and mechanical barriers. The author proposed that additional work will be required for thermal management of very thin silicon device preparation.

The session was closed several minutes after the scheduled conclusion, with conversations continuing

into the halls. The cross-company interaction successfully enabled networking as well as intriguing debate on future sample-prep challenges, including stricter required tolerances, handling of smaller and more complex form factors, and growth of techniques requiring very thin RST.

ISTFA 2016 NANOPROBING USER GROUP

Moderators: Nicholas Antoniou, Revera, Inc., and Baohua Niu, TSMC
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The Nanoprobing User Group, with nearly 100 people in attendance, had a very packed schedule that included five exceptional speakers covering a wide range of interesting topics. The session was sponsored by FEI/Thermo Fisher Scientific.

Dr. Sung Park started the discussion with an interesting new technology presentation: infrared photo-induced force microscopy (IR PiFM). This is an atomic force microscopy (AFM)-based platform that, coupled with a wideband-tunable mid-IR laser, can "fingerprint" chemical species near the AFM resolution limit. PiFM can acquire both the topography and spectra images concurrently. Dr. Park showed the breadth of the capabilities of the PiFM with data on various polymer systems, such as polymer-polymer blends, polymer interfaces, bio-polymers, and block copolymers. By enabling imaging at the nanometer scale with chemical specificity, PiFM provides a powerful new analytical method for deepening our understanding of nanomaterials and facilitating technological applications of such materials.

Dr. Frank Altmann of Fraunhofer IMWS spoke about the application of nanoprobing and scanning electron microscopy (SEM)-based current imaging for failure analysis applications in semiconductor microelectronics. Two electron-beam-based probing techniques were discussed in great detail, highlighting the capabilities of each method. One is electron beam induced current (EBIC), and the other is electron beam absorbed current (EBAC). For both methods, the primary electron beam of the SEM acts as a local current source that generates a resulting current density within the IC structure. The introduced or absorbed current is acquired by a probe needle placed at a certain IC position that is initially identified in the SEM image, subsequently amplified, and finally synchronized with the SEM image. EBIC is commonly used to investigate *pn* junctions of diodes to obtain information about the position and size of the depletion zone and to verify dopant process parameters. EBAC, on the other hand, allows the localization of opens and shorts within the metal network. Furthermore, a recently developed approach allows the localization of thin oxide shorts or weaknesses by EBAC as well. Both techniques are capable of electrical characterization of a single transistor and defect localization. Dr. Altmann then detailed some of the sample-prep techniques: delayering, cross sectioning, and focused ion beam (FIB) circuit cut/edit, which are critical to the success of EBIC and EBAC analysis of ICs.

Mr. Bob Newton of Thermo Fisher Scientific talked about electron beam induced resistance change (EBIRCH) best practices and best-known methods (BKMs), based on his years of experience in the field. He covered key features of the EBIRCH system and current BKMs for defect localization. He described how to set voltage bias and beam conditions, given a possible defect depth, and also introduced a novel workflow to ensure optimum defect localization while keeping device integrity intact. The introduced workflow is general in that it can be used on many types of semiconductor devices and shows a high success rate on each type.

Dr. Tomáš Hrnčíř of Tescan, Czech Republic, presented xenon plasma FIB delayering and nanoprobing on an Intel 14 nm sample. Using a commercially available Intel 14 nm microprocessor unit sample that features the latest ultra-low-k dielectric materials and physically very thin layers, Dr. Hrnčíř discussed the advantage of xenon plasma FIB delayering as a key enabling technique to prepare a well-characterized sample surface for much-needed nanoprobing of each critical layer. Dr. Hrnčíř presented a configuration of a xenon plasma FIB with specialized gas-injection system chemistries and an SEM with high resolution at very low beam energy (≤500 eV to minimize beam damage to sensitive devices) as the platform for preparing samples for nanoprobing. Freshly delayered surfaces can be used immediately for nanoprobing by utilizing the Kleindiek Probe Shuttle installed inside the xenon plasma FIB-SEM chamber. This approach allows nanoprobing on perfectly clean and flat surfaces. He showed atomic force microscopy measurement data that

confirmed the flatness of the surface and its suitability for nanoprobing because of slightly raised metal/via and transistor contacts over the insulator/dielectric layers.

Mr. Christian Catalan of Rasterly Lab was the last speaker. He discussed the importance of and the challenges facing failure analysis and probing engineers in data management and analysis for nanoprobing. He shared his thoughts on what makes an effective workflow as well as useful data summary charts. He demonstrated an advanced data analysis platform that addresses many of the aforementioned issues. It is a web-based application that caters to collaborative teams, reduces the dependency on scripting solutions such as Excel, and introduces advanced capabilities such as saved sessions, searchable analyses, and effortless collaboration with colleagues. In the broader scope, this is a call for standards in data analysis, so that workflow can be universal and highly accessible to nanoprobing users.

ISTFA 2016 CONTACTLESS FAULT ISOLATION USER GROUP

Moderators: Patrick Pardy and Dan Bockelman, Intel Corporation
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Over the past few years, the Contactless Fault Isolation User Group has looked for innovations and research on how to move the capabilities forward for future process geometrical scaling. Some presentations were given in topic areas such as higher-numerical-aperture lenses, shorter wavelength usage, and so on. Although these developments will be very important moving forward, we continue to use a very large industry-installed base of current technologies to perform failure analysis and debug of our products. This large number of tools represents a huge capital outlay for many companies, so the use of them for an extended period of time continues to be imperative. Therefore, this year's focus for the Contactless Fault Isolation User Group centered on both innovation and efficiency for the existing industry standard infrared-based optical probe toolset. We want to "wring" every cent of value that we can from these tools until the next inflection point is reached due to fab process and where the future of the industry leads.

Dr. Krishna Kuchibhotla of Checkpoint Technologies gave the presentation "Unique Dual-Beam Interferometer for Probing ICs." This new IC-probing technology showcases a dual adjustable laser beam using phase-shift interferometry. The new hardware splits the incident beam into probe and reference beams, which can be moved independently of each other. A phase shift interferometer splits the beam into two separate beams, with a phase difference that can be adjusted between 0 and 2 π. Precision phase control allows the operator to obtain a good fringe contrast, which provides improved signal detection. The operator can use the probe beam for probing and park the reference beam anywhere within the permissible piezo field of view. The hardware also provides shutter capabilities to shut off one of the beams. The tool name is SOM-DBI, for laser scanning optical microscope with integrated dual-beam interferometer. An upgrade option for the DBI is available for existing tools. The new capability uses the same software but adds a new graphical user interface window with a second beam (green color) that can be moved around independently from the existing beam (red color). Either unseparated or separated dual-beam modes can be used, but the separated mode offers an improved signal. An example was shown that illustrated how using unseparated versus single mode gave a +3 db signal improvement. Another example showed that for a small node, the aligned dual-beam configuration provided +1.7 db improvement when compared to using a single-beam configuration only. In summary, this is a unique method of DBI with adjustable *x*, *y*, and *z* flexibility for the two beams.

Mr. Neel Leslie of FEI/Thermo Fisher Scientific Company gave the second presentation, "Advanced CW Laser Voltage Probe Technique: Imaging Non-Periodic Signals." A new technique, known as laser voltage tracing (LVT), was presented. This technique adds a gated integrator to get past any limitations of the spectrum analyzer. The test loop frequency and number of averages determine the hardware bandwidth. Subtraction is done between the gate and gated signal, and the result is digitized by the laser scanning microscope. When anomalies occur, the

screen is painted with black-and-white pixels to highlight potential circuit issues and their physical location in the field of view. An example was shown where normal laser voltage imaging could not be used due to the low duty cycle. Instead, the LVT technique was used to visually signal anomalies. Further root-cause analysis required tracing the circuit with normal laser voltage probing (LVP). The minimum gate time is 500 ps, but it is dependent on the type of signal being probed. The hardware upgrade adds a new box to the system but does not require a new rack. The highest bandwidth for the current LVT system is 450 MHz.

The next presentation, given by Dr. Ramya Yeluri of Intel Corp., was entitled "Use of Second Harmonic and Thermal Effects of Laser Voltage Probing." Dr. Yeluri presented the background for LVP, stating how an incident beam, through the backside of silicon, is modulated and realized in the reflected beam. This change is produced by the difference in reflectivity with respect to time. Free-carrier density change is the dominant effect, while electroabsorption at the active junction is a secondary effect. It is not possible to separate the effect of gate and drain spatially on current technologies, due to the small, compact geometries relative to the laser spot size. All periodic signals can be expressed as a sum of sine and cosine functions. Perfect square waves have odd harmonics only, so second harmonics can detect deviations (such as a missing bit, bad duty cycle, or bad slew rate). The first case study included a distorted duty-cycle clock. Typically, the duty cycle would need to be measured by probing at each location along a suspected path, but the use of frequency mapping at the second harmonic enabled detection of duty-cycle distortion without requiring probing for each node separately. The second case study demonstrated how thermal effects can be detected with LVP. For this case, there was an ohmic short to V_{SS}, which caused contention on the output pMOS of an inverter. While probing the inverter, the observed amplitude was much higher, due to the thermal effect. These techniques can be used with the existing infrared tools and provide for efficiency improvements in debug cases.

All three presentations were well received, with many follow-up discussions and questions and answers. Each of the presentations was tied to either innovations or efficient use of the existing optical probe tools in today's IC semiconductor industrial complex. The content showed that innovations by both original equipment manufacturers and the customer were still very robust and that future potential ones exist. Approximately 55 personnel attended the Contactless Fault Isolation User Group meeting, which was sponsored by Checkpoint Technologies.

ISTFA 2016 FIB USER GROUP

Moderators: Steven Herschbein, Globalfoundries, and Michael Wong, Intel Corp.
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Focused ion beam (FIB)-driven sample-preparation techniques, failure analysis methods, chip circuit modification/editing, and improved tools continue to be popular topics at ISTFA. This year, the FIB User Group was held Thursday afternoon, at the very end of the conference. Despite the late time, the gathering was well attended, with a peak attendance of approximately 60 people. Many familiar faces from the failure analysis, design debug, and materials community along with tool vendors joined us for light refreshments and stimulating discussion. Six presentations covered a wide range of topics, including a survey of conventional as well as novel conductive polymer coatings used in capping and charge control; two papers covering the advances and mechanics of slicing, harvesting, and imaging scanning/transmission electron microscope (S/TEM) lamellae; the feasibility of producing an FIB-SEM cluster tool for advanced analytics; and a circuit edit example that used capacitance rather than resistance for controlled delay. The organizers also wish to thank Thermo Fisher Scientific for its sponsorship.

The session's first speaker was Bryan Tracy of EAG Laboratories, who presented "Capping and Coatings for FIB XTEM." Bryan's background is in SEM and TEM, and success in these endeavors is highly dependent on selection of the right protective coating for the application, to deal with charge control and milling artifacts. He listed multiple key requirements for a good cap, which included the avoidance of nano-waterfall streaks, protecting the surface from e-beam and ion beam damage, understanding specific cap chemical avoidance when

prepping for analytics, optimizing *Z* contrast, thickness and step-coverage constraints, and accidental cross-contamination in a dirty prep tool or from a tool internal component that contradicts one's conclusions. He also mentioned general things to avoid when possible, such as high viscous or mechanical forces that could deform the sample, solvents that may interact with materials in the sample, high-temperature application or cures, and so on. He listed more than a dozen commonly used coatings (Sharpie pen, polysilicon, SiN, epoxy, eBeam C, eBeam and iBeam Pt, a list of sputtered metals, silicides, and sputtered carbon) along with some of his favorite lab tooling for applying those materials, as well as pictures of a few coated structures in cross section. In the end, he professed an overall preference for sputtered carbon because of its fine grain, purity, control of thickness and coverage, optical transparency, and low impact on the sample.

Valery Ray of PBS&T, MEO Engineering Co. followed up on some of Bryan's comments about the need to coat samples that will be subject to charged particles or electron beams. The approach in his presentation, "Old FIB Tricks with New Conductive Polymers," was to forgo expensive lab high-vacuum systems and instead employ low-cost spray-on or spin-on liquid-based materials.

Valery began with an overview of the 100-year history of conductive polymers and how discovery and innovation in materials has helped fuel flat-panel and battery technology. Polymers and surfactants have found wide acceptance in electron beam lithography, where their conductive properties can help prevent charge buildup on insulating substrates that would otherwise result in beam deflection and pattern distortion. Commercially available formulations, such as ESpacer 300 and aquaSAVE, were discussed and how relatively easy they are to spin apply and remove, along with their electrical properties. Perhaps the highlight of his talk was the details of his home-built spin coater for material application, using such "high-tech" items as a bench vise, a Dremel rotary tool holding an SEM stud, and a plastic 100 DVD holder as an overspray containment device!

Valery showed several examples of SEM, FIB, and TEM images produced with materials coated with conductive surfactants. The SEM images were quite good as a result of the improved surface-charge control. Of course, minimizing total thickness is important, particularly with FIB imaging. In some cases, FIB images were reduced to only minimal topology contrast when thick applied layers resulted in a totally planarized surface. The TEM images were particularly interesting, where typical e-beam-deposited materials were separated from the surface by a thin layer of polymer prior to the FIB lamella preparation.

The next two presentations dealt with advanced TEM preparation methods. Stephan Kleindiek of Kleindiek Nanotechnik presented "A Novel Software Approach to TEM Sample Lift-Out Using the Lift-Out Shuttle." Richard Young of FEI/Thermo Fisher Scientific presented "TEM Prep Goes Forth—Ready for Seven."

Stephan showed his latest load-lock-compatible shuttle with smart control software. The system replaces the conventional TEM lift-out technique that requires the "welding" of a manipulator needle to the top of a sample and then cutting it loose once the sample is attached to the lamella holder. Instead, this system employs a mechanical microgripper (tweezer-like assembly) that can grab a sample and let it go at will. Offering simplicity and mouse-click convenience, a single screen interface controls aspects of the shuttle stage, SEM/FIB column, and gripper.

Richard's presentation echoed some of Stephan's theme of lift-out automation, but he took it further by looking at the requirements of the entire sample-prep process. High-volume process monitor jobs done in support of manufacturing can rely on a high degree of automation, but with the understanding that placement-centering accuracy and final thinning results will suffer. If work must be done at the highest resolution with very exacting placement—essential, for example, on 7 nm gate structures—the best choice is still semiautomated, or "guided," operations.

He also showed what can be achieved on the newest generation of tools, where improvements in ion and electron columns along with advanced in-tool S/TEM imaging combine to produce exceptional results. Ion columns can now run at 500 to 1 kV while producing useable images, enabling superior beam placement with reduced amorphous formation. The SEM columns have a higher current density, enabling better concurrent imaging and endpointing. Finally, in situ S/TEM imaging improvements may eliminate the need to take a trip to a dedicated S/TEM.

Ed Principe of Tescan USA re-introduced the audience to the concept of the analytical cluster tool in his presentation, "Ultra-High Vacuum Modular FIB-SEM Platforms for Advanced Materials Processing and Characterization." As Ed pointed out, the ultrahigh vacuum (UHV) multibeam FIB-SEM for Auger analysis was commercialized nearly 20 years ago. Given the new ion species and analytical techniques we have today, what could we build next?

Ultraclean UHV chambers are required for a number of advanced surface analysis techniques (time-of-flight

secondary ion mass spectrometry, Auger, x-ray photoelectron spectroscopy, ion scattering spectroscopy) on top surfaces or in cross section, with a 3-D understanding of the structure readily available through reconstruction techniques. It also allows for advanced materials processing (nanomachining and growth on pure surfaces) by reducing the contamination factor.

New ion columns are available (liquid metal ion source, liquid metal alloy ion source, plasma, gas field), and beams of gallium, helium, neon, argon, xenon, silicon, gold, and so on are all possible. Each offers different depth versus spread, producing varying machining capabilities and materials processing opportunities.

A modular platform design could allow a purchaser to specify a varying number of ion columns (or multisource columns), high-resolution SEM, advanced analytical techniques, multiple precursor chemistry injectors, and so on, all in one customizable and reconfigurable system.

The final talk was a late-submission FIB circuit edit case study by Hideo Tanaka of FEI/Thermo Fisher Scientific titled "Controlling Timing Delay on Ring-Oscillator Circuits with Quantized FIB-Based Metal Insulator Semiconductor (MIS) Capacitors." The edit challenge was to add a specific timing delay to reduce the operating frequency of a ring oscillator. The operating performance of the ring was directly measurable, so the impact of any edit could be quantified. The author noted that the traditional way of accomplishing this is to add an FIB-deposited resistor, but this requires two connection vias and a cut—something there isn't always room to add. Instead, they took the approach of adding a capacitor to ground on the output (single connection to inverter chain and to a nearby ground). The capacitor itself was made by FIB-deposited metal-insulator-metal plates. The initial-sized capacitor slowed the circuit by approximately 200 Hz—not as much as desired. They then added three additional structures in parallel until it dropped another 230 Hz to the desired amount. The takeaway was that, although the results were not as linear as expected, the technique definitely works. More study is required to understand the layer deposition variables that will lead to a predictable capacitance value for a defined area (dielectric thickness and permittivity value).

INTERNET RESOURCES FOR ENGINEERING

COURSERA

URL: coursera.org

Coursera is a compilation of internet lectures from university institutions around the world. It provides universal access to most topics in the science, technology, engineering, and mathematics fields.

GREATEST ENGINEERING ACHIEVEMENTS OF THE 20TH CENTURY

URL: greatachievements.org

Explore a list of the top 20 achievements from the National Academy of Engineering and learn how engineering shaped a century and changed the world. The website contains detailed historical information, timelines, and personal essays by key innovators for each of the 20 major engineering accomplishments of the 20th century.

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

URL: ansi.org

ANSI oversees the creation, promulgation, and use of thousands of norms and guidelines that directly impact businesses in nearly every sector: from acoustical devices to construction equipment, from dairy and livestock production to energy distribution, and much more. ANSI is also actively engaged in accrediting programs that assess conformance to standards, including globally-recognized cross-sector programs such as the ISO 9000 (quality) and ISO 14000 (environmental) management systems.

AMERICAN SOCIETY FOR ENGINEERING EDUCATION (ASEE)

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PRODUCT NEWS

PRESS RELEASE SUBMISSIONS:
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Larry Wagner, LWSN Consulting Inc.
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FEI OFFERS EFA WORKFLOW SOLUTIONS

Semiconductor manufacturers can turn to new electrical failure analysis (EFA) solutions for the tools required to identify and analyze faults in their products. The new nProber III fault localization and transistor characterization tool developed by FEI (Hillsboro, Ore.) provides process development and failure analysis down to the 7 nm technology node. The new Meridian 7 optical fault isolation tool, also developed by FEI, is designed to provide the resolution needed for nondestructive localization of electrical faults at sub-10-nm nodes.

FEI's Meridian 7 optical fault isolation tool

"Automation is a high priority in our roadmap," said Cecelia Campochiaro, Vice President of EFA Solutions at Thermo Fisher Scientific. "The nProber III system begins our move toward automating the nanoprobing technique by incorporating intelligent-guided operations designed to improve time-to-results and reduce the skill required to run the tool."

These new solutions are part of a complete EFA workflow that includes fault isolation, electrical probing, delayering, sample preparation and imaging, and, when needed, atomic-level imaging in a transmission electron microscope (TEM). The nProber III allows FA engineers to find and characterize individual devices preparatory to extracting thin sectional samples for physical failure analysis in the TEM. In some critical applications, nanoprobing can potentially increase TEM success rates. Designed to be an effective and easy-to-use tool, the nProber III doubles the resolution and probe stability over its predecessor.

The new Meridian 7 provides visible laser voltage imaging and probing as well as dynamic laser stimulation on sub-10-nm devices. By avoiding a requirement for ultrathin substrates, it preserves the integrity and functionality of the device under test to provide a reliable and practical production solution. It offers a 25% optical resolution enhancement over the previous-generation system and has a smaller spot size for better fault localization. In addition, the new Meridian 7 offers more certainty in navigation and computer-aided design overlay, less cross-talk, and higher waveform signal-to-noise over its predecessor.

For more information: web: bit.ly/2fLQZvH.

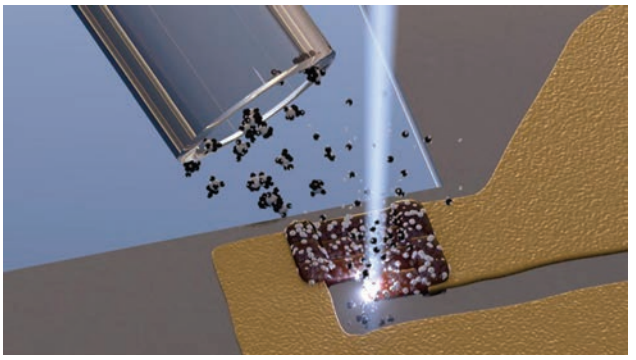
3-D NANOPRINTING IMPROVES AFM PERFORMANCE

Tiny sensors made through nanoscale 3-D printing may be the basis for the next generation of atomic force microscopes (AFMs). These nanosensors can enhance the microscopes' sensitivity and detection speed by miniaturizing their detection component up to 100 times. The sensors were used in a real-world application for the first time at École Polytechnique Fédérale de Lausanne (EPFL) in Switzerland, and the results were published in *Nature Communications.* The sensor is made up of highly conductive platinum nanoparticles surrounded by an insulating carbon matrix.

Atomic force microscopy is based on powerful technology that works a little like a miniature turntable. A tiny cantilever with a nanometric tip passes over a sample and traces its relief, atom by atom. The tip's infinitesimal up-and-down movements are picked up by a sensor so that the sample's topography can be determined. One way to improve AFMs is to miniaturize the cantilever, because this will reduce inertia, increase sensitivity, and speed up detection. Researchers at EPFL's Laboratory for Bio- and Nano-Instrumentation achieved this by equipping the cantilever with a 5-nm-thick sensor made with a nanoscale 3-D printing technique. "Using our method, the

cantilever can be 100 times smaller," says Georg Fantner, the lab's director.

The nanometric tip's up-and-down movements can be measured through the deformation of the sensor placed at the fixed end of the cantilever. However, because the researchers were dealing with minute movements—smaller than an atom—they had to pull a trick out of their hat. Together with Michael Huth's lab at Goethe Universität at Frankfurt am Main, Germany, they developed a sensor made up of highly conductive platinum nanoparticles surrounded by an insulating carbon matrix. Under normal conditions, the carbon isolates the electrons. However, at the nanoscale, a quantum effect comes into play: Some electrons jump through the insulating material and travel from one nanoparticle to the next. "It's sort of like if people walking on a path came up against a wall, and only the courageous few managed to climb over it," said Fantner. When the shape of the sensor changes, the nanoparticles move farther away from each other, and the electrons jump between them less frequently. Changes in the current thus reveal the deformation of the sensor and the composition of the sample.



The sensor is made up of highly conductive platinum nanoparticles surrounded by an insulating carbon matrix. Source: EPFL

The researchers' real feat was in finding a way to produce these sensors in nanoscale dimensions while carefully controlling their structure and, by extension, their properties. "In a vacuum, we distribute a precursor gas containing platinum and carbon atoms over a substrate. Then we apply an electron beam. The platinum atoms gather and form nanoparticles, and the carbon atoms naturally form a matrix around them," said Maja Dukic, the article's lead author. "By repeating this process, we can build sensors with any thickness and shape we want. We have proven that we could build these sensors and that they work on existing infrastructures. Our technique can now be used for broader applications, ranging from biosensors and antilock braking sensors for cars to touch sensors on flexible membranes in prosthetics and artificial skin."

For more information: web: nature.com/articles/ncomms12487.

ECONO BOARD PROBES ENHANCE MEASUREMENTS

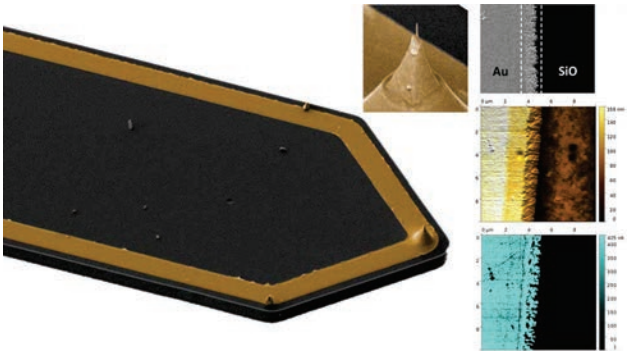
Econo Board probes are the first group released from Oxford Instruments Asylum Research's new line of SurfRider probes. "Econo Board probes can be used by all atomic force microscope users doing routine measurements," said Teimour Maleki, Director of MEMS and Business Technology at Asylum Research (Santa Barbara, Calif.). "We're excited to now offer not only an economical probe but one that can be used for many advanced modes. When you buy probes from Asylum Research, you are assured that the industry's best customer support team will help you select the optimal probe for your sample and experiment."

Econo Board probes are available in eight different models covering resonance frequencies ranging from 13 to 300 kHz. Econo Board probes come in PtIr-coated and noncoated models. They are ideal for all atomic force microscope brands, models, and modes, including tapping mode, force modulation, contact mode, and nanoelectrical and nanomechanical characterization modes.

For more information: web: oxinst.com.

SELF-SENSING CANTILEVERS AVAILABLE FOR AFSEM

GETec and Nanosurf (Suwon, Korea) now offer self-sensing conductive cantilevers for the atomic force scanning electron microscope (AFSEM) that enable conductivity probing in the vacuum environment of the SEM. The SEM is an established tool for imaging, processing, and materials analysis of surfaces. However, it is not possible to measure local electrical properties, such as the



Self-sensing conductive cantilever with solid platinum tip

conductivity of the surface. With micromanipulators, local conductivity can be probed only pointwise.

Measurement of local conductivity is a standard imaging mode with atomic force microscopy (AFM) in air and is used as an analytical tool in failure analysis, measurement of doping concentration, and materials characterization. However, surface contamination and the common water film between tip and sample reduce reliability and repeatability.

Enter the AFSEM, the AFM for the SEM. With its new, self-sensing conductive cantilevers, it enables correlative conductivity probing in the vacuum environment of the SEM and reduces the problems encountered in air. The cantilevers feature solid platinum tips, reducing tip radius compared to cantilevers with conductive coatings.

For more information: web: nanosurf.com.

TERAVIEW ADDS NEW TERAHERTZ APPLICATIONS

TeraView (Cambridge, U.K.), the pioneer and leader in terahertz technology and solutions, announced further expansion of its installed instrument base as well as the addition of new terahertz applications. The company now has over 100 systems in the field, further establishing TeraView's position as the leading global provider of terahertz technology and solutions. TeraView's systems are deployed at leading research laboratories and at production facilities around the world. Key industrial applications include the pharmaceutical, automotive, and semiconductor packaging industries.

Recent system sales marked introduction of the TeraPulse terahertz imager and spectrometer, coinciding with the launch of the EOTPR 5000, TeraView's fully automated terahertz system for the inspection of advanced semiconductor packaging. TeraView customers are now located in more than twenty countries around the world, and systems are deployed across a range of industries where the unique capabilities of terahertz light overcome the restrictions of conventional imaging and diagnostic technologies, including greater accuracy and sensitivity to faults, defects, and quality variations in customer products.

Since the initial sale of TeraView's first system to the pharmaceutical industry, TeraView has continued to innovate and expand its system deployment and application expertise into various industries and countries, with repeat sales to a technologically diverse customer base. This expansion has led to recent appointments of TeraView agents in Russia, South Korea, Taiwan, and Japan. The company has also established direct technical support in the United States and Asia to augment its team in Europe.

Dr. Don Arnone, TeraView's Chief Executive Officer, commented, "The fact that we have now sold over 100 turn-key systems into applications in both research and development and industrial inspection is a milestone not just for TeraView but for the expansion of terahertz technology itself and its uses. This expansion is based on close collaboration with our customers, researchers, and development engineers across the world, and it demonstrates the global footprint that terahertz technology now has across a range of industries and scientific disciplines."

For more information: web: teraview.com.

NATIONAL INSTRUMENTS ANNOUNCES NEW OSCILLOSCOPE

National Instruments (Austin, Texas), the provider of platform-based systems that enable engineers and scientists to solve the world's greatest engineering challenges, announced a new high-speed, high-resolution, high-voltage oscilloscope. The PXIe-5164 is built on the open, modular PXI architecture and includes a user-programmable field-programmable gate array (FPGA) to help aerospace/defense, semiconductor, and research/physics applications that require high-voltage measurements and high levels of amplitude accuracy.

"PXI oscilloscopes from National Instruments reduce test time, increase channel density, and now deliver even better measurement flexibility with the combination of high bandwidth, resolution, and input voltage," said Steve Warntjes, Vice President of Research and Development at National Instruments. "Our new PXIe-5164 oscilloscope can make some measurements that box instruments today just can't handle. If you want to measure a high-voltage signal of up to 100 V_{pp} at up to 1 GS/s, you can now use the same instrument to see small signal details that would normally be hidden by the noise of the instrument, thanks to the 14-bit analog-to-digital converter."

The PXIe-5164 features:

- Two 14-bit channels sampled at 1 GS/s with 400 MHz bandwidth
- Two Category II-rated channels with voltage input range to 100 V_{pp} with programmable offsets allowing measurements up to ±250 V
- Up to 34 channels to build parallel, high-channel-count systems in a compact form factor in a single PXI chassis
- A 3.2 GB/s streaming data rate enabled by eight lanes of PCI Express Gen 2 bus communication

- A Xilinx Kintex-7 410 FPGA to create custom internet protocol, including filtering or triggering, programmed through LabVIEW

PXI oscilloscopes deliver the ease of use expected from a box oscilloscope. Engineers can use the interactive soft front panels in NI-SCOPE software to make basic measurements, debug automated applications, or view the scope data while the test program runs. The driver includes help files, documentation, and ready-to-run example programs to assist in test code development, and it includes a programming interface that works with a variety of development environments, such as C, Microsoft.NET, and LabVIEW system design software. Engineers can also use PXI oscilloscopes with TestStand test management software, which simplifies the creation and deployment of test systems in the lab or on the production floor.

PXI oscilloscopes are an important part of the National Instruments platform and ecosystem that engineers can use to build smarter test systems. These test systems benefit from more than 600 PXI products ranging from direct current to mmWave and feature high-throughput data movement using PCI Express bus interfaces and sub-nanosecond synchronization with integrated timing and triggering. Supported by a vibrant ecosystem of partners, add-on internet protocol, and applications engineers, the National Instruments platform helps to dramatically lower the cost of test, reduce time to market, and future-proof testers for tomorrow's challenging requirements.

For more information: web: ni.com.

TELEDYNE LECROY INTRODUCES HIGH-DEFINITION OSCILLOSCOPE

Teledyne LeCroy, Inc. (Chestnut Ridge, NY) introduced the latest offering in its high-definition oscilloscope line. The HDO9000 high-definition oscilloscope uses HD1024 high-definition technology that automatically optimizes vertical resolution under each measurement condition to deliver 10 bits of vertical resolution. The combination of the next-generation most advanced user interface (MAUI) with OneTouch and a big, bright, 15.4 in. capacitive touch screen takes oscilloscope efficiency, intuitiveness, and ease of use to a completely new level. The HDO9000 high-definition oscilloscopes offer 10-bit resolution, bandwidths of 1 to 4 GHz, and sample rates of 40 GS/s, enabling efficient and accurate debug in high definition.

Teledyne LeCroy's HDO9000 high-definition oscilloscope

"Teledyne LeCroy has been providing industry-leading high-definition oscilloscopes since 2011, and the HDO9000 adds significant capabilities to the HDO line of products," said Tom Reslewic, Chief Executive Officer of Environmental and Electronic Measurement Instrumentation. "The addition of the HD1024 technology to an exceptionally deep analysis toolbox enables the HDO9000 to easily uncover even difficult-to-find signal abnormalities."

The HDO9000 and MAUI with OneTouch allows users to perform all common operations with a single touch of the 15.4 in. high-resolution display, optimized for convenience and efficiency. Users' instinctive interaction with the oscilloscope dramatically reduces measurement setup time. Furthermore, in addition to the versatile standard toolset, Teledyne LeCroy offers a broad variety of optional software packages to equip the HDO9000 for all validation and debug requirements, ranging from automated standards compliance packages to flexible debugging toolkits.

For more information: web: teledynelecroy.com.

BOARD OF DIRECTORS NEWS

EDFAS BOARD OF DIRECTORS REPORT

Bill Vanderlinde, EDFAS Secretary, IARPA
william.vanderlinde@iarpa.gov

The EDFAS Board of Directors held its annual face-to-face meeting on Saturday, November 5, 2016, in Fort Worth, Texas, preceding the ISTFA event. Board President Zhiyong Wang kicked off the meeting with the President's report, a high-level review of 2016. In his report, Zhiyong summarized recent accomplishments, including two new EDFAS awards, an ISTFA 2016 third track, new tutorial topics, three short courses, and creation of an International Growth Committee. Future plans include an ISTFA event at Semicon Asia in 2018, and ISTFA co-location with the International Test Conference in Phoenix in 2018. Our strategic focus is on strengthening our credentials and growing through our membership, technical excellence, and strategic collaborations and partnerships.

ASM International Interim Executive Director Tom Dudley announced that ASM has brought on new leadership with substantial business expertise to renew ASM: Managing Director Bill Mahoney, Chief Information Officer Ron Aderhold, and Membership Manager Susan Davis. Initiatives include running ASM as a business, a new commitment to ASM affiliates, and investing in laboratory upgrades and an additive manufacturing lab at ASM Headquarters in Materials Park, Ohio. Chief Information Officer Ron Aderhold explained ASM's digital transformation strategy to leverage the cloud and use a streamlined application suite. The strategy will be digital first, not print first, resulting in enriched on-line content.

Committee chairs shared year-to-date progress and 2017 plans for their respective areas, covering membership, *EDFA* magazine, education, ISTFA, the journal, and international growth.

The education committee is working to engage the next generation of engineers. Education initiatives include a certificate program and an on-line learning community.

Felix Beaudoin, Editor of *EDFA*, reported that the magazine continues to have excellent technical content and strong advertising. A recent survey of the EDFAS membership confirms the value that members place on the magazine's technical content. Please contact Felix if you are interested in writing an article!

Szu Huat Goh, Chair of the International Growth Committee, discussed sponsoring an ISTFA booth at events in Asia. Our international visibility will increase as we prove our value to overseas audiences.

Looking forward to next year, General Chair Sam Subramanian provided a preview of ISTFA 2017 in Pasadena, California, which will be themed "Striving for 100% Success Rate." Felix Beaudoin was announced as Technical Program Chair for ISTFA 2017.

The Board continues to pursue international collaborations, virtual content, and social media using web-based technologies. They are also seeking to better leverage EDFAS volunteers and are looking to implement failure analysis tool roadmapping.

The Board of Directors strives to strengthen the visibility and credibility of our Society by providing value to EDFAS members and, through its volunteers, beneficial contributions to our industry. Your engagement in EDFAS is highly encouraged. Please feel free to connect with any Board member to discuss your ideas or interest in volunteering in the Society.

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TRAINING CALENDAR

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SEMICONDUCTOR ONLINE TRAINING

EDFAS offers online training specialized for semiconductor, microsystems, and nanotechnology suppliers and users. These online training courses are designed to help engineers, technicians, scientists, and managers understand each of these dynamic fields. This one-year subscription provides access to several courses covering semiconductor failure analysis, design, packaging, processing, technology, and testing. Find out more by visiting edfas.org and clicking on Education.

February 2017

EVENT	DATE	LOCATION
Fundamentals of Non-Destructive Testing	1/30-2/1	Novelty, OH
Introduction to Metallurgical Lab Practices	2/13-15	Novelty, OH
Science and Technology of Materials	2/21-23	Novelty, OH
How to Organize and Run a Failure Investigation	2/27-28	Foothill Ranch, CA
Contact: ASM International		
Failure and Yield Analysis	1/30-2/2	Portland, OR
Advanced CMOS/ FinFET Fabrication	2/6	Portland, OR
Semiconductor Statistics	2/7-8	Portland, OR
Contact: Semitracks, Inc.		
IMAPS 12th European Advanced Technology Workshop on Micropackaging and Thermal Management	2/1-2	La Rochelle, France
Contact: IMAPS France		
Pan-Pacific Microelectronics Symposium	2/6-9	Kauai, HI
Contact: SMTA		

March 2017

EVENT	DATE	LOCATION
Principles of Failure Analysis	3/1-3	Foothill Ranch, CA
Metallurgy for the Non-Metallurgist	3/6-7	Novelty, OH
Metallographic Techniques	3/20-23	Novelty, OH
Component Failure Analysis	3/20-23	Novelty, OH
Contact: ASM International		

March 2017 (cont'd)

EVENT	DATE	LOCATION
Reverse Engineering: A Material Perspective	3/27-29	Novelty, OH
Metallographic Interpretation	3/27-30	Westlake, OH
Principles of Failure Analysis	3/27-30	Novelty, OH
Contact: ASM International		
Dallas Expo & Tech Forum	3/7	Plano, TX
Houston Expo & Tech Forum	3/9	Stafford, TX
Intermountain (Boise) Expo & Tech Forum	3/29	Boise, ID
Contact: SMTA		
Semiconductor Reliability	3/13-15	Singapore/Malaysia
Contact: Semitracks, Inc.		
Grounding and Shielding: The Essence of EMC Design	3/13-16	Barcelona, Spain
RF Component and System Measurements	3/13-17	Barcelona, Spain
Contact: CEI-Europe AB		
South East Asia Technical Conference on Electronics Assembly	3/28-30	Penang, Malaysia
Contact: SMTA_SE Asia		

April 2017

EVENT	DATE	LOCATION
Future Wireless Networks: 5G/6G Technology	4/3-5	Amersfoort, The Netherlands
Contact: CEI-Europe AB		
West Penn Expo & Tech Forum	4/5	Monroeville, PA
Contact: SMTA		

April 2017 (cont'd)

EVENT	DATE	LOCATION
Practical Fractography	4/5-6	Lansing, NY
Corrosion	4/24-27	Novelty, OH
Metallography for Failure Analysis	4/24-27	Novelty, OH
Contact: ASM International		

May 2017

EVENT	DATE	LOCATION
Defect-Based Testing	5/3-4	Munich, Germany
Failure and Yield Analysis	5/8-11	Munich, Germany
Semiconductor Reliability and Qualification	5/15-18	Munich, Germany
Semiconductor Statistics	5/22-23	Munich, Germany
Contact: Semitracks, Inc.		
Michigan Expo & Tech Forum	5/11	Grand Rapids, MI
Carolinas Expo & Tech Forum	5/16	Greensboro, NC
Contact: SMTA		
Contamination, Cleaning & Coating Conference	5/23-24	Amsterdam, The Netherlands
Contact: SMART Group		

Contact Information

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LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Thermography and Thermal-Related Phenomena

Michael R. Bruce, Consultant
mike.bruce@earthlink.net

The current column covers peer-reviewed articles published since 2014 on thermography and thermal-related phenomena. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

- M.S. Anwar, J. Alam, M. Wasif, et al.: **"Fourier Analysis of Thermal Diffusive Waves,"** *Am. J. Phys.,* 2014, *82*, p. 928.
- D.G. Cahill, G. David, L. Shi, et al.: **"Nanoscale Thermal Transport. II. 2003–2012,"** *Appl. Phys. Rev.,* 2014, *1*, p. 011305.
- D.R. Cremons, D.A. Plemmons, and D.J. Flannigan: **"Femtosecond Electron [Video] Imaging of Defect-Modulated Phonon Dynamics [in Semiconductors],"** *Nat. Commun.,* 2016, *7*, p. 11230; also see D. McCormick: **"Watch [Nanoscale] Heat Surge across Semiconductors at the Speed of Sound,"** *IEEE Spectrum,* April 19, 2016, spectrum.ieee.org/tech-talk/at-work/test-and-measurement/video-sees-heat-surge-across-nanometers-at-the-speed-of-sound, accessed April 20, 2016.
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- F. Fertig, J. Greulich, and S. Rein: **"Spatially Resolved Determination of the Short-Circuit Current Density of Silicon Solar Cells via Lock-In Thermography,"** *Appl. Phys. Lett.,* 2014, *104*, p. 201111.
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- J. Hepp, F. Machui, H.-J. Egelhaaf, et al.: **"Automatized Analysis of IR-Images of Photovoltaic Modules and Its Use for Quality Control of Solar Cells,"** *Energy Sci. Eng.,* 2016, *4*, p. 363.
- W. Jeong, S. Hur, E. Meyhofer, et al.: **"Scanning Probe Microscopy for Thermal Transport Measurements,"** *Nanoscale Microscale Thermophys. Eng.,* 2015, *19*, p. 279.
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- M. Kuball and J.W. Pomeroy: **"A Review of Raman Thermography for Electronic and Opto-Electronic Device Measurement with Submicron Spatial and Nanosecond Temporal Resolution,"** *IEEE Trans. Device Mater. Reliab.,* 2016, *16*, p. 667.
- J. Maassen and M. Lundstrom**: "Steady-State Heat Transport: Ballistic-to-Diffusive with Fourier's Law,"** *J. Appl. Phys.,* 2015, *117*, p. 035104.
- F. Menges, H. Riel, and A. Stemmer: **"Nanoscale Thermometry by Scanning Thermal Microscopy,"** *Rev. Sci. Instrum.,* 2016, *87*, p. 074902.
- M. Partanen, K.Y. Tan, and J. Govenius: **"Quantum-Limited Heat Conduction over Macroscopic Distances,"** *Nat. Phys.,* 2016, *12*, p. 460.
- D. Pile: **"Infrared Optics: Nanoscale Heat [Transfer],"** *Nat. Photon.,* 2016, *10*, p. 79.
- S.Y. Ryu, D.K. Kim, J.K. Kim, et al.: **"Surface-Temperature Measurement and Submicron Defect Isolation for**

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- A.V. Sachenko, Y.V. Kryuchenko, V.P. Kostylyov, et al.: **"Temperature Dependence of Photoconversion Efficiency in Silicon Heterojunction Solar Cells: Theory vs. Experiment,"** *J. Appl. Phys.,* 2016, *119*, p. 225702.
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INTERNET RESOURCES FOR ENGINEERING

EUROPEAN ELECTRONIC COMPONENT MANUFACTURERS ASSOCIATION (EECA)

Under the EECA's umbrella organization, there are two autonomous industry associations whose members come from manufacturing and related industries as well as from national associations:

• European Passive Components Industry Association (EPCIA)

URL: eusemiconductors.eu/epcia/epcia-home

EPCIA represents and promotes the common interests of the passive components manufacturers active in Europe and ensures an open and transparent market for passive components in Europe as part of the global marketplace.

• European Semiconductor Industry Association (ESIA)

URL: eusemiconductors.eu/esia/home

ESIA is the organization representing the European semiconductor industry in Brussels. Semiconductor products are the key enabler for improved energy consumption and performance across a wide range of everyday technology applications in society. These applications in the field of industrial operations, consumer electronics, healthcare, security, and energy devices have contributed to improved energy efficiency for positive societal change.

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INTERNET RESOURCES FOR ENGINEERING

THE SCIENCE, TECHNOLOGY AND BUSINESS DIVISION OF THE LIBRARY OF CONGRESS

URL: loc.gov/rr/scitech/general.html

The Science, Technology and Business Division of the Library of Congress (under the "Researchers" tab) is tasked with providing reference and bibliographic services and developing the collections in all areas of science and technology (with the exception of clinical medicine and technical agriculture) and business, management, and economics. Reference assistance and access to the Library's scientific collections is provided through their Science Reference Services link.

NATIONAL RESEARCH COUNCIL CANADA (CANADA INSTITUTE FOR SCIENTIFIC AND TECHNICAL INFORMATION, OR CISTI)

URL: nsl-bsn.nrc-cnrc.gc.ca/eng/home

The National Research Council is the leading agency for research and development in Canada. It began as the National Science Library in 1957 and changed to CISTI in 1974 to reflect the wide scope of services provided and the increasing role in development of electronic information products and services for the scientific/technical community.

WORLD SEMICONDUCTOR COUNCIL (WSC)

URL: semiconductorcouncil.org

The WSC is an international forum that brings together industry leaders to address issues of global concern to the semiconductor industry. It is comprised of the semiconductor industry associations of the United States, Korea, Japan, Europe, China, and Chinese Taipei. The goal of the WSC is to promote international cooperation in the semiconductor sector to facilitate the healthy growth of the industry from a long-term, global perspective.

SEMICONDUCTOR INDUSTRY ASSOCIATION (SIA)

URL: semiconductors.org

The SIA is the voice of the U.S. semiconductor industry, one of America's top export industries and a key driver of America's economic strength, national security, and global competitiveness. The SIA seeks to strengthen U.S. leadership of semiconductor manufacturing, design, and research by working with Congress, the Administration, and other key industry stakeholders to encourage policies and regulations that fuel innovation, propel business, and drive international competition.

GUEST COLUMNISTS

CHALLENGES IN USING MOBILE DEVICES FOR AUTOMOTIVE ELECTRONICS

E. Jan Vardaman and Linda Bal, TechSearch International, Inc.
tsi@techsearchinc.com

Electronic content in automotive applications has increased dramatically over the past few years. Automobiles are on the threshold of a radical change in technology. The industry has moved from ceramic to leadframe and laminate and packages. Interconnect technology is transitioning from wire bond to flip-chip and wafer-level packaging (WLP), including fan-out WLP. Vehicles have increased connectivity, improved self-diagnostics, and a greater number of safety features.

Increasingly, semiconductors that were not specifically developed for the automotive market are being used in vehicles. Many innovations desired in future vehicles have been designed for larger market segments, such as consumer and computer, that can justify the required research and development and are able to drive down cost with high-volume manufacturing. Some examples of these features include higher graphics capabilities in infotainment, cluster and head-up solutions, and Advanced Driver Assist Systems (ADAS) technology. There are three main scenarios of ADAS:

- Systems that provide feedback to the driver when an obstacle or situation exists. The driver has the sole discretion to determine and take action.
- Systems where the car electronics take action after the driver has been warned but fails to take action
- Autonomous driving systems where the driver has no input

New automotive safety features include increased connectivity, improved self-diagnostics, crash-avoidance technology, and advanced driver assistance. This translates into an increased use of image sensors and radar.

Automotive electronics qualification requirements are classified by AEC-Q100 grades that depend on the ambient operating temperature range (Table 1). Grade 0 corresponds to the harshest operating environment and critical power train operations. Most ADAS operations fit in Grade 1. Driver information systems displays or communication devices fit in Grade 2 or 3. Table 2 provides details of AEC-Q100 qualification tests.

"MANY INNOVATIONS DESIRED IN FUTURE VEHICLES HAVE BEEN DESIGNED FOR LARGER MARKET SEGMENTS, SUCH AS CONSUMER AND COMPUTER, THAT CAN JUSTIFY THE REQUIRED RESEARCH AND DEVELOPMENT AND ARE ABLE TO DRIVE DOWN COST WITH HIGH-VOLUME MANUFACTURING."

Members of the German Electrical and Electronic Manufacturers' Association (ZVEI) have formed a new working group to create awareness of the potential differences between automotive and consumer-grade

Table 1 AEC-Q100 grades vary based on operating environment temperature range

AEC-Q100	Ambient operating temperature range
Grade 0	–40 to +150 °C
Grade 1	–40 to +125 °C
Grade 2	–40 to +105 °C
Grade 3	–40 to +85 °C

Source: AEC-Q100

components. This working group has reviewed the cradle-to-grave process and requirements of each and has identified 66 potential differences. According to the ZVEI group, "More and more semiconductors that were not specifically developed for the automotive market and their use profiles are being used in vehicles. Given the fact that the automotive value chain increasingly introduces ADAS and safety functions into vehicles, any failing device in any relevant electronic control unit (ECU) within the car can impact the application and endanger human health or even life. The consequential safety risk impacts not only the involved companies but may also lead to direct, personal consequences for the responsible employee or manager."

At the FutureCar Workshop, organized by the Georgia Institute of Technology and Semiconductor Equipment and Materials International, participants discussed many of the issues associated with the development of packaging for automotive electronics, especially considering the increasing number of safety features, which include the increased use of sensors as well as combinations of sensors with controllers. These sensors operate in environments that are harsher than mobile devices.

In many cases, zero-defect quality and 15-plus-year reliability at the ECU level cannot be accomplished with standard components alone. Shortcomings can be mitigated by collaboration among automotive original equipment manufacturers, Tier 1 suppliers, and component makers regarding modifying vehicle and/or device mission profile and adding system-level solutions, such as redundancy, external component protection, and/or cooling. Participants at the workshop agreed that future cooperation and collaboration is necessary to ensure reliability for automotive electronics.

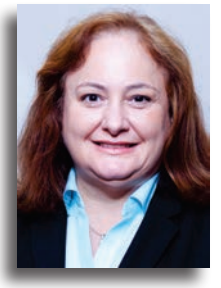
Table 2 AEC-Q100 qualification tests

Stress	Standard JEDEC conditions	AEC-Q100 Grade 0	AEC-Q100 Grade 1	AEC-Q100 Grades 2 and 3
Preconditioning	**MSL 1:** 85 °C/85% relative humidity (RH) for 168 h, unlimited floor life **MSL 2:** 85 °C/60% RH for 168 h, 1 year floor life **MSL 2a:** 30 °C/60% RH for 696 h, 4 weeks floor life **MSL 3:** 30 °C/60% RH for 192 h, 1 week floor life	Min Level 3, per J-Std-020	Min Level 3, per J-Std-020	Min Level 3, per J-Std-020
Temperature cycling	Condition A: –55 to 85 °C Condition B: –55 to 125 °C Condition C: –65 to 150 °C	Precondition before –55 to 150 °C for 2000 cycles	Precondition before –55 to 150 °C for 1000 cycles –65 to 150 °C for 500 cycles	Precondition before **Grade 2:** –55 to 125 °C for 1000 cycles **Grade 3:** –55 to 125 °C for 500 cycles
Temperature/ humidity bias (THB)	THB: 85 °C/85% RH for 1000 h	Precondition before THB: 85 °C/85% RH for 1000 h		
Unbiased highly accelerated stress test (HAST)	Unbiased HAST: 130 °C/85% RH for 96 h or 110 °C/85% RH for 264 h	Precondition before unbiased HAST: 130 °C/85% RH for 96 h or 110 °C/85% RH for 264 h		
High-temperature storage life	Condition A: +125 °C Condition B: +150 °C Condition C: +175 °C	175 °C for 1000 h or 150 °C for 2000 h	150 °C for 1000 h or 175 °C for 500 h	125 °C for 1000 h or 150 °C for 500 h

Note: Typical package-related tests. Additional device tests required: high-temperature operating life, early life failure rate, program/erase endurance, power and temperature cycling. Source: AEC-Q100, JESD22

ABOUT THE AUTHORS

E. Jan Vardaman is the president and founder of TechSearch International, Inc., which has provided analysis on technology and market trends in semiconductor packaging since 1987. She is the co-author of *How to Make IC Packages* (published in Japanese by Nikkan Kogyo Shinbunsha), a columnist with *Circuits Assembly Magazine,* and the author of numerous publications on 2.5- and 3-D TSV trends. Jan is a member of the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society, International Microelectronics and Packaging Society, Institute for Interconnecting and Packaging Electronic Circuits, Microelectronics Packaging and Test Engineering Council, and Semiconductor Equipment and Materials International. She was elected to two terms on the IEEE CPMT Board of Governors. Prior to founding TechSearch International, Jan served on the corporate staff of Microelectronics and Computer Technology Corporation, the electronics industry's first precompetitive research consortium.



Linda Bal, senior analyst, has more than 25 years' experience in the design, test, and manufacturing of electronic packaging for semiconductors and systems. She has held positions at Freescale, Motorola, Microelectronics and Computer Technology Corporation, and Eastman Kodak and has also authored or co-authored numerous publications. She is a member of IEEE, JEDEC, and the International Microelectronics Assembly and Packaging Society (IMAPS). A member of the IMAPS technical committee since 2007, Linda's contributions include chairing the flip-chip/wafer-level packaging track for the Device Packaging Conference in 2013 and 2014, co-chairing the flip-chip track in 2009 and 2010, and moderating technical panel discussions in 2011 and 2012. Linda received her BSEE degree from Purdue University in 1985.

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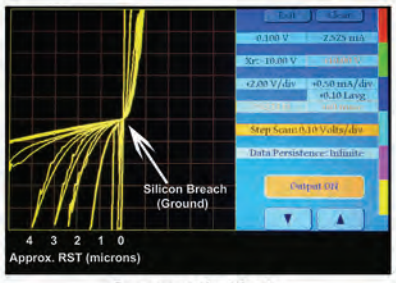

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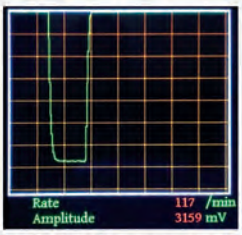
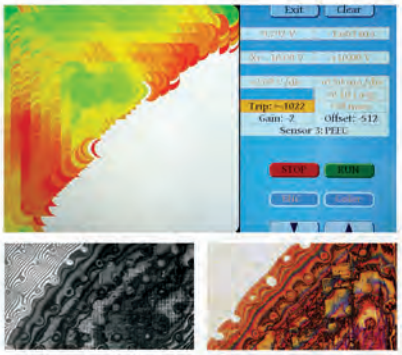
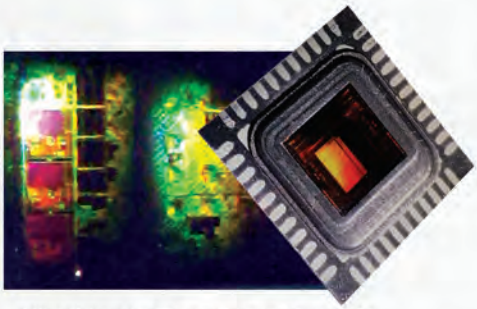


'Soft' Oscilloscope Mode



NIR and VISIBLE Images show the same position on the Plot screen for silicon breach.



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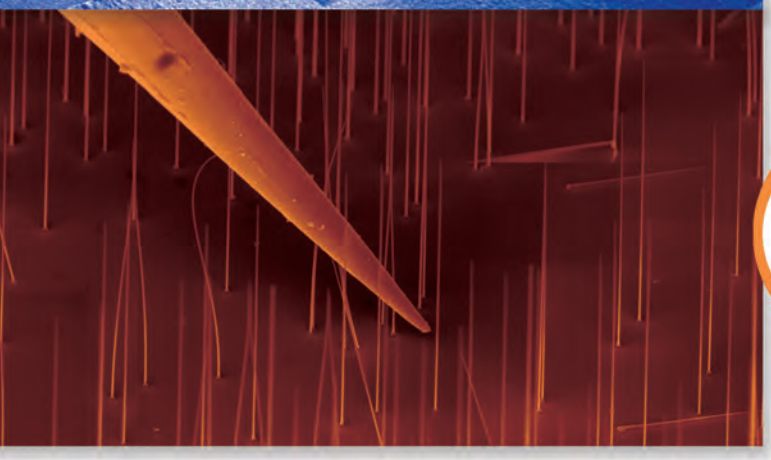

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