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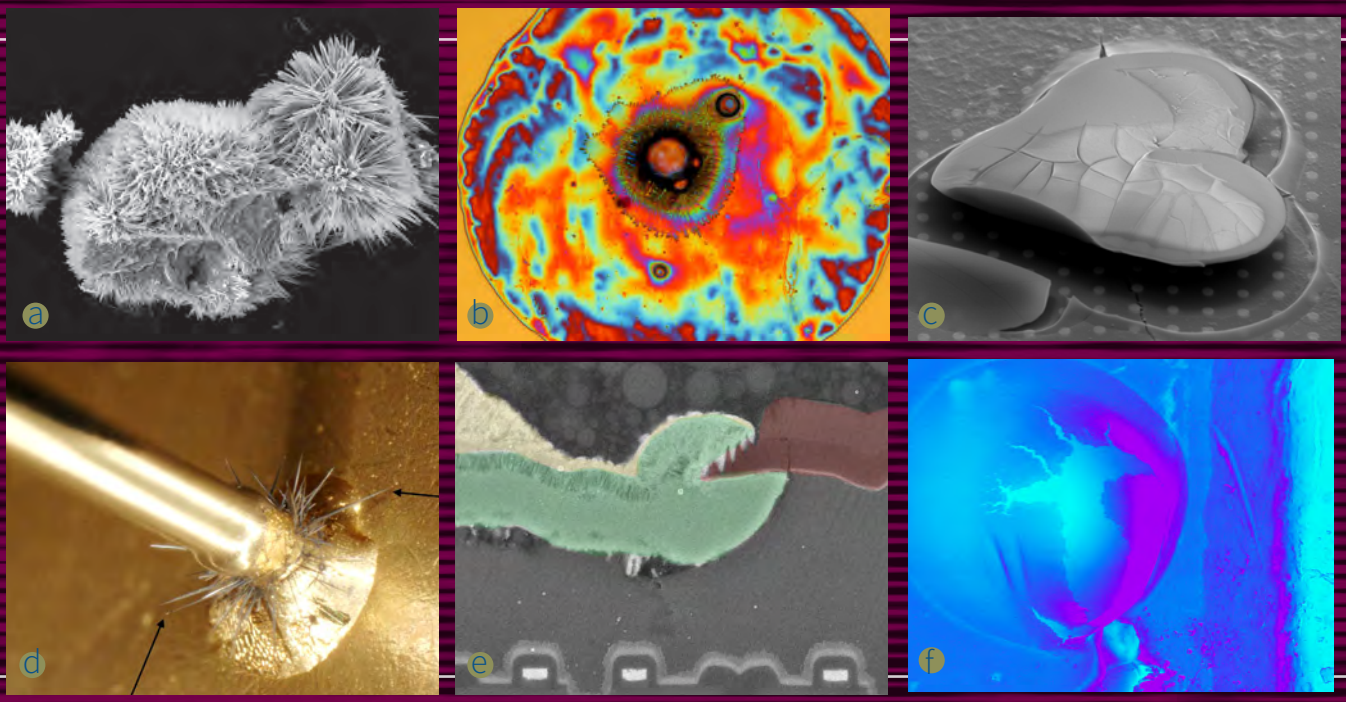

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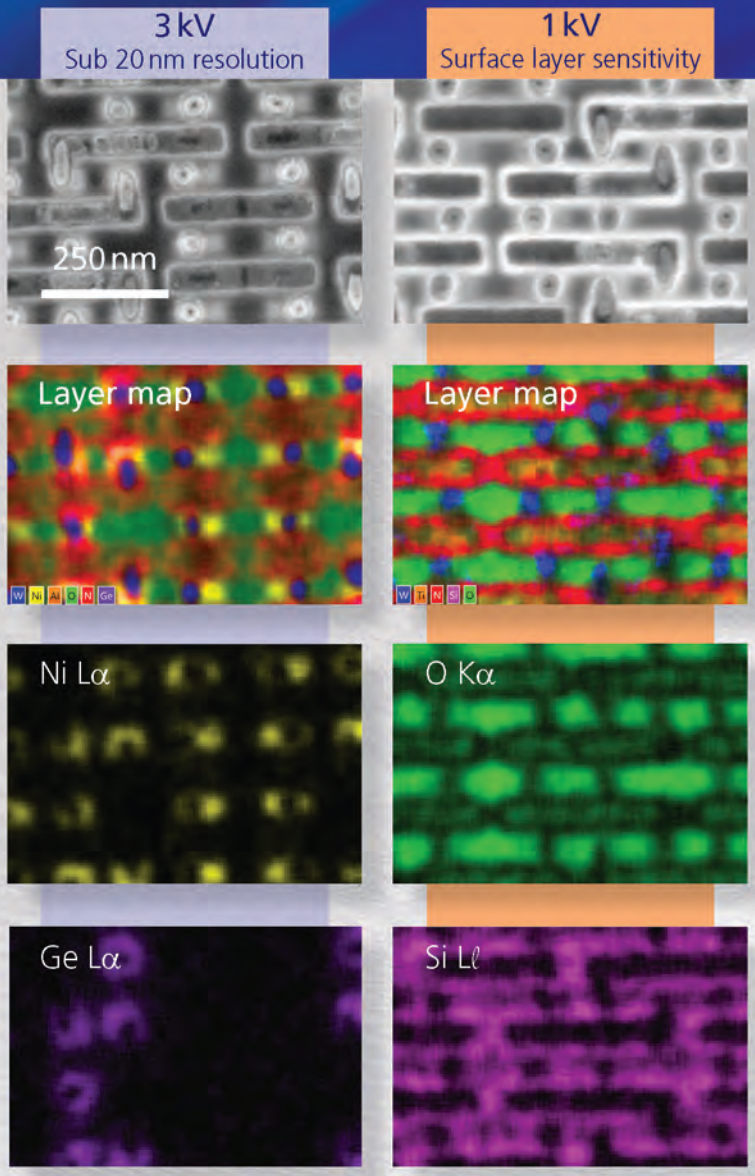

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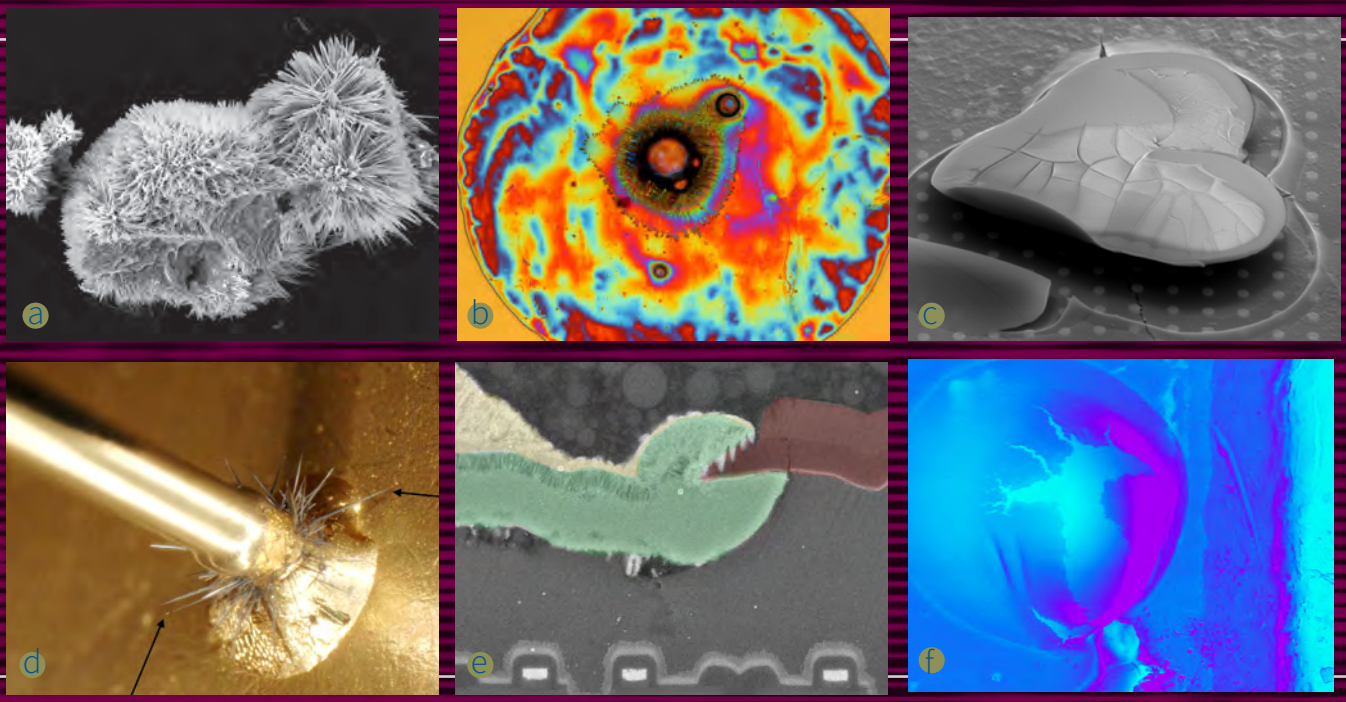

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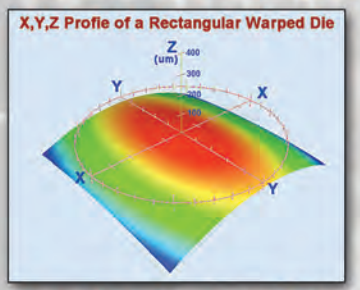

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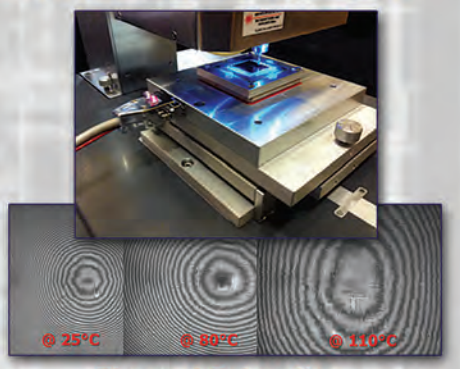

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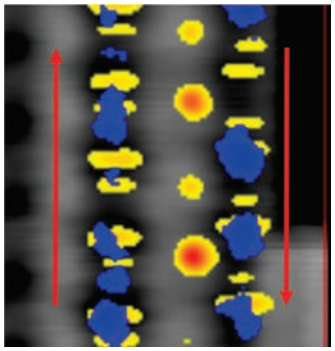

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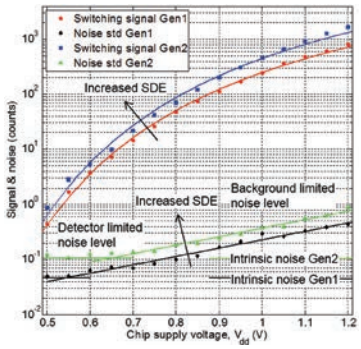

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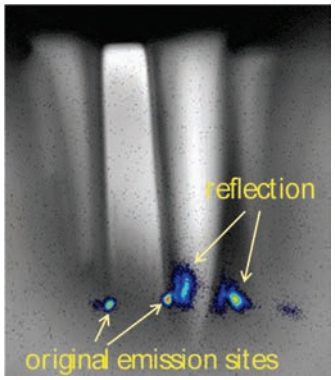

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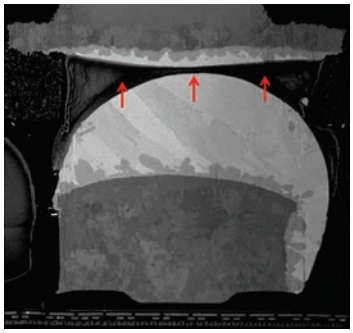

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ABOUT THE COVER

See page 59 for a description of the contest winners' collage on the cover.

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PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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GUEST EDITORIAL

FAILURE ANALYSIS IN HIGH-VOLUME MANUFACTURING

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The ever-increasing financial stakes faced by semiconductor high-volume manufacturing (HVM) on moving to the next node have propelled failure analysis (FA) to levels unimaginable even 20 years ago. The primary driving forces behind this can be summed up as resulting from:

- Increased process complexity (new materials and structures)
- Increased number of mask steps per device node
- Tighter process control

The increased process complexity derives from the fact that 20 years ago shrinkage simply entailed shrinkage. However, excessive leakage (short channel effects, etc.) in logic devices brought an end to this Dennard scaling at approximately the 130 nm node (launched in 2001, at which time copper interconnects and low-k dielectrics were already mainstream). Progressing beyond 130 nm required the introduction of strain engineering, high-k metal gate stacks, and movement to 3-D structures.

The increased number of mask steps arises from the increased process complexity discussed above, and the fact that ArF lithography (193 nm wavelength) has been used throughout the 90 to 14 nm logic nodes, with the latter being well beyond the dry ArF lithography diffraction limit. Surpassing this limit has required the introduction of new approaches, such as immersion lithography (193*i*), phase shift masks (PSM), optical proximity correction (OPC), litho-etch-litho-etch (LELE) techniques, self-aligned double patterning (SADP), and so on. Moving to 7 nm without the use of extreme ultraviolet (EUV) lithography will likely require the extension of LELE, that is, LELELELE, implementation of self-aligned quadruple patterning (SAQP), and so on. These processes have driven the number of mask steps from ~50 steps for the 28 nm node when using OPC, PSM, 193*i*, etc., to ~66 steps for 14 nm when using OPC, 193*i*, PSM, SADP, etc., to an expected ~80 steps for the 7 nm node if not using EUV.

Tighter process control drives the need for additional metrology and more stringent control of contamination/particles. In this vein, airborne particle sizes have not changed over the last 20 years, which implies that their impact should increase in a quadratic fashion with each subsequent node. In addition, smaller particles are having a greater impact.

The scope of FA labs can encompass everything from the chemical analysis of incoming chemicals, qualification/matching of process tools/recipes/environment, to the evaluation of the root cause of electrical issues noted at the unfinished die through to the shipped package level. As with HVM, the FA labs have had to derive new analytical solutions to the questions raised on moving

(continued on page 45)

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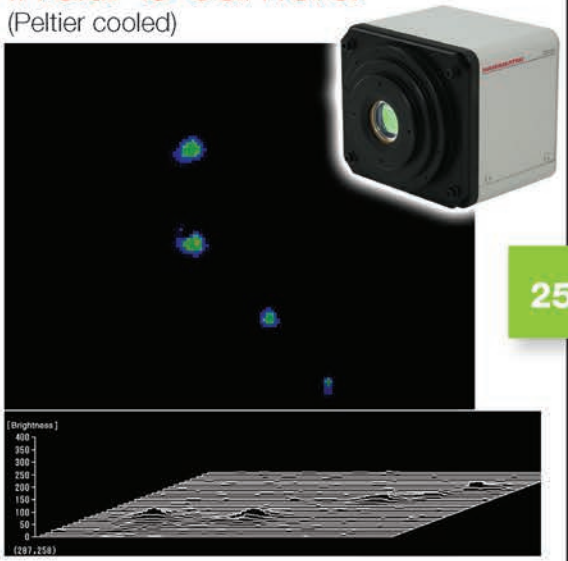

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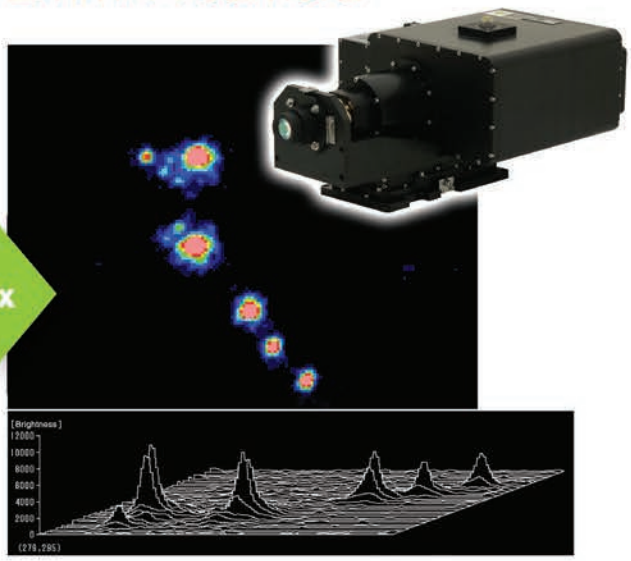

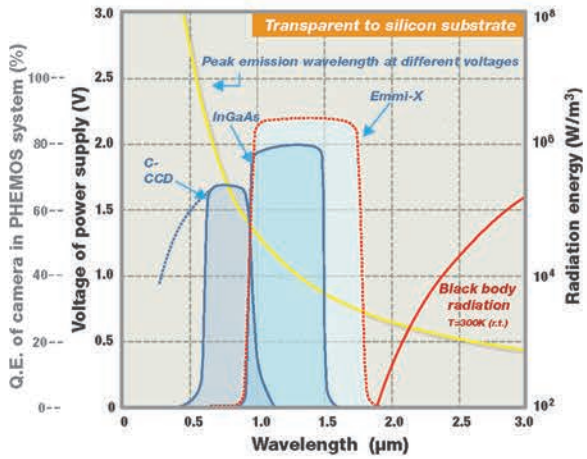

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LVI AND LVP APPLICATIONS IN IN-LINE SCAN CHAIN FAILURE ANALYSIS

Zhigang Song and Laura Safran, Globalfoundries
zhigang.song@globalfoundries.com

Laser voltage imaging (LVI) has the unique capability of mapping the periodic signal in a device under test (DUT). It is very suitable for scan chain diagnosis because data propagation through the scan chain is clocked with a periodic signal. Thus, LVI can easily identify the broken point for a scan chain failure, whether its defect is in the data path or in the clock path. Laser voltage probing (LVP) involves acquiring the waveform in a time domain from a particular point, such as the signal broken point identified by LVI, and a reference point. This can further confirm the failure and help with understanding the failure signature. This article discusses combining these two techniques in an in-line scan chain logic macro diagnosis, which has greatly improved the failure analysis success rate.

INTRODUCTION

Historically, static random access memory (SRAM) yields have been the only qualification metrics during technology development, and consequently, failure analysis of SRAM is the main feedback for process improvement and yield learning.[1,2] This is because the high density and small feature size of SRAM make its yield very sensitive to process variation, and the failing bit cells can be precisely localized for physical failure analysis. As microelectronic technology progresses in the nanometer realm, logic circuits and structures are also becoming dense and sensitive to process variation. Logic failures may also have root causes different from SRAM failure. If these technology weak points for logic circuits are not detected and resolved during the technology development stage, they will greatly affect the product manufacturing yield ramp, leading to longer design time to market. Moreover, analysis of logic failure in the product is much more difficult and time-consuming, involving tester-based fault isolation[3,4] and software-based scan diagnosis.[5,6] Thus, it is very important to have an in-line scan chain logic macro implemented for early detection of the logic circuit weak points during technology development. Furthermore,

"THE COMBINATION OF LVI AND LVP APPLICATION IN SCAN CHAIN DIAGNOSIS HAS IMPROVED THE IN-LINE SCAN CHAIN LOGIC FAILURE ANALYSIS SUCCESS RATE TO THAT OF SRAM FAILURE ANALYSIS."

LVI's unique capability to map the periodic signal[7-9] in a DUT makes it a great diagnostic technique for scan chain failure, whether the scan chain failure is due to a clock issue or an issue with the latch itself. In addition, LVP probing[10-13] can further confirm the failure identified by LVI. The combination of LVI and LVP application in scan chain diagnosis has improved the in-line scan chain logic failure analysis success rate to that of SRAM failure analysis. This article reviews the LVI and LVP technique principles and their unique capabilities, then describes an in-line scan chain logic macro, and finally presents three case studies of LVI and LVP applications in in-line scan chain failure analysis.

LVI AND LVP TECHNIQUE REVIEW

Laser voltage probing[10-13] employs a near-infrared laser beam shining on the transistor active area through

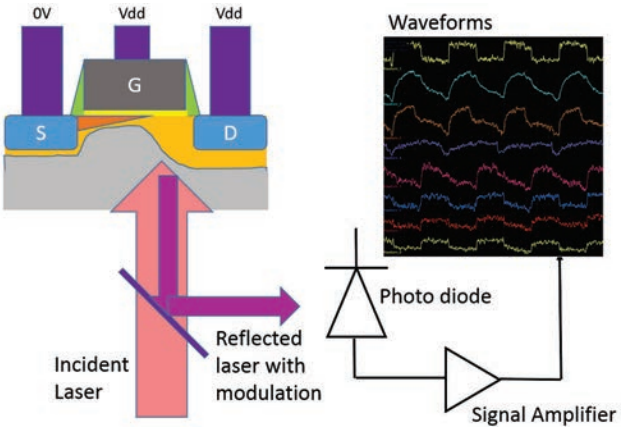

Fig. 1 LVP schematic

the silicon backside while the DUT is exercised. The laser beam reflects from the interface between the backside silicon and the active regions, such as drain and channel. The reflected laser beam has a modulated amplitude and phase. Because the modulated amplitude is dependent on the transistor state, namely the electrical field in the drain area and/or the free carrier density in the channel, extraction of the modulated amplitude of the reflected laser beam indicates the states of the transistor, on which the laser beam is focused. Figure 1 is a simplified LVP schematic. Initially, the application of LVP was mainly in design debug and device characterization, rather than fault isolation. This is because the waveforms obtained with LVP at any given time come from a particular point, namely one transistor or one node. To search for a defective transistor or node, it is necessary to probe each transistor or node one by one. It is time-consuming.

Rather than acquiring data at a single point on a DUT in the time domain, LVI[7-9] collects data in the frequency domain from numerous points in the field of view on a DUT. The LVI technique rasters a laser beam across an area of a DUT through the backside silicon. At each point, the reflected laser beam is modulated in both amplitude and phase at the switching frequency of the transistor under the area on which the laser is focused. The modulated reflected laser beam shoots on a photodetector with transimpedance and radio-frequency amplifiers, and then a modulated electrical signal is generated. After spectrum analysis, a signal with a particular frequency is generated. The signal synchronizes with the laser scan and forms an LVI image, overlapping with a normal optical image of the laser scanning area. Figure 2 is an example of an LVI image, showing the data and clock signals. Because LVI collects data in the frequency domain, it is necessary to map the transistor switching at a particular frequency. It is convenient to run the clock and data at different frequencies so that both the clock and data paths in the scan chain can be individually and simultaneously traced. Thus, it quickly became a powerful fault isolation technique for scan chain failures. With subsequent LVP, the defect for a scan chain failure can be narrowed down to an inverter or a node.

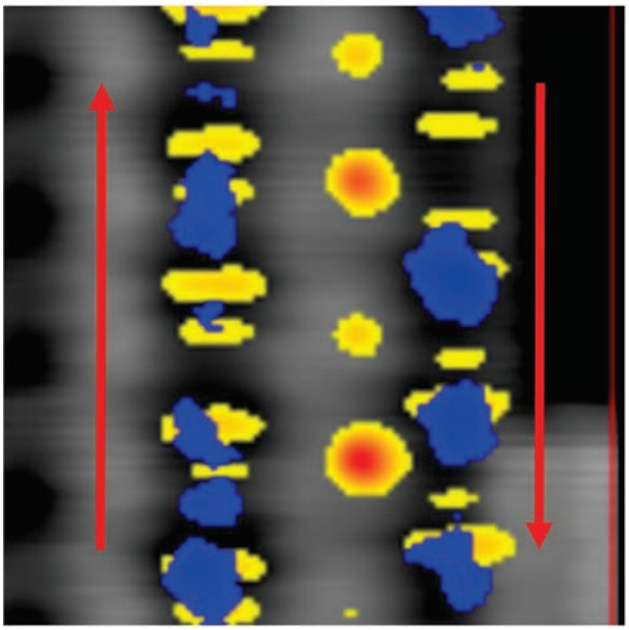

Fig. 2 **Example of LVI image for a scan chain: blue for data signal, yellow for clock signal, and red arrows for data propagation direction**

IN-LINE SCAN CHAIN LOGIC MACRO DESCRIPTION

The in-line scan chain logic macro can first be tested at metal-4 layer for early yield learning. It is comprised of several scan chains organized in 16 blocks. Each block has six packs, and each pack has six scan chains, which share the same clock buffer and preload data buffer (Fig. 3). Each scan chain group/block is composed of a different type of level-sensitive scan design and general scan

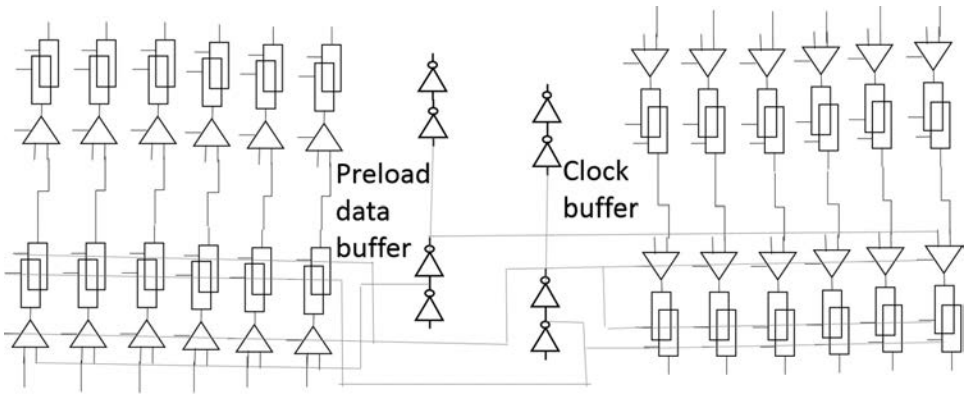

Fig. 3 **Diagram of scan chains in a pack showing the latches at the same position for six scan chains in a pack that share the same preload data buffer and clock buffer**

design latch. Most latches are representative of the ones used in product logic. The length of the scan chains/blocks varies according to the size of a given latch type. The smallest group of latches that can be tested independently is a pack, when all but one pack are skipped across all blocks with the help of a skip test scan chain. Between subsequent latches, a mux-2 circuit is implemented to enable two modes: serial scan, where data are fed from the previous latch, and preload mode, where data are preloaded from a buffer.

The in-line scan chain logic macro can be operated in three different modes: flush, scan, or preload. The first two modes are used to test the functionality of the macro. In the flush mode, all clocks are kept high, and serial data ripple through the latches from the scan input pins to the scan output pins. For the scan mode, the serial data are scanned through the latches by clocking the latches' master and slave clocks.

The preload mode is used to electrically identify the failing latch in the event of a failure during the flush/scan mode operations, that is, when the data observed on the scan output pins do not match the expected data based on the pattern exercised on the scan input pins. In the preload mode, data are loaded simultaneously in all latches through the mux-2 circuit according to two possible sequences of 0101… or 1010…, respectively. These are referred to as checkerboard and reverse checkerboard patterns. As an example, in Fig. 4 the chain has a total of eight latches. The preloaded checkerboard pattern was "01010101," and the observed scan-out pattern was "00000101." After comparing these two patterns, the first suspected failing latch was found to be latch No. 5 from the scan-out pin. However, when the reverse checkerboard pattern "10101010" was preloaded, the observed scan-out pattern was "00000010." It suggested that the first failing latch was latch No. 4 from the scan-out pin, and latch No. 4 with a stuck-at-0 fault also explained the observed scan-out pattern in the checkerboard preload test. With the checkerboard and reverse checkerboard tests, the first failing latch was identified to be latch No. 4 from the scan-out pin. In summary, the first failing latch is identified as the closest failing latch from the output pins of both complementary checkerboard and reverse checkerboard patterns.

The aforementioned latch callout identification procedure can be simplified with graphical display, which has been described in detail in Ref 14. Figure 5(a) shows an example of a single-latch failure, while Fig. 5(b) shows a clock-type failure. In Fig. 5, a white pixel indicates the measured data matches the expected data, while a dark pixel indicates the measured data do not match the expected data. The first datum scanning out from the scan chain is displayed at the extreme left. The first dark pixel counting from the left, whether in a checkerboard row or a reverse

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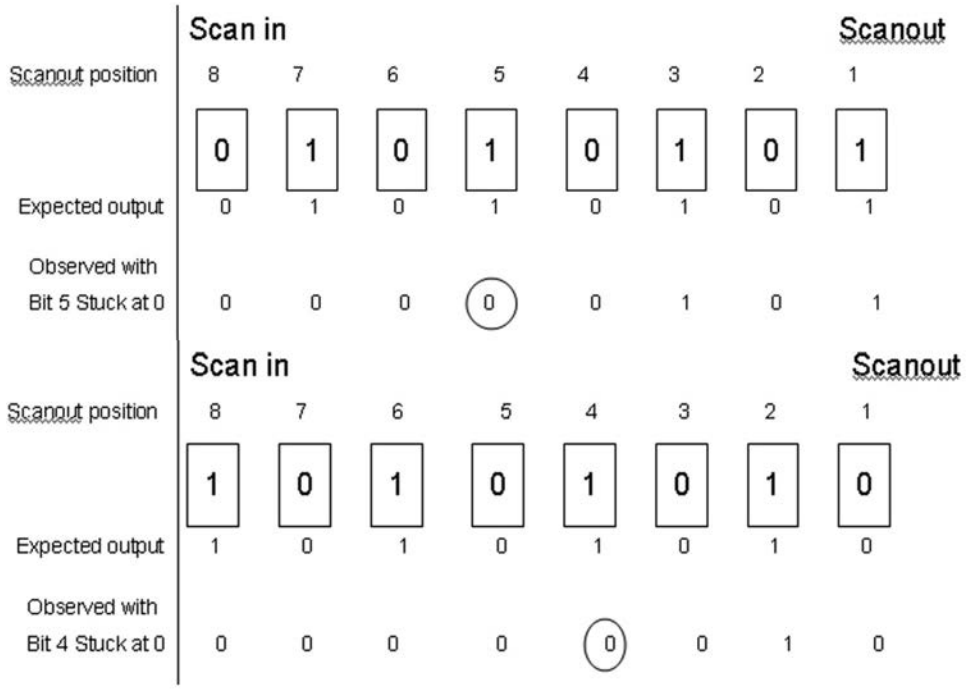

Fig. 4 **Example of eight-latch scan chain with latch No. 4 stuck at 0 identified by checkerboard pattern (top) and reverse checkerboard pattern (bottom) preload tests**

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LVI AND LVP APPLICATIONS IN IN-LINE SCAN CHAIN FAILURE ANALYSIS *(continued from page 6)*

checkerboard row, pinpoints the latch callout (Fig. 5a). In Fig. 5(b), the six scan chains in a pack are failing at the same latch position, indicating a clock-type failure.

CASE STUDIES

Because the in-line scan chain logic macro is diagnosable and single-latch fallout can be identified based on the preload test, a hard single-latch failure may be successfully analyzed with routine physical failure analysis (PFA) using top-down scanning electron microscopy (SEM) inspection. However, as defined previously, the root cause of a clock-type failure could be any failure in the buffers and the interconnects of the preload data and clock lines, or a bridging fault in the preload data and clock input circuits in any individual latches. This involves a large area. Clearly, it is more challenging to perform PFA on a clock-type failure. Thus, for clock-type failures, LVI and LVP diagnoses are necessary for localizing the failure to a small area prior to PFA. In addition, for soft single-latch failures, although the possible defective area is the same as for hard single-latch failures, the defect causing a soft single-latch failure is much smaller and more subtle. Due to the subtle nature of the defect and the large number of transistors (as many as 50 per latch) that must be inspected, the success rate with routine PFA for soft single-latch failures is very low.

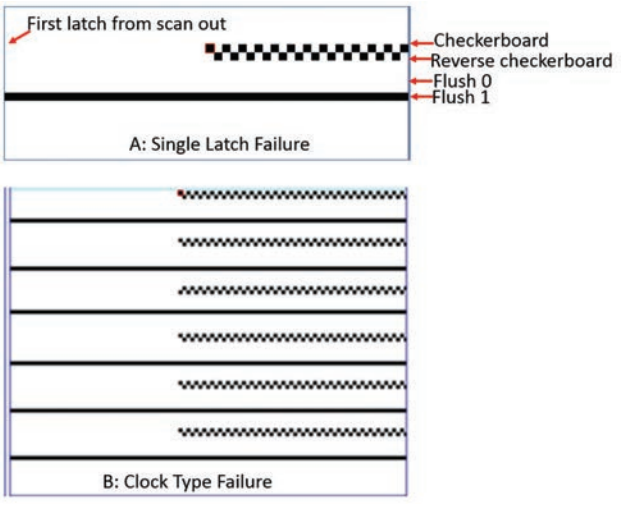

Fig. 5 Examples of (a) single-latch and (b) clock-type failures

With the help of LVI and LVP, the success rate has been improved to approximately 85%. This section describes three cases that demonstrate how to apply LVI and LVP in diagnosing scan chain clock-type failures and soft single-latch failures. The root causes of these failures were found by subsequent PFA.

SKIP TEST SCAN CHAIN FAILURE

As previously mentioned, the in-line scan chain logic macro has been divided into 16 blocks, with different latch types or layout variations in each block. A skip test scan chain is implemented to enable each block to be tested individually. Before testing the 16 blocks of main scan chains, a skip test is performed to check the integrity of the skip test scan chain. In the first case study, a chip suffered from skip test failure. First, LVI was performed with the skip test scan chain under flush test, and the LVI image showed that the data could pass through the skip test scan chain successfully (Fig. 6a). However, the data signal stopped at the sixth latch, aligning with the last pack of block 1, when the skip test scan chain was run under clock mode test (Fig. 6b). This implied that the skip test scan chain failure was due to a clock signal issue. Both L clock and D clock signals were mapped with LVI, and it was found that the L clock signal propagation was fine, while the D clock

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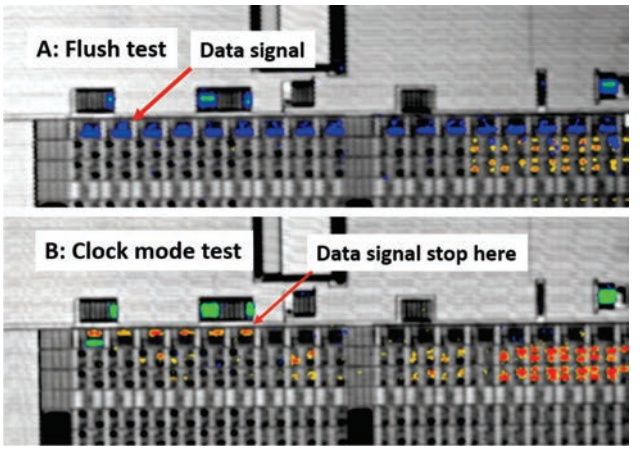


Fig. 6 LVI image for the skip test scan chain. (a) Flush test. (b) Clock mode test

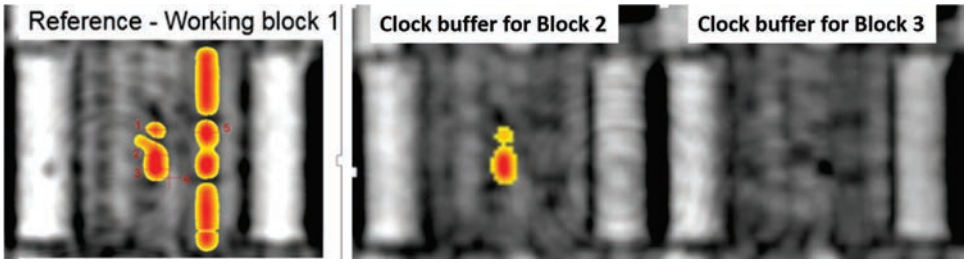
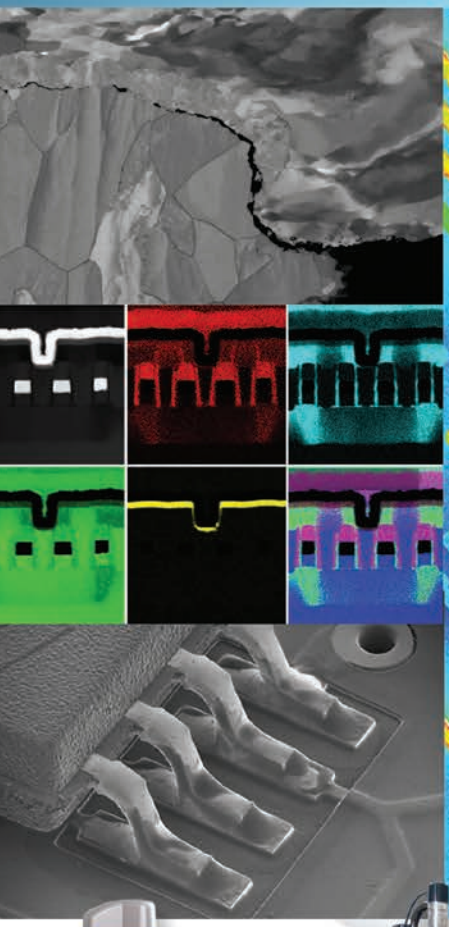


Fig. 7 LVI images at the clock buffers (D clock) for block 1 (reference), block 2, and block 3

WHEN FA = FAST ANSWERS FOR FAILURE ANALYSIS



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LVI AND LVP APPLICATIONS IN IN-LINE SCAN CHAIN FAILURE ANALYSIS

(continued from page 8)

signal propagation was broken (Fig. 7). Further comparison of the LVI signals from the clock buffers for blocks 1, 2, and 3 showed that many LVI signals were missing from the clock buffer for block 2, compared to those from the clock buffer for block 1, and no LVI signal came out from the clock buffer for block 3. This indicated that the D clock signal was supposed to propagate from the clock buffer for block 1, to the clock buffer for block 2, to the clock buffer for block 3, and so on; however, it stopped at the clock buffer for block 2. With layout tracing, it was found that there are several cascaded inverters for each clock buffer (Fig. 8). Laser voltage probing was employed to collect the waveform from each inverter. The waveforms shown at the right in Fig. 8 were collected from five points. Waveform 1 was from inverter 1, and waveforms 2 and 3 were from inverter 2 because of a long inverter. Waveforms 4 and 5 were from inverters 3 and 4, respectively. It clearly showed that the clock signal got stuck starting at inverter 3. The subsequent PFA showed a short between the source/drain contact and the gate contact at inverter 3, leading to a malfunction of this inverter, which was responsible for the skip test scan chain failure (Fig. 9).

SCAN CHAIN CLOCK-TYPE FAILURE

The second case study is a clock-type failure for a main scan chain pack, namely the same latch callout for

(continued on page 12)

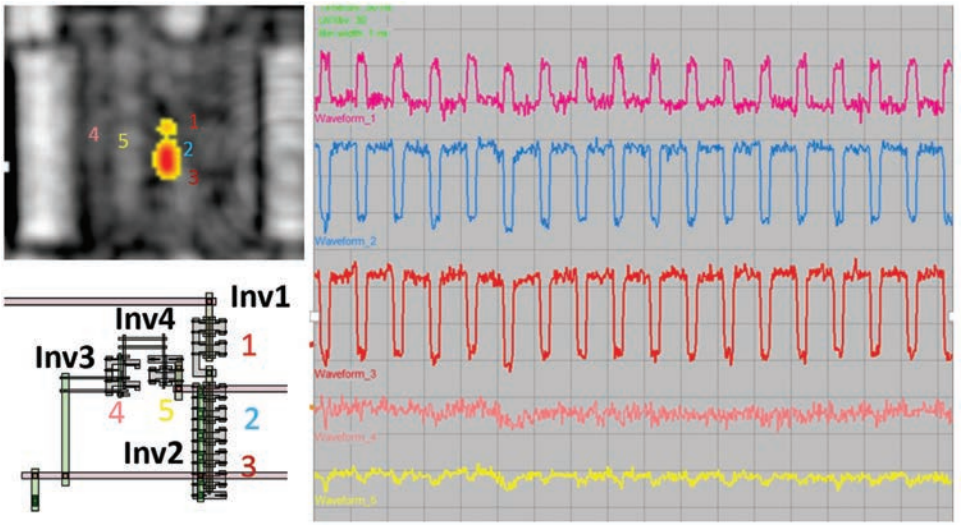

Fig. 8 **LVP waveforms collected from five points marked in the layout clip of the cascaded inverters**

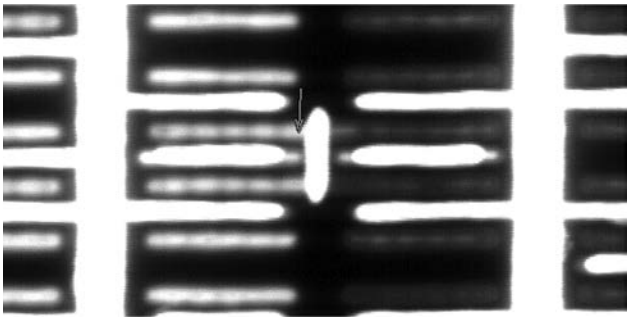

Fig. 9 **SEM image showing a short between the source/drain contact and the gate contact at inverter 3**

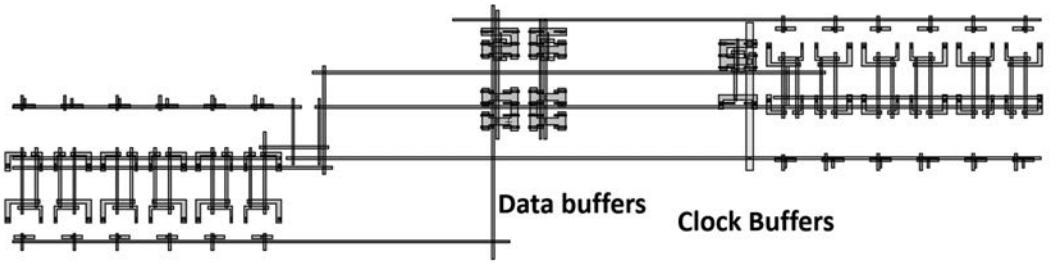

Fig. 10 **Layout tracing that shows these latches at the same position in different scan chains in a pack are sharing the same clock buffer and data buffer**

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LVI AND LVP APPLICATIONS IN IN-LINE SCAN CHAIN FAILURE ANALYSIS *(continued from page 10)*

all six scan chains in the same pack. These six latches are clocked by the same clock buffer and also are loaded by the same data buffer during preload mode (Fig. 10). The chip was subject to LVI analysis. The LVI image, shown in Fig. 11 with the clock signal in yellow and the data signal in blue, revealed that the data signal stopped at the latch callout. Figure 12 is a higher-magnification LVI image at the latch callout. It further showed that the clock signal is very weak in the latch callout. However, the clock signal in the clock buffer is still very strong. Furthermore, the latches close to the clock buffer have some data signal, while the latches far from the clock buffer do not have any data signal passing through. This implied that the signal became degraded between the clock buffer and the latch callout. Laser voltage probing was employed to check the clock signal in the latch callout (Fig. 13). Comparing the waveform from point 1 to the waveforms from points 2, 3, and 4, it was clearly seen that the waveforms at points 2, 3, and 4 were degraded. Based on layout tracing, the suspected defect was believed to be a highly resistant via in the interconnect from the clock buffer to the input of the latch callout. A subsequent focused ion beam (FIB) cross section on the suspected highly resistant via found a hollow V2 (Fig. 14).

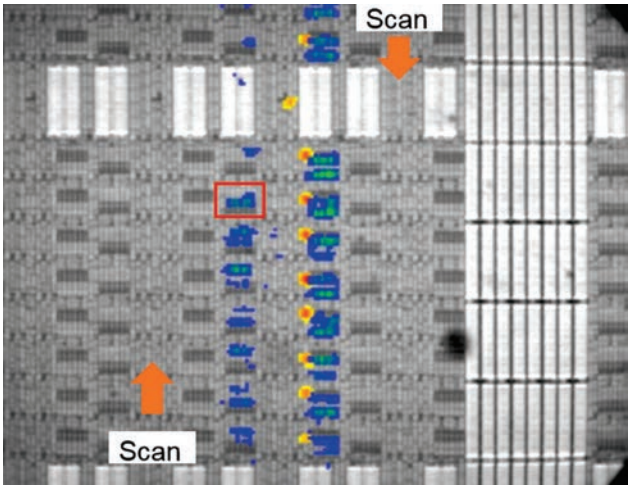

Fig. 11 **LVI image of the six scan chains with clock-type failure in a pack. The red square indicates the latch callout position.**

SCAN CHAIN SINGLE-LATCH SOFT FAILURE

The third case study is a scan chain single-latch soft failure. The latch passed at high voltage but failed at low voltage. Although routine PFA on a scan chain single-latch hard failure can find a defect in most cases, a soft failure

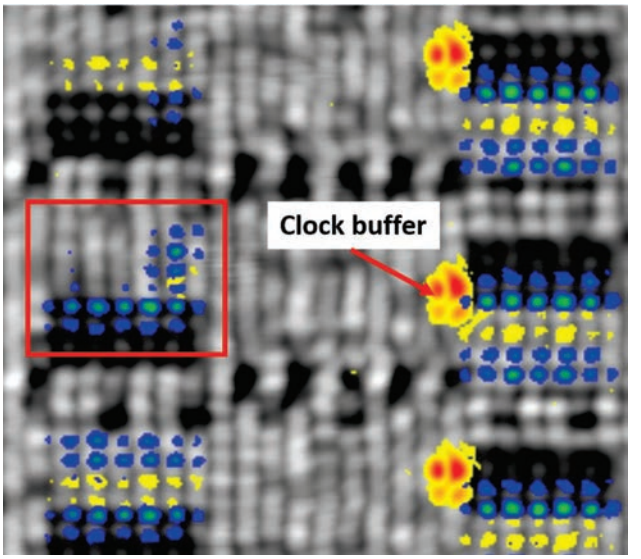

Fig. 12 **Magnified LVI image of Fig. 11 shows a strong clock signal at the clock buffer and some data signals for the latches close to the clock buffer, and no data signals for the latches far from the clock buffer.**

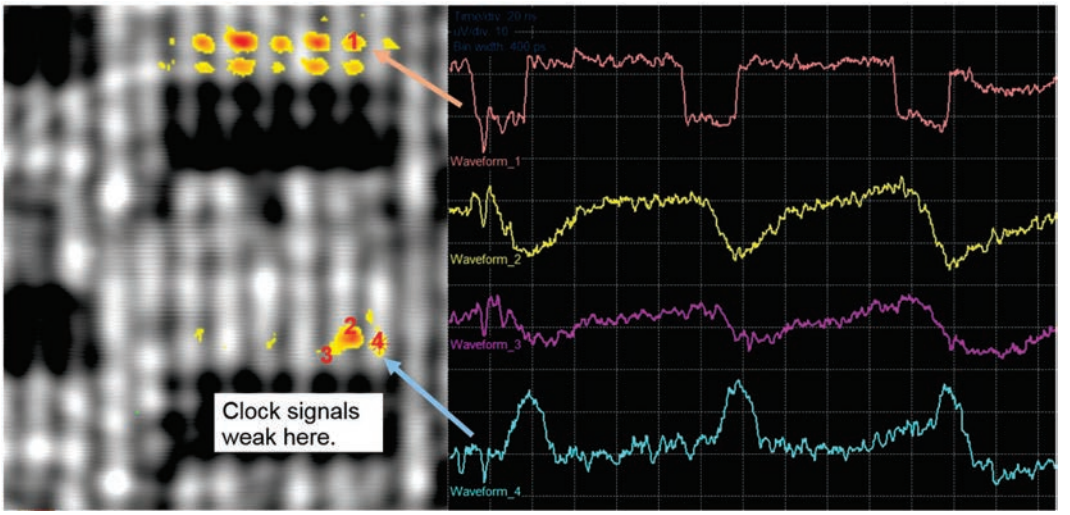

Fig. 13 **LVP waveforms of the input clock circuitry inside the latch callout show a weak clock signal compared to the one from the reference latch.**

is usually caused by a very subtle defect that may be very difficult to find. To maintain a high PFA success rate for soft failures, fault isolation is often performed prior to destructive PFA. In this case, LVI and LVP were again employed for the fault isolation. The LVI image of the clock signal and the data signal for a reference scan chain, SO3, and the failing scan chain, SO5, is shown in Fig. 15. It shows that the clock signal (in yellow) appears to be acceptable in both scan chains, while the data signal (in blue) stops at the latch callout for SO5 and continues to propagate for

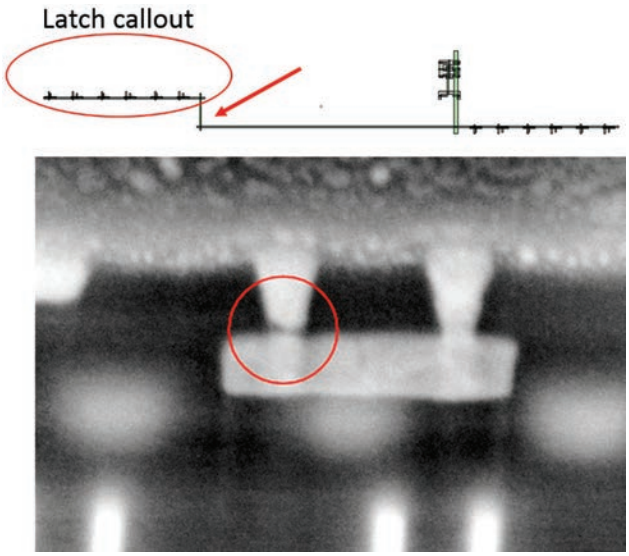

Fig. 14 FIB cross section showing hollow V2 in the clock signal line from the clock buffer to the latch callout

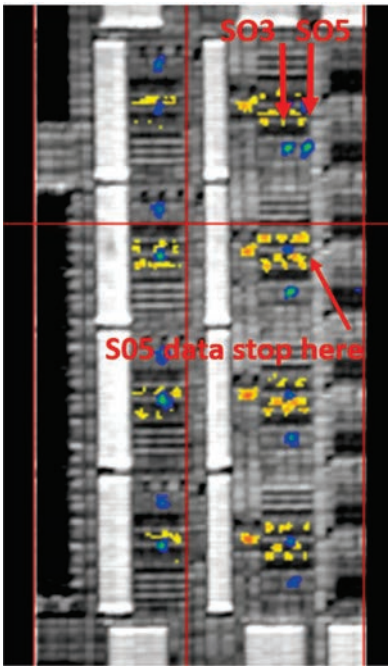

Fig. 15 LVI image of data signal and clock signal for a reference scan chain, SO3, and the failing scan chain, SO5, indicating a broken point at the latch callout for the failing scan chain, SO5

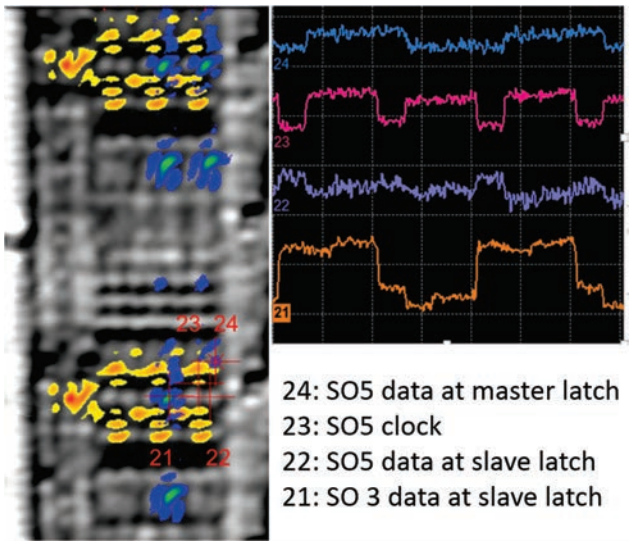

Fig. 16 LVP waveforms from the master latch of the latch callout, the slave latch from the latch callout, and the adjacent reference latch, indicating data missing at the slave latch for the latch callout

SO3. The higher-resolution LVI image (Fig. 16) from the feeding latch and the latch callout showed that the data actually had propagated to the master latch of the latch callout but had not transferred to the slave latch. This was further verified with LVP waveforms collected from the master and slave latches, as shown at the right in Fig. 16. The subsequent PFA found a gate-to-source-resistant short defect, which was responsible for the scan chain single-latch soft failure.

SUMMARY

The unique capability of LVI to map periodic signal propagation makes it very useful in scan chain diagnosis. For scan chain clock-type failures or single-latch soft failures, routine PFA with top-down SEM inspection often found no defect. Laser voltage imaging can clearly show the broken point of the clock signal or data signal for these failures. Follow-up LVP probing can further confirm the failing nodes and help explain the failure signature. Employing LVI and LVP in the diagnostic analysis greatly improves the in-line scan chain logic macro failure analysis success rate.

ACKNOWLEDGMENTS

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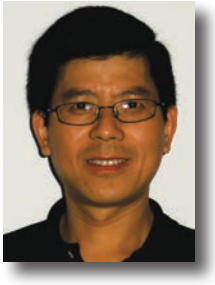
ABOUT THE AUTHORS



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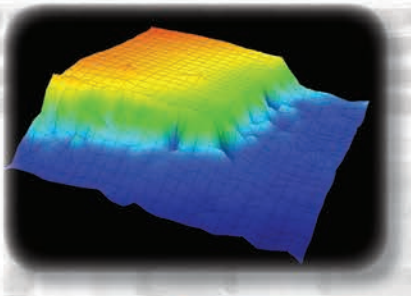

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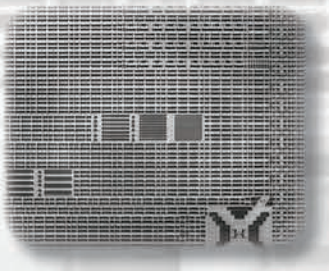

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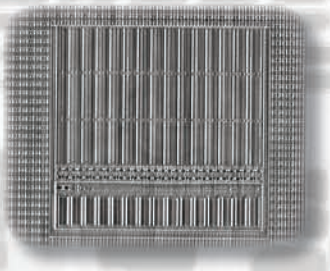

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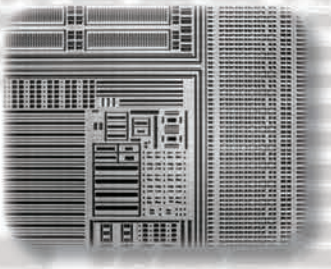

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SUPERCONDUCTING SINGLE-PHOTON DETECTOR ENABLES TIME-RESOLVED EMISSION TESTING OF LOW-VOLTAGE SCALED ICs

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TIME-RESOLVED OPTICAL PROBING OF SIGNALS ON SCALED ICs

Notwithstanding the continuous advances in design-for-manufacturing and design-for-test features, the use of noninvasive optical techniques for probing waveforms from internal nodes of integrated circuits (ICs) remains very important for the fast and accurate localization of failures.

Currently, laser voltage probing (LVP)[1] is the most commonly used time-resolved technique. A continuous-wave laser beam is focused through a high-numerical-aperture (NA) optical system to a specific transistor. When a voltage waveform is applied across the transistor under test, there is a change in free-carrier density that alters the local refractive index and the silicon absorbance, thus giving rise to a modulation in the reflected laser light.

"LUCKILY, NOVEL PHOTODETECTORS SUCH AS THE SUPERCONDUCTING SINGLE-PHOTON DETECTOR (SSPD) THAT HAVE BECOME AVAILABLE IN RECENT YEARS HAVE HELPED RETURN THE LIGHT TO THE TRE TECHNIQUE, DUE TO LOWER NOISE (FEW DARK COUNTS PER SECOND) AND BETTER JITTER."

The small modulation in the light reflected from the structure is detected by a fast photodiode (Fig. 1a). This method is extremely sensitive and has only a modest

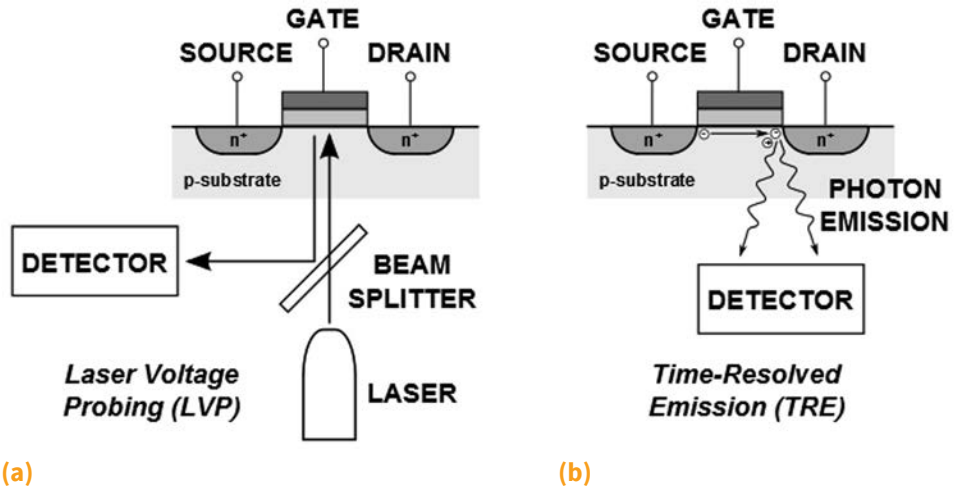

Fig. 1 **Comparison of the two main optical techniques used to detect timing-related faults within an IC. (a) In LVP, a laser is shined toward the device, and the reflected light is modulated by the carriers and detected by a detector. (b) In TRE, NIR photons are spontaneously emitted by the IC and collected by the detector.**

linear dependency on circuit voltage. However, the laser may also alter timing characteristics of the device. As device geometries shrink, the number of injected carriers required to affect the operation of the circuit also decreases, thus making it possible to cause catastrophic damage to the device. Furthermore, when multiple switching transistors lie inside the focused laser spot, the acquired signal becomes complex to interpret due to the constructive and destructive contributions. Different transistors modulate the reflected beam with different phase conditions, and so the signal is not strictly additive; in some cases, the modulation may be cancelled out almost completely through two opposing phase conditions. Usually, LVP is used in combination with a laser scanning microscope, allowing the user to test a portion of the chip (laser voltage imaging).

On the other hand, time-resolved emission (TRE),[2] also known as picosecond imaging circuit analysis (PICA), is a truly noninvasive technique, based on the collection of intrinsic near-infrared (NIR) photon emission from CMOS transistor channels (Fig. 1b). This technique allows one to detect both the logic state of the gates and the switching events (Fig. 2). Considering a digital gate, a faint but continuous emission is produced by the leakage current during off-state with the gate grounded and the drain high. No emission is produced when the transistor is in ohmic state with drain and source shorted; a short, bright emission peak is produced during a switching event, because the transistor momentarily undergoes saturation. Contrary to LVP, TRE signals are always additive, meaning that if two different devices are emitting close to each other, the resulting collected waveform will have the signals from both devices. Time-resolved emission measurement of off-state leakage[3] and carrier recombination have led to completely new applications, such as latch-up ignition,[4] power supply noise,[5] slew-rate measurement,[6] self-heating estimation,[7] variability characterization,[8] and so on. However, during the last decade, the use of TRE has been significantly limited by two critical factors: sensitivity (as a combination of detection efficiency, detector noise, and spectral coverage) and time resolution. As the chip supply voltage is reduced, the intrinsic photon emission decreases exponentially, making the use of TRE techniques challenging for low-power ICs. Luckily, novel photodetectors such as the superconducting single-photon detector (SSPD)[9] that have become available in recent years have helped return the light to the TRE technique, due to lower noise (few dark counts per second) and better jitter (approximately 30 ps full width at half-maximum). It must be noted that at the present time, TRE allows one to probe single points in a chip; however, lower acquisition times are needed with better detectors, and raster scanning can be applied to cover at least a small area of the device under test (DUT). Moreover, 2-D detectors are currently being developed, which will enable parallel acquisition.

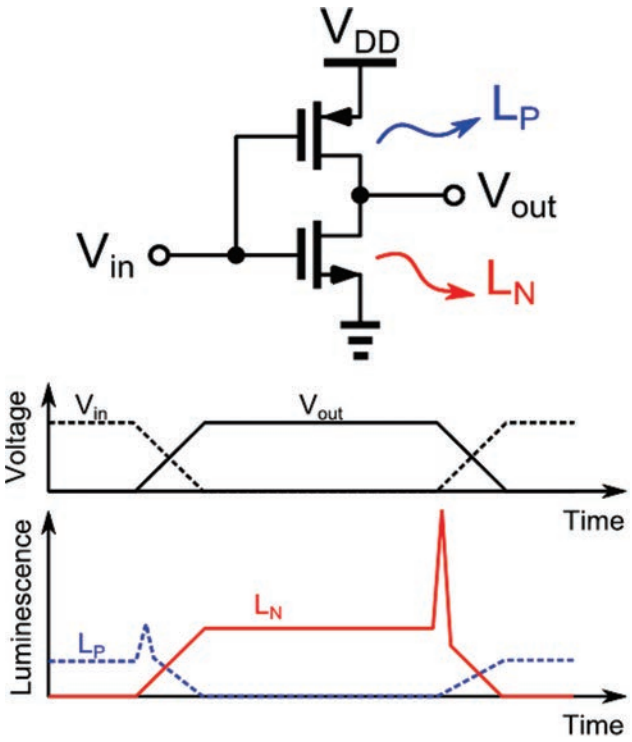

Fig. 2 **Example of luminescence signal (L) from a simple inverter gate. With TRE, it is possible to retrieve both the logic state of the gate (the gate is leaking when it is off) and when it turns on (in correspondence of the switching emission peak).**

SUPERCONDUCTING SINGLE-PHOTON DETECTOR

An SSPD is a meander made of superconducting material (in this case, NbN shaped in a 9-μm-diameter circle to match the single-mode fiber used to collect the light;

Table 1 Comparison of LVP and TRE techniques

	LVP	TRE
Invasive	Yes—may alter circuit behavior and cause damage	No—completely passive
Time resolution	~1 ns	~30 ps
Power supply dependency	Linear	Exponential

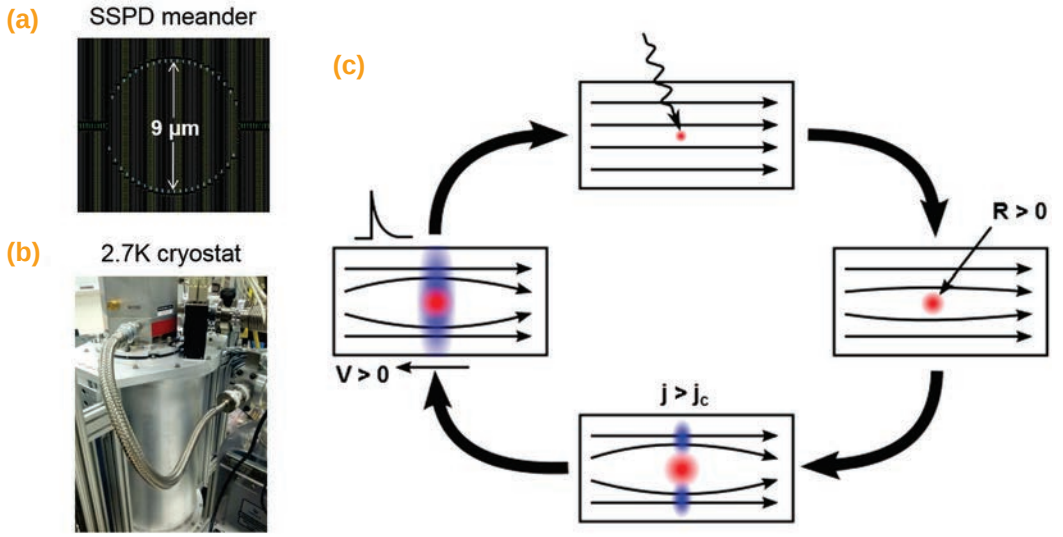

Fig. 3 **(a) NbN meander, shaped in a 9-µm-diameter circle, that was used for this work.[10] (b) Three-stage closed-cycle cryostat that houses the SSPD.[10] (c) Working principle of the SSPD. The detector is biased at a constant current lower than the critical current. When a photon hits the nanowire, a hotspot is created. The current crowds at the edges, and when it becomes higher than the critical current value, the superconductivity is lost, leading to a voltage pulse that can be detected by external electronics.**

Fig. 3a) that is kept below the superconducting critical temperature of a few degrees Kelvin by using a closed-cycle cryostat (Fig. 3b). The detector is biased at a constant current. When a photon hits the meander, it creates a hot spot (Fig. 3c, top) that makes the current crowd toward the remaining portion of the nanowire (Fig. 3c, right), causing it to exceed the critical current density value, j_c (Fig. 3c, bottom). At this point, the meander superconductivity is broken (i.e., it becomes resistive), and a voltage pulse across the SSPD (Fig. 3c, left) can be detected by the front-end electronics. After a few nanoseconds, the meander returns to superconductivity and is ready to detect a new incoming photon.

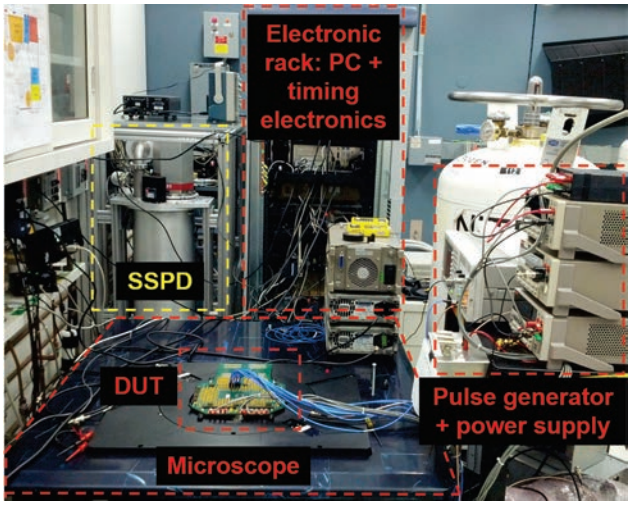

Fig. 4 **Experimental setup used to acquire TRE waveforms**

LOW-VOLTAGE SENSITIVITY

The typical experimental setup used to acquire TRE waveforms with the SSPD is shown in Fig. 4. A pulse generator provides a clock to the DUT while its spontaneous emission is collected by the high-NA solid immersion lens of a microscope and, through a single-mode fiber, is fed to the SSPD. The delay between each detected photon from the SSPD and the clock synchronization signal is measured by the timing electronics. The cumulative histogram of all the photon arrival times is used to reconstruct the TRE waveform. Note that most of the optical tools (e.g., those from FEI and Hamamatsu) can be retrofitted to perform TRE measurements. The only requirements are a fiber port to connect the SSPD as well as timing electronics to reconstruct the measured waveform.

Figure 5 shows the emission intensity measured at different chip supply voltages from an inverter gate in 32 nm silicon-on-insulator (SOI) technology using two generations of SSPD.[10] The switching emission signal is measured as the amplitude of the switching emission peak in the TRE waveform, while the noise is the standard deviation of the intensity level correspondent to the semiperiod during which the field-effect transistor (FET) is conductive. Figure 5 shows that the measurement noise is limited by the detector noise (dark-count rate, or DCR) for voltages lower than 0.65 V. The second-generation SSPD is characterized by a higher system detection efficiency; as a consequence, both the switching emission

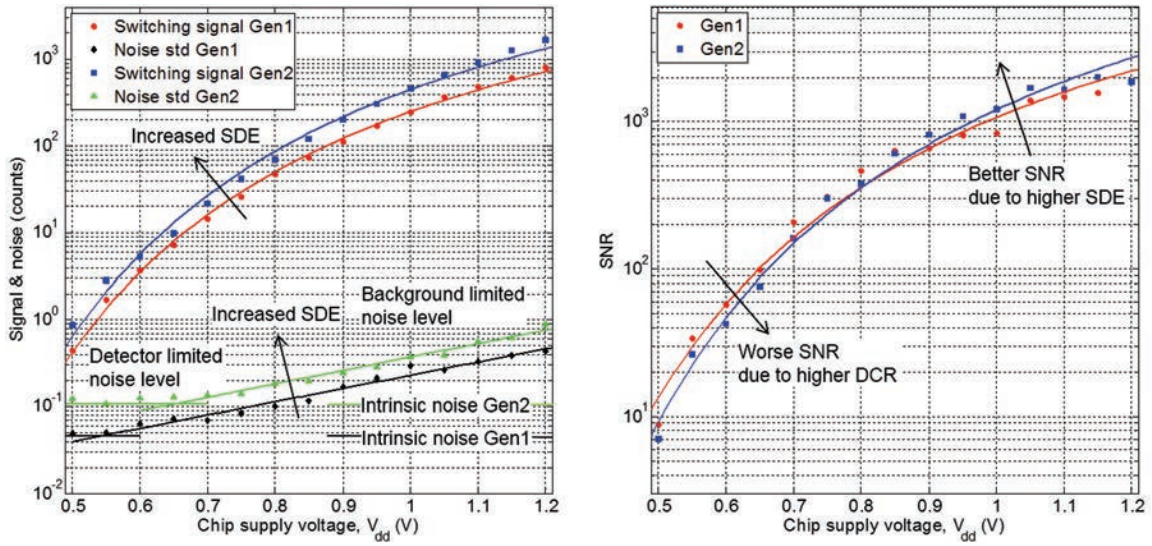

Fig. 5 **(a) Switching emission signal and noise as a function of chip supply voltage for two different generations of SSPD.[10] The noise at low voltage is limited by the detector noise, while at high voltage it is limited by the background (i.e., light coming from neighboring devices). (b) Signal-to-noise ratio (SNR) as a function of supply voltage for the two detectors.[10] SDE, system detection efficiency; DCR, dark-count rate**

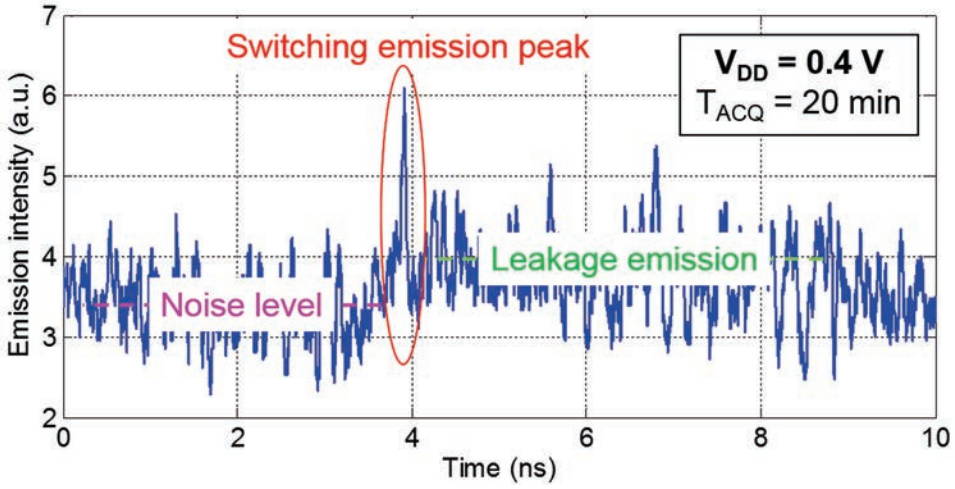

Fig. 6 **Ultra-low-voltage TRE measurement acquired from an inverter chain fabricated in IBM SOI 32 nm technology.[10] The leakage emission can be distinguished from the noise level, and the switching emission peak can be easily identified.**

signal and the noise are higher. (In fact, the measurement noise increases with voltage because some light from the neighboring FETs is collected as well.) The resulting signal-to-noise ratio (SNR) is shown in Fig. 5(b). The second-generation SSPD yields a better SNR at high voltage due to its improved detection efficiency, but it also has worse performance at low voltage due to its higher DCR.

It should be noted that the switching emission peak amplitude strongly depends on the temporal response (i.e., jitter) of the system (detector + electronics): the lower the jitter, the narrower and taller the peak. Therefore, it is crucial to optimize the SSPD front-end electronics. With careful tuning of the main system knobs that are available to the user,[11] it is possible to acquire TRE waveforms in just a few seconds at a nominal supply voltage of 0.9 V and in approximately 20 min at a world record low-supply voltage of only 0.4 V[10] (Fig. 6).

APPLICATION TO SCALED TECHNOLOGY NODES

The capabilities of TRE have been demonstrated on scaled technology nodes such as a ring oscillator fabricated in 14 nm FinFET technology. The TRE waveform acquired from one of the inverter stages is shown in Fig. 7. Each minimum-sized transistor has five fins, and the separation between *n*FET and *p*FET of each inverter is 86 nm.

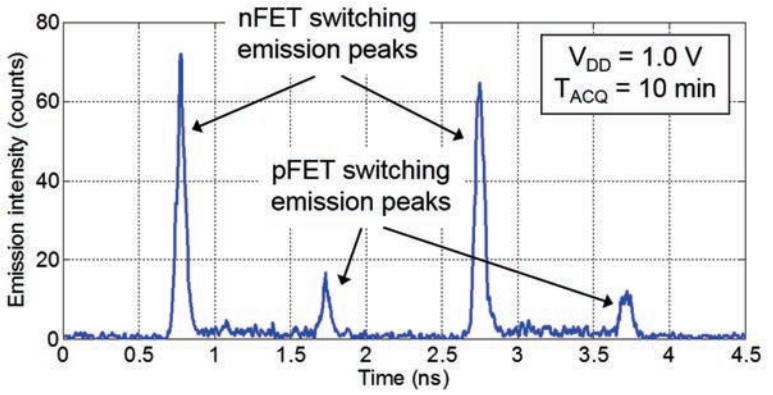

Fig. 7 TRE waveform acquired from an inverter of a 100-stage IBM 14 nm FinFET SOI ring oscillator. The light is collected from a single inverter. The switching emission peaks from both the *n*FET and *p*FET are visible.

The frequency of the ring operated at 1 V is 508 MHz, leading to a period of approximately 2 ns. Due to the scaled feature size, light can be collected from both the *n*FET and *p*FET in a single measurement, as shown in Fig. 7.

CONCLUSIONS

Notwithstanding the continuous advances of design-for-manufacturing and design-for-test features, time-resolved optical probing techniques remain an indispensable tool to increase the accuracy and speed of fault localization. Novel detectors, such as the SSPD, have become available to return light to TRE techniques that can aid or replace LVP in situations where complete noninvasiveness is necessary. The detector and the technique have been demonstrated for scaled nodes such as 14 nm FinFET SOI and for ultra-low-power supply voltages down to 0.4 V.

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(continued on page 22)

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NOTEWORTHY NEWS

ITC 2016

The International Test Conference (ITC) will be held **November 15 to 17, 2016**, at the Fort Worth Convention Center in Fort Worth, Texas. ITC is the world's premier conference dedicated to the electronic test of devices, boards, and systems and covers the complete cycle from design verification and validation, test, diagnosis, failure analysis, and back to process, yield, reliability, and design improvement. At ITC, test and design professionals can confront the challenges the industry faces and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

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3-D TECHNOLOGY: FAILURE ANALYSIS CHALLENGES

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INTRODUCTION

Chip-level three-dimensional integration, that is, 3-D stacked IC (3-D SIC), where chips are thinned, stacked on each other, and vertically interconnected using through-silicon vias (TSVs) and microbumps, promises a large improvement in performance and functionality of microelectronics systems. However, it also promises additional challenges for the failure analysis (FA) community.

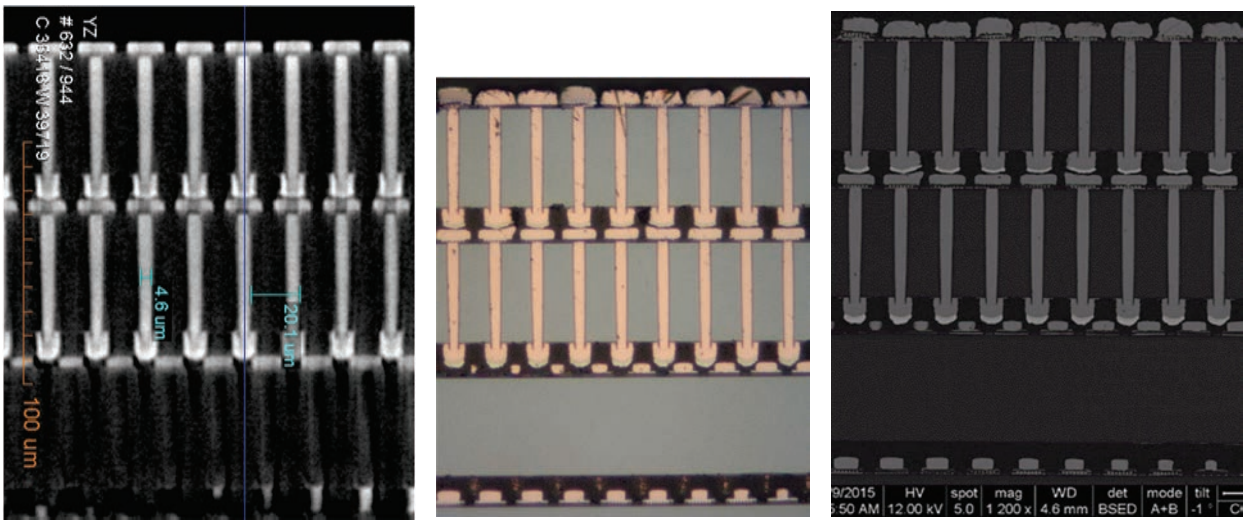
Two-dimensional chip-level FA already must deal with the challenges imposed by the high density, which reduces dimensions and increases complexity of the active devices, together with an increased number of layers in the back-end-of-line (BEOL) required to interconnect it all. The main FA solutions approach the problem from the backside of the chip, requiring appropriate thinning and probing solutions. One could happily argue that life will become easier in 3-D, because the chips are already thinned before stacking, thus reducing that barrier. This may partly be the case; however, the current 3-D chips are only thinned to typically 50 µm, which is not enough for backside probing of high-density, nanosized transistors. In addition, they are stacked rather rigidly on top of each other. Even when a failure location is electrically found to be restricted to a particular chip, removing one chip from a stack without damaging it is certainly an issue that will bring new challenges for sample-preparation specialists. In addition, the chips are electrically interconnected in a vertical manner. A failure may be somewhere on the chip, but it may also be in the interconnection between the chips, in the TSVs inside the chips, or in the microbumps. Misalignment easily leads to bad interconnections and potential failures. Breakdown of the TSV liner can cause leakage paths and copper diffusion into the silicon. Intermetallic formation can cause issues in the microbumps. Stress in the TSV can affect nearby transistors or cause damage in the BEOL layers on top. In addition to these new interconnection elements, mechanical and thermal issues will also bring additional risks for failure, especially if mechanically fragile ultra-low-k dielectrics are used in the BEOL. There is a clear need for techniques that can nondestructively locate a failure in a (packaged) 3-D stack, together with sample-preparation methods that allow easy and fast access to the failure site for further inspection.

"THERE IS A CLEAR NEED FOR TECHNIQUES THAT CAN NONDESTRUCTIVELY LOCATE A FAILURE IN A (PACKAGED) 3-D STACK, TOGETHER WITH SAMPLE-PREPARATION METHODS THAT ALLOW EASY AND FAST ACCESS TO THE FAILURE SITE FOR FURTHER INSPECTION. "

Referring to FA for 2-D chips, Dave Vallett mentioned in the October 1997 *IEEE Spectrum* that "FA is sometimes rightly compared to looking for a needle in a hay stack, and in this case, the haystack is getting larger, while the needle is getting smaller." This is still true, but when talking about 3-D IC technology, one could modify his quote to: "3-D FA is like looking for a needle in a hay barn, with the needle getting smaller and the hay barn getting ever bigger, and an increasing amount of cats and mice messing things up," with the "cats and mice" being TSVs and microbumps.

X-RAY IMAGING AND SCANNING ACOUSTIC MICROSCOPY

The most common nondestructive techniques that allow a look inside a 3-D stack of chips are x-ray imaging and scanning acoustic microscopy (SAM). These techniques are well known from package-level FA. Their main drawback for 3-D applications has been their



(a) (b) (c)

Fig. 1 **Comparison of (a) virtual cross-sectional image obtained by XRM and (b, c) optical and SEM images taken after physical cross sectioning for 20-µm-pitch TSVs (5 µm diameter) and bump joints. Images by Carl Zeiss X-Ray Microscopy, Inc.; sample from imec. Figure from Ref 3, with permission from SMTA and Chip-Scale Review**

resolution, but there are promising developments for both techniques. Recent advances in 3-D x-ray microscopy (XRM)/tomography demonstrate a submicron resolution of 0.7 µm, even down to 50 nm for special systems. However, this extreme resolution requires relatively small samples and/or a very long measurement time (several hours). Provided that the failure location is known, one could also use focused ion beam (FIB) or plasma-FIB or combined FIB-SEM or -TEM imaging, allowing slices to be made through the place of interest and providing better resolution.[1,2] However, the main advantages of x-ray are that it is nondestructive—no risk to remove a failure—and it allows in situ 3-D imaging of relatively large areas of a sample. Figure 1[3] is an example of an image of a 3-D stack, showing TSVs and microbumps. The comparison with an optical cross-sectional image and an SEM image demonstrates the very good resolution of the current x-ray microscopy systems.

Scanning acoustic microscopy requires the sample to be immersed in water, allowing ultrasound, typically in the megahertz range, to couple into it. The spatial resolution of this technique depends on the frequency: the higher the better. Unfortunately, this implies a lower penetration depth of the sound waves into the sample. For 3-D applications, the conventional systems can be used to detect and locate delamination between chips, or cracks in chips, but their resolution (at best approximately 5 µm) is too small to detect, for example, micron-sized voids in copper TSVs of microbump failures. A promising evolution is the GHz-SAM, using sound waves with 1 to 3 GHz frequency. It was demonstrated that this technique can visualize voids in TSVs,[4] but the exact resolution and sensitivity still must be verified. An advantage of this technique is that not only bulk sound waves but also surface (Rayleigh) waves can be generated, and these waves, reflecting from TSV edges or even cracks, can be visualized.[5] An example of such a fringe pattern near TSVs is shown in Fig. 2. The asymmetry is most likely related to the anisotropy of silicon. This technique may be very promising for detecting, for example, cracks or delamination near TSVs or even in the BEOL layers. However, an in-depth understanding of the

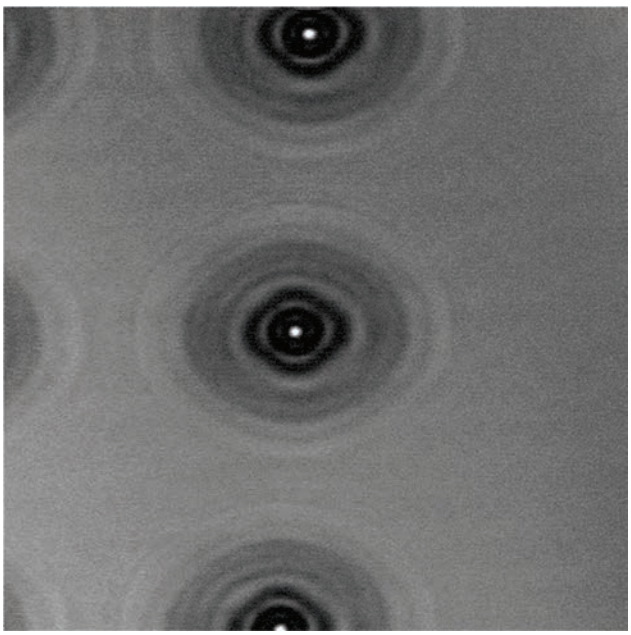


Fig. 2 **Rayleigh fringes observed near 5-µm-diameter TSVs using a GHz-SAM system. Experiments done at FhG CAM Halle, Germany; sample from imec; PVA TePla system**

application domain and the limitations of this technique is still missing and requires further testing and modeling of the interaction of sound waves with such samples.

Although currently it is not clear whether small voids inside a TSV can cause failures, it is preferable to avoid them, and, for that reason, they must be detected early in the processing sequence. As such, this is more an in-line wafer-level metrology requirement than an FA requirement. For this reason, in addition to GHz-SAM, other sound-based techniques are being investigated, such as laser-based acoustic analysis,[6] where the signals obtained from control TSVs are compared with those from TSVs with voids.

THERMOGRAPHY AND MAGNETIC CURRENT IMAGING

In addition to x-rays and sound, there are some other candidates that allow a nondestructive look inside a 3-D stack: for example, heat and magnetic fields. A defect that generates some heat can be located using an infrared (IR) camera, and, even more, its location in depth can be found using a lock-in thermography (LIT) system.[2] These systems are very sensitive, nondestructive, and can locate defective spots even through a packaged 3-D stack. However, one major drawback of LIT is the spatial resolution, inherent to the IR wavelength, which requires solid immersion lenses (SILs) to somewhat improve the resolution. In addition, the depth localization requires some knowledge of the thermal conduction of the different layers in the stack, that is, calibration and/or modeling. Nevertheless, several publications have already demonstrated various LIT applications for FA of 3-D stacks.[2] Although the depth sensitivity may not be adequate to locate the liner breakdown position along a TSV, it was recently demonstrated by researchers from FhG CAM that studying the emission intensity at different focusing depths can provide additional depth information (Fig. 3).

Magnetic current imaging (MCI), a technique that received increasing attention due to its potential applications for 3-D technology,[7] can provide a better spatial resolution (even submicron) than LIT, provided that the magnetic sensor is close enough to the current path. In this technique, the in-plane current flow in a sample is visualized by detecting the associated magnetic field. This allows, for example, the detection of shorts. A drawback is that the distance between the current path and the detector determines the resolution and sensitivity. However, both can be used to obtain some information about the location in depth. An example is given in Fig. 4, where the technique could be used to locate a short in a 3-D stack.[8] Further sample preparation was done using a plasma FIB to analyze the failure site.

It was also demonstrated that the MCI technique can locate opens. By generating a standing current wave in an open conductor, the position of the open can be located by analyzing the decay of the detected magnetic field along the conductor. As such, this technique could be a solution to nondestructively detect both opens and shorts in 3-D SIC stacks. However, further development is once again required to provide higher sensitivity and better in-plane and depth resolution. A very promising detector technology for this purpose is the one based on detection of the magnetic spin moment of single-color-center, nitrogen-vacancy lattice defects in diamond.[9] These detectors promise not only a magnetic sensitivity better than 1 pT/sqrt Hz but also a sub-10 nm spatial resolution, highly outperforming the currently used superconducting quantum interference device and giant magnetoresistance (GMR) sensors. In addition, these sensors can detect not only the out-of-plane magnetic field but all field components, and they are also sensitive to local temperature variations. This development may open the way for improved MCI on 3-D stacks and also solve some FA issues of current and future 2-D and 3-D nanotechnology.

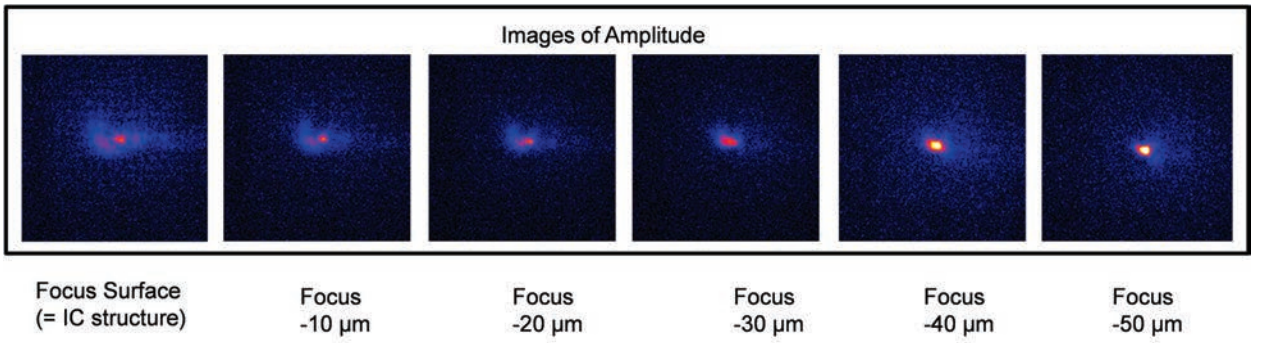


Fig. 3 **Backside LIT images with SIL taken of a breakdown spot of a 5-µm-diameter, 50-µm-deep copper TSV at different focus positions. The images clearly indicate that the breakdown is located close to the bottom of the TSV (focus −50 µm). Measurements by C. Grosse and F. Altmann, FhG CAM, Halle, Germany; sample from imec**

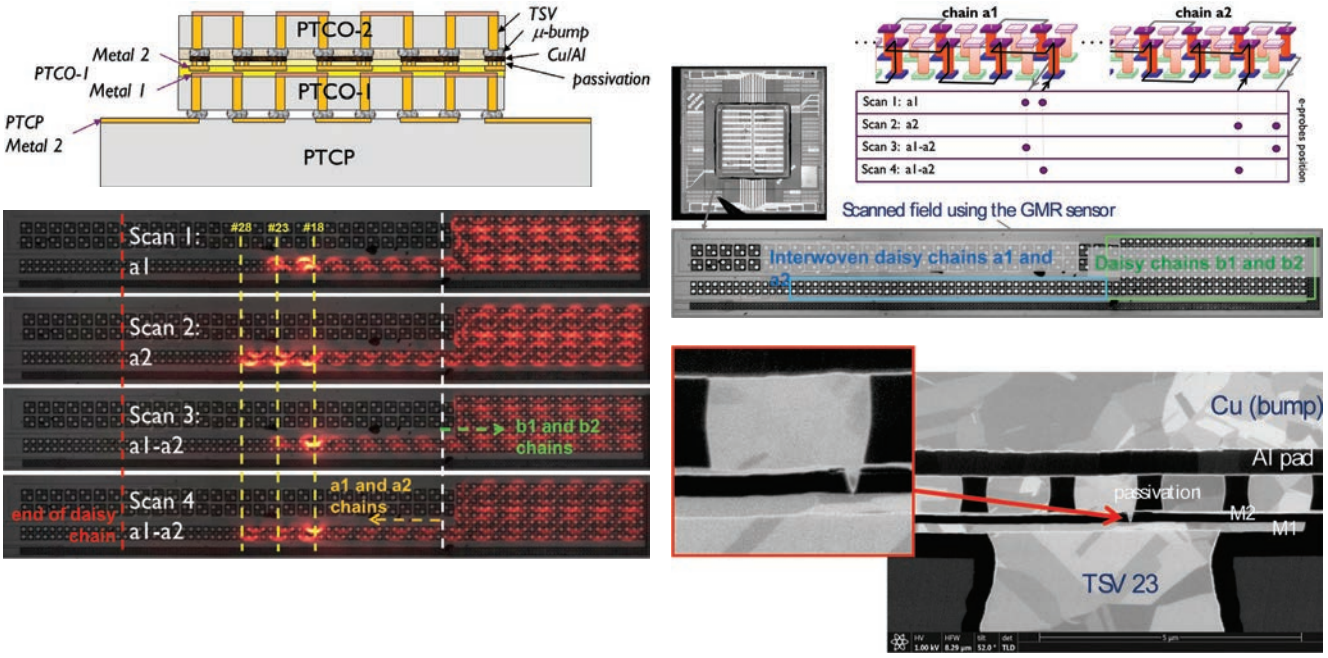


Fig. 4 **Failure analysis to find the location of a short between interwoven daisy chains a1 and a2 using magnetic field imaging (by Neocera) on a 3-D stacked IC sample (from imec) containing two thinned chips (50 µm, PTCO-1 and -2) and one thick chip (~750 µm, PTCP), interconnected by 5 × 50 µm copper TSVs and microbumps. The sample contains two interwoven daisy chains (a1 and a2) running between PTCP and PTCO-1 (metal 1). Other daisy chains (b1 and b2) run between PTCO-1 and PTCO-2 and are not connected to chain a1. MCI is performed to test chains a1 and a2 and between a1 and a2. The images indicate shorts between the chains and between chains a and b. MCI allowed the short position near TSV No. 23 to be located. Plasma FIB (by FEI) confirmed a failure short between M1 and M2 of PTCO-1 above TSV No. 23.[7]**

If a failure results in an open or short affecting the interconnections in the top chip, and if electrical access to the chips is possible, SEM-based FA techniques, combined with local probing, remain of high value. For example, electron beam absorbed-current imaging was demonstrated to locate an open in a TSV daisy chain.[2]

OPTICAL TECHNIQUES

The traditional light-based techniques can also be applied, if the light can access the region of interest in or out of a 3-D stack. A lesser-known technique, polariscopy,[5] was demonstrated to be very sensitive to local mechanical shear stress variations, as also detected near TSVs. One can expect that any defect affecting this stress, such as voids or delamination, will affect these stress fields and be detectable. Although promising, the technique is rather complicated and sensitive to sample conditions; further research and development is necessary to understand its applicability and limitations.

Time-domain reflectometry, measuring the reflected signal of a low-amplitude 35 GHz pulse applied into a conductive circuit, can be used to nondestructively detect a failure in an interconnection trace. However, this technique typically could not be used for 3-D stacks because of its limited sensitivity and resolution. New developments, using optically generated terahertz signals (electro-optical terahertz pulsed reflectometry), demonstrated that bump-level failures could be detected in 3-D stacks.[10]

It was shown several years ago that photon emission microscopy (PEM) was able to locate a liner breakdown position in a TSV.[11] If access is not possible from the top, it can be done from the cross section, in some cases. To allow close inspection of a TSV, as demonstrated in Fig. 5, an FIB can be used to open an area around it, leaving some silicon around the TSV. The PEM image is then obtained in situ by rotating the sample with the cross-sectional site up, allowing analysis of the TSV area with large magnification, and, in the meantime, probing from the sides. In this case, the breakdown was found to be near the bottom of the TSV, at the backside of the copper TSV.

However, this requires locating the leaky TSV first. One recently demonstrated solution for locating a defective TSV is the use of light-induced capacitance alteration (LICA), a type of alternative technique to optical-beam-induced resistance change, light-induced voltage alteration, or thermally-induced voltage alteration. In LICA,[12] a laser is scanned across a TSV chain while simultaneously measuring the capacitance between the chain and the

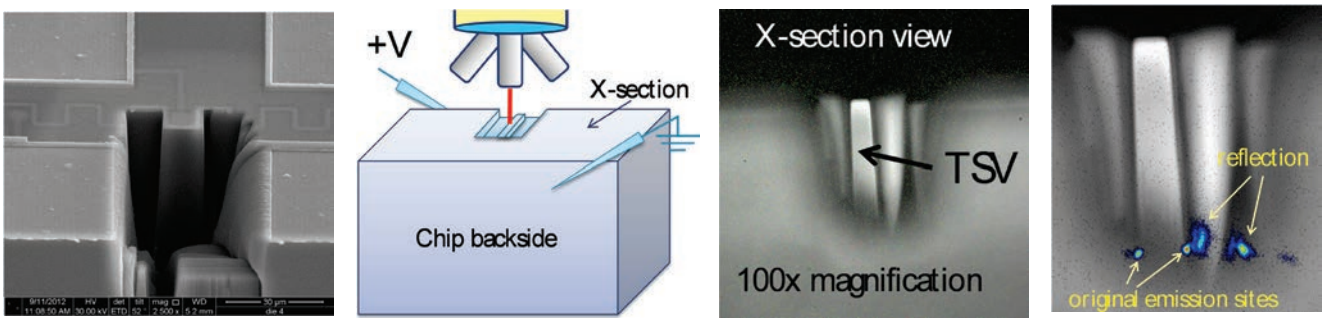


Fig. 5 In situ localization of the breakdown site of the liner of a 5-µm-diameter, 50-µm-deep copper TSV. (a) Sample prepared by cleaving and FIB, leaving silicon near the TSV. (b) Schematic showing the sample in the PEM setup and the probing from the sides. (c) Crosss-sectional microscopy image taken with the PEM setup. (d) Overlay image showing emission detected near the bottom of the TSV. Some light is reflecting from the side walls of the FIB-cut hole.

silicon substrate. Every time the silicon near a connected TSV is probed by the laser, the measured capacitance will change. When a nonconnected TSV is probed, no change will be detected. This new technique allows easy and fast localization of an open or short position at the TSV level. As with all laser-based techniques, one drawback is that optical access to the TSV region is required, which may become problematic if several chips are stacked.

CONCLUSIONS AND OUTLOOK

It is clear that although several techniques have been demonstrated to provide some solutions for FA of 3-D systems, they all have their limitations. Either they are limited to the external chips, or they lack in resolution, or they are too slow. A clever design-for-test will be necessary to partly solve this problem. In addition to further advances in FA tools, new sample-preparation solutions are also required, allowing one to singulate chips from a 3-D stack without destroying their functionality and testability. The latter requires additional probing solutions on TSVs and microbumps.

When looking to the 3-D landscape,[13] this technology is also evolving toward smaller dimensions. Some things may become easier for the failure analyst, but others will certainly become more complicated. The 3-D SIC technology, involving die stacking, die-to-wafer stacks, and die-to-silicon-interposer stacks, all interconnected through TSVs (typically 5 µm or larger in diameter), is evolving to within-die 3-D system-on-chip, involving parallel front-end-of-line (FEOL) wafer processing and wafer-to-wafer bonding, where the BEOL of the top thinned flipped wafer makes direct interconnection to the one on the bottom wafer. This involves much smaller TSVs of a few microns in height and a diameter down to 0.5 µm. Future development will bring sequential FEOL device processing, that is, transistor-level 3-D integration, also called 3-D IC. Imagine finding the failing transistor in a chip containing two or more stacked layers of highly dense nanosized transistors. This 3-D IC technology is especially promising for vertical devices, and it has already been demonstrated for 3-D NAND memory devices. It is clear that FA research and development will remain very challenging in the future.

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Ingrid De Wolf received a Ph.D. in physics from KU Leuven University, Belgium, in 1989. That same year, she joined imec in Belgium, where she worked in the field of microelectronics reliability, with special attention on gate oxide reliability, mechanical stress analysis using micro-Raman spectroscopy, and failure analysis. From 1999 to 2014, she headed the group REMO, where research focuses on reliability, testing, and modeling of 3-D technology, interconnects, MEMS, and packaging. She has authored or co-authored 14 book chapters and more than 350 publications and has won several Best Paper Awards at conferences focusing on reliability and failure analysis. Dr. De Wolf is chief scientist at imec, an IEEE senior member, and a professor in the materials engineering department at KU Leuven, where she teaches courses on nondestructive testing, MEMS reliability and failure analysis, characterization techniques, and failure mode and effects analysis.

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EMERGING TECHNIQUES FOR 2-D/2.5-D/3-D PACKAGE FAILURE ANALYSIS: EOTPR, 3-D X-RAY, AND PLASMA FIB

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INTRODUCTION

Over the past decade, semiconductor packaging technologies have increased drastically in their complexity and importance.[1] These trends, combined with on-going semiconductor technology developments toward 14 nm and below, result in complex device buildups and high failure analysis (FA) success yield requirements. To fulfill these requirements and to enable 2.5-D and 3-D product solutions, long-established package processes such as wire bonding are constantly fading while chip-scale packages (CSP) are on the rise.[2] Packaging trends such as through-silicon vias (TSVs), micropillars, and stacked-dice devices emerge more and more to become standard process applications, leading to a more compact design and higher functionality density. An example is given in Fig. 1, which shows a modern 2.5-D test vehicle including packaging technologies such as silicon interposer and micropillar interconnects.[3]

Figure 1 shows two full-wafer-thickness dice, which are stacked on a thinned silicon interposer. The dice package is finally assembled on an organic laminate. Micropillar technology is used to enable a high-density interconnection between the dice, while TSV and C4 bumps finalize the overall communication toward the environment.

"THE ENABLEMENT OF SUCH PACKAGING SOLUTIONS NOT ONLY REQUIRES NEW PROCESSES FOR TSVs, THIN-DIE MANUFACTURING, ASSEMBLY, AND TEST BUT ALSO A WELL-DEFINED CONCEPT OF PROCESS AND SUPPLY CHAIN, INCLUDING PACKAGE FA."

The enablement of such packaging solutions not only requires new processes for TSVs, thin-die manufacturing, assembly, and test but also a well-defined concept of process and supply chain, including package FA. When performing FA of these new package devices, standard fault isolation techniques such as I-V bench testing, time-domain reflectometry (TDR), or scanning acoustic

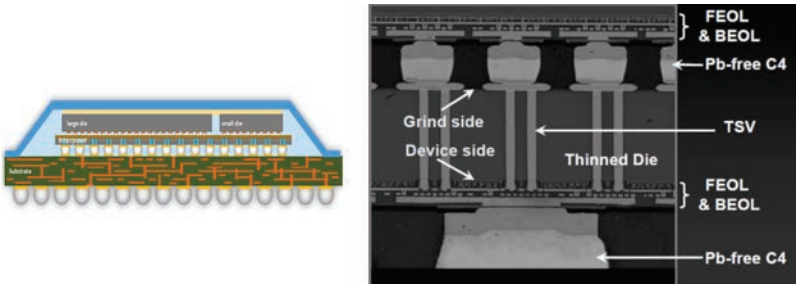


Fig. 1 (a) Example of 2.5-D integrated system-in-package based on interposer technology.[2] (b) High-magnification image of interconnection realization between full die (top), thinned die (middle), and laminate (bottom) using TSV, micropillar, and thinned-die packaging.[3]

microscopy face challenges to identify the correct defect area with the sample still fully functional. In addition, sample-preparation techniques such as mechanical cross sectioning and top-down sample delayering are reaching their limitations where preparation artifacts can no longer be neglected.

ANALYSIS OF CURRENT PACKAGE FA FLOWS, CHALLENGES, AND REQUIREMENTS

While complex packaging is desired from a product point of view, it also induces additional risks and challenges regarding manufacturing yield, device performance, and life-time reliability. Considering these facts, a new threshold of requirements for successful FA is introduced:

- Using copper as the main material for TSVs and micropillar realization induces a coefficient of thermal expansion (CTE) mismatch to silicon material. As a result, thermal and mechanical tension can lead to crack introduction.

FA request: Sample preparation is requested to avoid smearing effects during mechanical cross sectioning.

- Using thinned-die technology (e.g., interposer), especially on large package products, raises the influence of warpage and die-bowing effects. Similar to CTE mismatches, these can introduce crack propagation and layer delamination.

FA request: Handling of thin but large sample sizes; compensation for stress relaxation during sample deprocessing.

- Shrinking interconnect dimensions lead to a requirement to lower critical void size and concentration.

FA request: Artifact-free sample preparation and cross sectioning; early failure detection with shrinking defect size.

Analyzing these requirements, the need to maintain overall device functionality and therefore nondestructive testing and fault isolation becomes a priority. Furthermore, after successful defect isolation, a precise and local target-preparation method is desired that allows root-cause imaging in any layer inside the package stack. Although these requirements are not fully new to the FA industry, current state-of-the-art methods face their physical limitations:

- Optical-based methods, such as photon emission microscopy, optical beam-induced resistance change, or laser scanning microscopy, are often used for fault isolation but face limitations due to the complex package setups that block optical access for fully packaged devices.
- Confocal scanning acoustic microscopy is often used for delamination or crack detection within package products. However, due to the increasing layer and material amount combined with shrinking interconnect size, early defect detection becomes more and more difficult.
- Time-domain reflectometry is capable of isolating specifically the defect depth within the package. However, due to its pulse length in the megahertz range, it cannot keep up with the shrinking interconnect size; a *z*-resolution limit is increasingly hindering successful defect isolation.
- Mechanical cross sectioning is a state-of-the-art, fast, and effective way to achieve root-cause analysis. Within the introduction of copper-based interconnects and shrinking feature size, a shift toward focused ion beam (FIB) techniques is recognizable. As for package FA, standard FIB tools suffer from inadequate beam currents, which results in long cross-sectioning times in the tens-of-hours range.

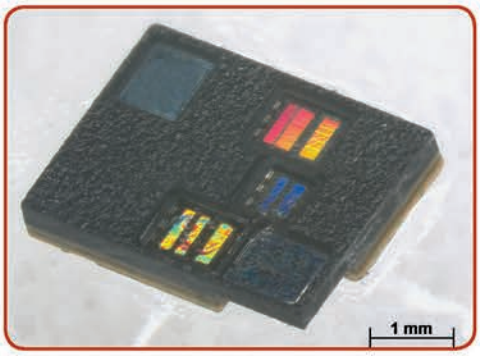
EMERGING PACKAGE FA METHODS FOR 2-D/2.5-D/3-D PRODUCT ANALYSIS

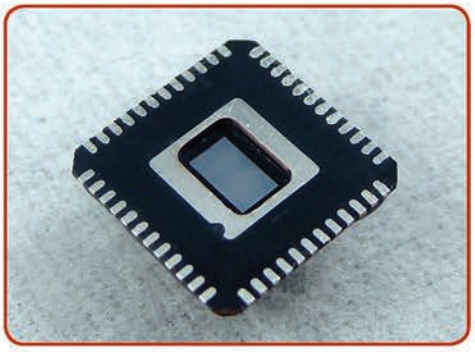
To overcome the limitations mentioned in this article and to meet FA requirements, several techniques have been either further or newly developed:

- *Lock-in thermography* (LIT) is a thermal defect localization method that can be applied for short localization in 3-D. Its resolution and sensitivity as well as the capability to isolate defects within specific 2.5-D/3-D packages have been successfully demonstrated and published.[4,5]
- *Superconducting quantum interference device (SQUID) or magnetic current imaging* has been further developed to isolate both shorts and opens and has been an often-applied board-level FA tool. Current developments aim to adapt this concept toward CSP-sized samples.[6]
- *3-D x-ray* has been widely adapted for semiconductor needs, and it provides high resolution and sensitivity. With the optimization of sources and detector material, a significant decrease in measurement time has been noticed. 3-D x-ray microscopy (XRM) offers a solution for structural analysis in complex 3-D integrated circuits because it can nondestructively penetrate through stacked materials and visualize internal structures with high resolution, even for intact 200 and 300 mm

(continued on page 34)

Small Device Preparation

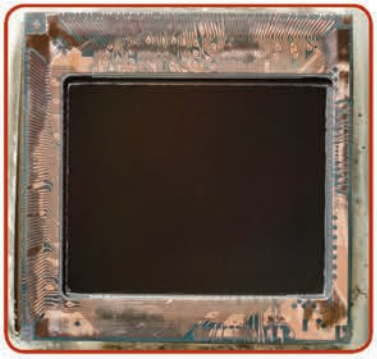




- Open areas as small as 100 x 100 µm

Complex Device & Stacked Die Deprocessing

- TSV exposure



- Targeted stacked die exposure

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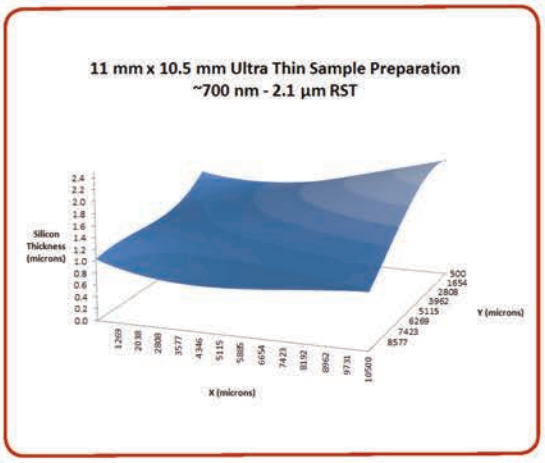
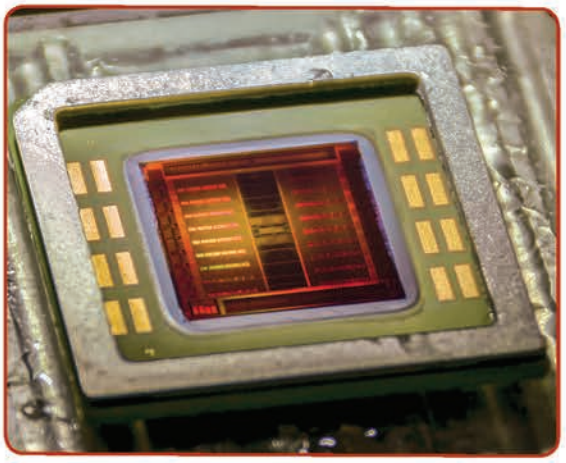
Solutions for Visible SIL Applications





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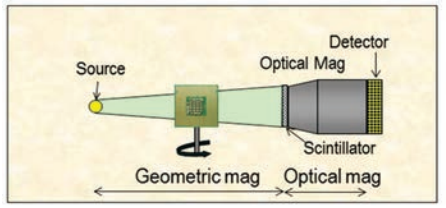
EMERGING TECHNIQUES FOR 2-D/2.5-D/3-D PACKAGE FAILURE ANALYSIS *(continued from page 31)*

wafers (Fig. 2). In process development, 3-D structures fabricated with a new or modified process often require validation prior to the next step. 3-D XRM imaging of specific critical structures, for example, gives direct physical evidence for the process engineer to analyze and unravel potential process issues. The benefits of 3-D x-ray include:

- Minor to no sample preparation

(a)



(b)

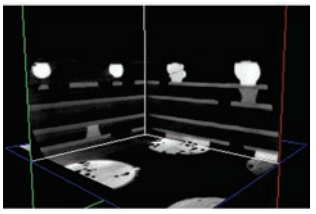
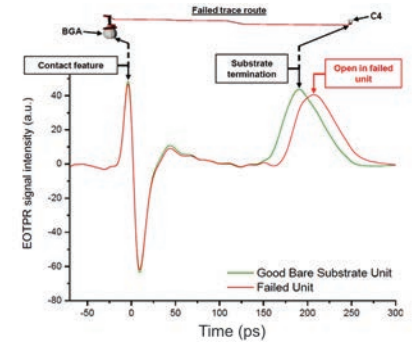


Fig. 2 (a) Operational principle of 3-D x-ray. Using sample rotation, several 2-D x-ray images are taken and processed. (b) As a result, a 3-D model is created that allows selective "virtual cross sectioning" of any desired *x-y-z*-layer.

(a)



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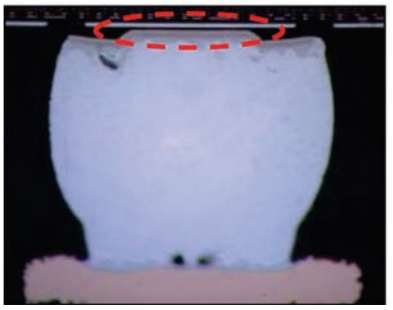


Fig. 3 (a) Introducing a high-frequency signal into the sample and measuring the time of flight of the reflected response allows a simple reference-versus-failing device comparison. (b) Cross sectioning and root-cause imaging of an open C4 bump after successful EOTPR measurement

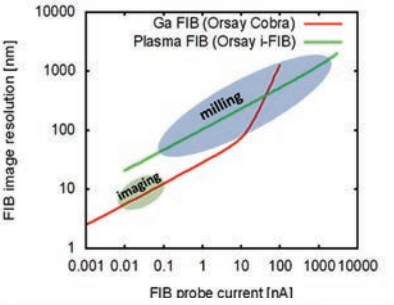
- Virtual cross sectioning leads to fully nondestructive FA
- 3-D navigation for FIB cross sectioning

- *Electro-optical terahertz pulse reflectometry* (EOTPR) has been introduced as a replacement for TDR applications by using a novel gigahertz-range pulse reflectometry.[7-11] During operation, electrical pulses are launched into the device under test via a high-frequency circuit probe. Reflections from device structures and faults are recorded as a voltage-time waveform by a fast photoconductive switch. This broadband technique has an extremely low time-base jitter and high temporal resolution. As a result of its principle, EOTPR can outperform classic TDR measurements and enable early defect isolation, whether in the package substrate, the die-substrate interface, or the die itself. An example can be seen in Fig. 3, where the difference in signal travel led to the detection of a missing C4 bump connection.
- *(Xenon) plasma FIB* has been developed based on the widely used gallium FIB (Ga-FIB) applications. It benefits from a much higher beam current in the microamp range, which enables large cross sections on package samples within 1 to 2 h. Figure 4 shows a comparison of FIB image resolution as a function of beam currents for gallium- and xenon-sourced FIBs.

As seen in Fig. 4(a), for beam currents above ~50 nA, the spot size for the plasma FIB is noticeably smaller

(continued on page 36)

(a)



(b)

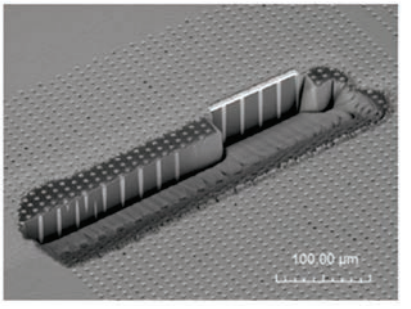
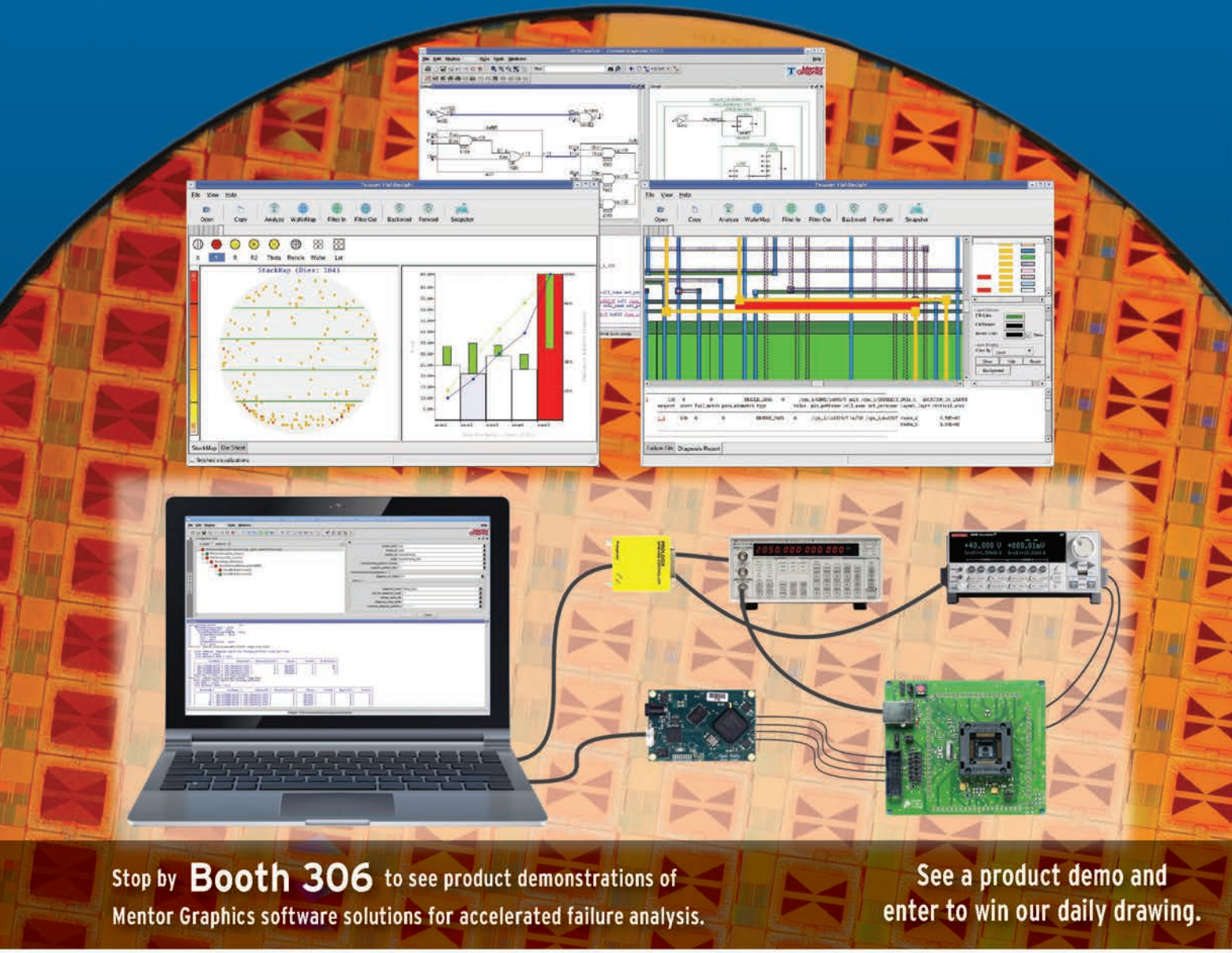


Fig. 4 (a) Comparison of resolution versus current for Ga-FIB and plasma FIB. (b) Demonstration of TSV cross sectioning

TIME TO ROOT CAUSE GETTING OUT OF CONTROL?



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EMERGING TECHNIQUES FOR 2-D/2.5-D/3-D PACKAGE FAILURE ANALYSIS *(continued from page 34)*

than for the Ga-FIB. Plasma FIBs are able to maintain a focused beam even at very large currents in the range of microamps. Due to this larger range of beam currents, plasma FIBs are able to achieve much higher milling rates for larger volumes of material removal. Although greater damage to the material may be expected with higher milling rates, the xenon atom, being heavier than gallium, creates a reduction of surface amorphization by approximately 24 to 57% on an integrated circuit.[12] Also, xenon, being a nonmetallic, inert element, does not form intermetallic compounds[13] as gallium ions do. With maintaining a high material-removal rate, higher beam currents must be used on the plasma FIBs. The main problem with using the higher beam currents and hence higher spot size is the generation of curtaining artifacts. To minimize these artifacts, the plasma FIB can be used in combination with a sample-rocking technique. The sample-rocking technique uses two alternating milling directions that are a few degrees away from the traditional vertical direction. Greatly improved results have been achieved by using this technique to cross section through silicon vias[14,15] and solder bumps.[15]

CASE STUDIES: APPLICATION OF EOTPR, X-RAY, AND PLASMA FIB FOR ELECTRICAL OPEN DETECTION

Because there have been many publications and discussions about the operational principle, performance, and comparison of SQUID and LIT, this article will focus on the application of EOTPR, 3-D x-ray, and plasma FIB specifically for the detection of electrical opens.

SAMPLE DESCRIPTION

To demonstrate the potential and advantage of the introduced FA techniques, a Globalfoundries test vehicle is investigated. Figure 5 depicts a schematic buildup showing a standard 20 nm flip-chip stacked dice sample with interconnects covered with mold compound.

OPEN DETECTION ON DIE-SUBSTRATE LEVEL

To demonstrate the FA flow advantage of the proposed methods, a sample with an electrical open in an unknown *x,y,z* location within the package has been used. After confirming the defect signature electrically, EOTPR is applied without any sample preparation. The results are plotted in Fig. 6. By comparing the failing sample to both a reference and a bare laminate sample, an additional peak can be observed.

The comparison in Fig. 6 clearly shows that the defect can be suspected in or close to the die-substrate interface. After reviewing the sample layout, the *z*-position of the defect is estimated, while *x* and *y* are still to be determined. For that purpose, the sample is investigated by 3-D x-ray (Fig. 7).

Reviewing the generated 3-D model, a difference in the fail-related microbump can be observed compared to the surrounding connections. By using the virtual cross-section feature, the root cause can be identified as a nonwetting bump issue. For the final step of the FA, the isolated defect position is investigated with plasma FIB. Therefore, the sample package is thinned from the laminate side. To ensure the defect is unharmed, sample preparation is stopped within the laminate, and the plasma FIB is used to cross section through the die-substrate interface (Fig. 8).

Cross sectioning the isolated defect area confirms the obtained 3-D x-ray results. Reaching the center of the bump, no connection between the microbump and substrate is visible. Instead, the original postbump shape

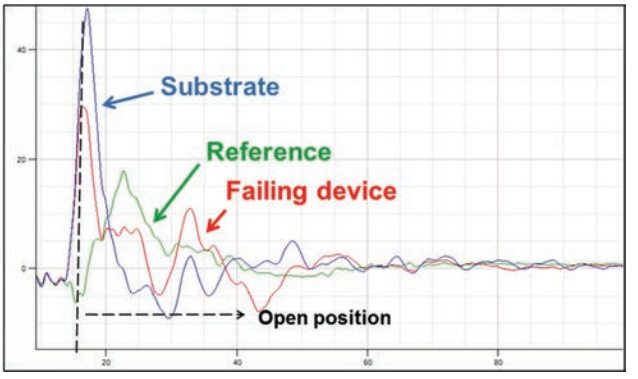


Fig. 6 EOTPR results on failing device, reference, and bare substrate indicate a defect located in the die-substrate interface

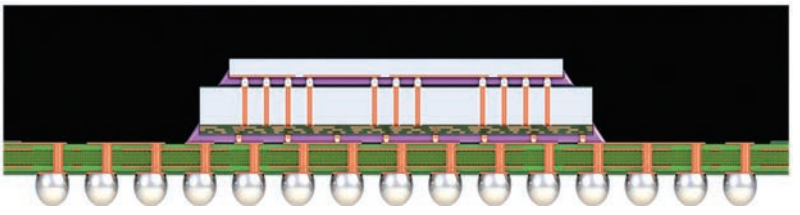
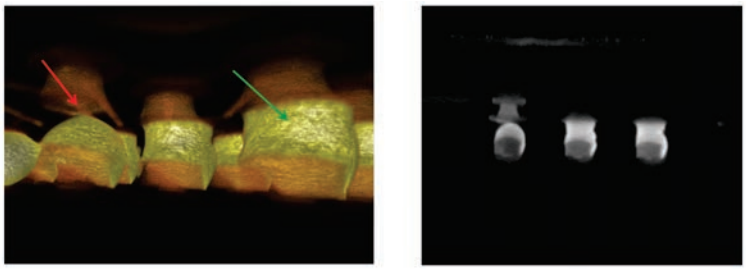


Fig. 5 Schematic drawing of wide I/O on logic dice with TSV



(a) (b)

Fig. 7 **(a) 3-D x-ray and (b) virtual cross section identify the root cause of the electrical open as a nonwet microbump.**

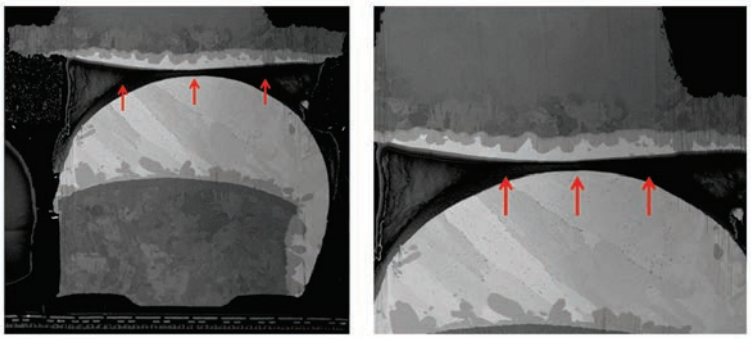


Fig. 8 **Plasma FIB cut through a failing bump confirms the 3-D x-ray results and root-cause theory of an unlanded microbump.**

is still visible, indicating a nonwet issue during package assembly.

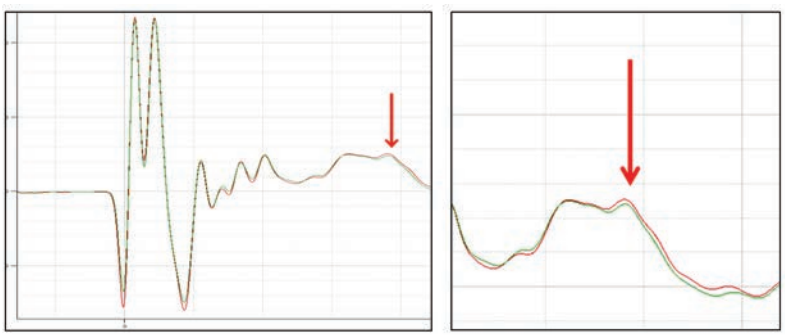
OPEN DETECTION ON DIE-DIE LEVEL

In a second case study, FA is conducted on the same package product. Here, multiple electrical opens have been detected after package assembly. Again, EOTPR is used as the first analyzing method (Fig. 9).

As the signal travels through the ball-grid array contact, laminate, and copper pillar region, an identical signature can be observed for reference and failing devices. As the signal enters the die-die interface, a slight difference is noticeable. This led to the working theory that the open is present within the TSV/microbump region. For further analysis, the region of interest was inspected by 3-D x-ray. As can be seen in Fig. 10, the root cause was identified as a general misalignment that resulted in partial or fully open interconnects between the TSV and microbump features.

For final confirmation and additional data gathering, the area of interest was cross sectioned by plasma FIB. Using the high-beam current advantage, a direct cut was made from the sample surface through the top die, interconnect interface, and bottom die (Fig. 11).

The FIB cross section through the TSV center for both reference and failing samples makes the failure root cause clearly visible. While the reference sample shows a solid interconnection between top die, microbump, and TSV, the failed sample is missing this connection. Furthermore,



(a) (b)

Fig. 9 **(a) EOTPR measurement overview and (b) high magnification of reference (green) and failing (red) device signatures. A slight difference is noticeable after the signal passes the ball-grid array contact and laminate.**

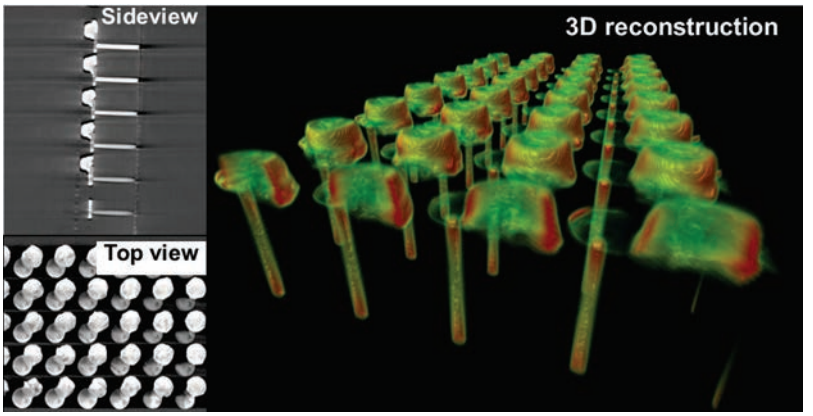
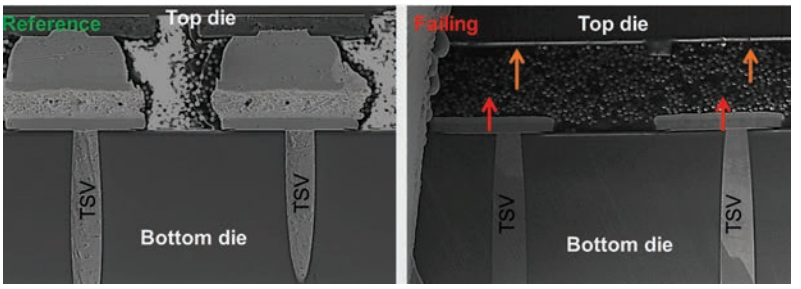


Fig. 10 3-D x-ray results showing a misalignment between microbumps and TSV features



(a) (b)

Fig. 11 Plasma FIB cut through x-ray-investigated area for (a) reference and (b) failing devices. High-magnification scanning electron microscopy imaging confirmed missing die-die interconnection as the root cause.

no bump pad can be seen on the top die side, which confirms a die-die misalignment as the most likely root cause. By using EOTPR, x-ray, and plasma FIB, this FA case was able to be closed within 5 to 8 h, with sufficient data information for follow-up questions and requirements.

CONCLUSION

In this article, the authors have attempted to reflect on the emerging issue of how high-quality package FA can be provided for increasingly complex 2-D, 2.5-D, and 3-D package products. After identifying pressing issues and potential bottlenecks with the state-of-the-art FA flow, the methods of EOTPR, 3-D x-ray, and plasma FIB have been introduced. An integration flow for specific FA cases has been proposed and demonstrated on two different case studies. Hereby, the FA results confirm the high potential of all three techniques and additionally enable the opportunity for a fully nondestructive FA approach. From a technical point of view, the following advantages can be observed:

- EOTPR allows for early detection of the defect *z*-position with the sample fully functional and unprepared. This enables further control over product-specific FA flow optimization.
- 3-D x-ray helps indicate the defect mechanism before physical failure analysis. Using the virtual cross-sectioning feature, the defect was isolated by 3-D, which allowed optimum navigation for the cross section. In addition, a combination of EOTPR and 3-D x-ray with a defect database opens the opportunity for a fully nondestructive package FA.
- Plasma FIB over conventional cross-sectioning techniques removes the risk of potential preparation artifacts such as cracks, foreign materials, or damage (slurry, acid, etc.). It also significantly reduces the turnaround time compared to Ga-FIB.

Considering these methods from a high-volume perspective, further optimization is required. In all cases, standard setups allow only one sample investigation at a time. While a multitool option is both cost and maintenance extensive, further development focus is needed on measurement automation.

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ABOUT THE AUTHORS

Christian Schmidt received his Diploma (Fachhochschule) in physics technology and data information from the University of Applied Sciences Merseburg and his Ph.D. in engineering from Martin Luther University Halle-Wittenberg. Since 2007, he has been an active member of the semiconductor FA industry, serving both as research fellow and FA engineer. Dr. Schmidt's development of 3-D defect localization using lock-in thermography has been widely published, leading to multiple patents and international paper awards. In 2014, he joined Globalfoundries Fab 8 in Malta, N.Y., first as a Member of the Technical Staff engineer before transitioning into the Senior Section Manager role for package FA.

Jesse Alton received an M.S. degree in physics from the University of London, Royal Holloway. He was employed at Pacific Northwest National Laboratory in Richland, Wash., where he undertook studies into the vitrification of high-level nuclear waste. He returned to the U.K. to complete a Ph.D. at the University of Cambridge, where he focused on the development of high-power terahertz sources and their applications. Upon completing his Ph.D., Dr. Alton joined TeraView Ltd. in April 2005, where he currently leads the Semiconductor Applications Group. He has authored or co-authored over 50 published papers.

Martin Igarashi has over 25 years of experience in the roles of engineering, applications engineering, sales and marketing, mergers and acquisitions, product development, and general management of product divisions in the electronic design automation, plasma etch, photolithography, test and measurement, and laser material processing industries. He has worked for companies such as Electro Scientific Industries, Toppan, ETEC Systems, Applied Materials, and Tektronix. Mr. Igarashi earned a Bachelor's degree in applied mathematics from the University of California, Santa Barbara. He currently heads TeraView's semiconductor business and is based in Portland, Ore.

Lisa Chan received a Bachelor's degree in chemical engineering and materials science and engineering from the University of California Irvine and a Ph.D. in materials science and engineering from Carnegie Mellon University. While at Carnegie Mellon, she researched the use of electron backscatter diffraction to investigate the relationship between grain-boundary orientations and intergranular corrosion cracking in aluminum alloys. Dr. Chan then analyzed grain-boundary distributions in three-dimensional microstructures of nickel-based superalloys, with a thesis titled "Synthetic Three-Dimensional Voxel-Based Microstructures that Contain Annealing Twins." In June 2013, Dr. Chan joined Tescan as an applications specialist responsible for performing demos, hosting training classes, and supporting customers. She is the main applications specialist for Tescan's FERA and XEIA plasma FIB-SEMs, but her expertise also extends to the LYRA and GAIA gallium FIB-SEMs and MIRA and VEGA microscopes. Dr. Chan has attended conferences, hosted workshops, and trained customers all over Canada and the United States.

Edward Principe is the FIB-SEM and FE-SEM Product Manager for North America for Tescan USA. Dr. Principe has more than 19 years of industry experience in advanced materials characterization, including FIB, FE-SEM, high-resolution TEM, ultrahigh-vacuum surface analysis methods (x-ray photoelectron spectroscopy, or XPS, and Auger), the design and manufacture of imaging near-edge x-ray-absorption fine structure (NEXAFS) hardware, and application of synchrotron-based methods (NEXAFS/XPS) for general materials research and the semiconductor industry. His previous employment includes Charles Evans & Associates (XPS/Auger/synchrotron), Applied Materials (FIB-Auger, distribution of relaxation time), Carl Zeiss NTS (Principal Scientist for North America), Founder/President of Synchrotron Research Inc., and Tescan USA (North America Product Manager for FIB-SEM and FE-SEM). Dr. Principe has written two textbook chapters on the application of FIB-Auger and FIB-based 3-D nanotomographic reconstruction, co-authored a Microscopy Society of America Best Paper Award winner relating to TEM/STEM characterization on advance dielectrics, and co-authored the recipient of an EDFAS Best Paper Award. He holds two patents in FIB-based 3-D reconstruction and has recently focused on the application development of both time-of-flight FIB-SIMS and the recent introduction of the Tescan RISE, the combination of electron and ion microscopy/spectroscopy with Raman optical spectroscopy.

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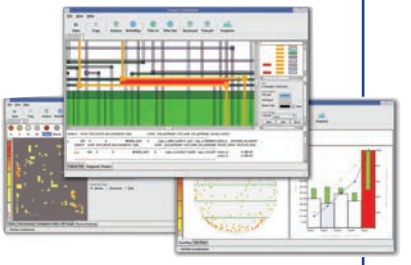

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423	Attolight AG
222	Balazs NanoAnalysis
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305	Hitachi High Technologies America, Inc.
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120	Materials Analysis Technology Inc.
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EDFAS ELECTIONS

EDFAS BOARD OF DIRECTORS ELECTIONS COMPLETED

Jeremy A. Walraven, Chair, EDFAS Nominations Committee, Sandia National Laboratories
jawalra@sandia.gov

The EDFAS Board of Directors general elections were completed in June 2016. This year we had five outstanding candidates nominated for two open Member-At-Large positions. Of the 662 EDFAS members, 117 voted in this year's election, resulting in a 17.67% participation. Elected to the Board for the September 2016 through August 2020 four-year term were:

Ted Lundquist
Consultant

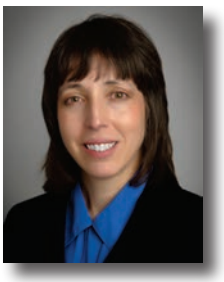
Becky Holdford
Consultant

On behalf of EDFAS and the Board of Directors, we would like to express our appreciation to all the candidates in this year's election. The Board would also like to thank the departing members Nicholas Antoniou, Christopher Henderson, and Jeremy Walraven for their years of service to EDFAS and its Board of Directors.

In August, the Board nominated and elected the officers for the September 2016 through August 2018 two-year term. The EDFAS officers for this two-year term are:

Positions filled by succession:

President:
Zhiyong Wang
Maxim Integrated



Immediate Past President:
Cheryl Hartfield
Oxford Instruments

Positions filled by vote of the Board of Directors:

Vice President:
Lee Knauss
IARPA

Secretary:
William E. Vanderlinde
IARPA

Finance Officer:
James Demarest
IBM

The Board of Directors is pleased to announce these results to the membership and looks forward to a successful future for EDFAS.

GUEST EDITORIAL

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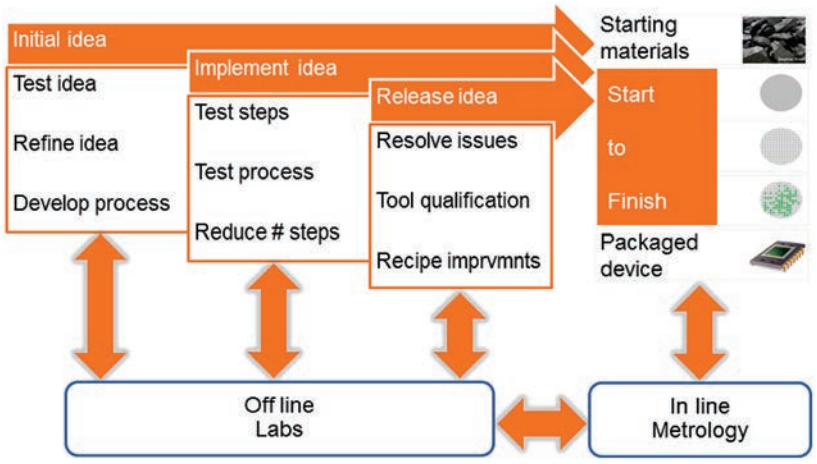

Fig. 1 Requirements of the FA labs in supporting R&D efforts

from the 130 nm to the 14 nm nodes. Solutions over this period can be subdivided into those resulting from:

- Enhancement of existing analytical techniques
- Development/application of new analytical techniques
- Development of new analysis approaches and/or sample-preparation methodologies

An example of the enhancement of existing analytical techniques lies in the introduction of spherical aberration correction in scanning electron microscopy and transmission electron microscopy (TEM)/scanning transmission electron microscopy (STEM). The fact that TEM/STEM are projection techniques has pushed the need for tomography and holography, with multiple approaches now available. Note: Although the diffraction limit of TEM/STEM is significantly smaller than that of atomic dimensions, the spatial resolution noted in tomography/holography now lies in the nanometer range.

Examples of the application of new techniques over this period may have included, but are not limited to, conductive atomic force microscopy, scanning spreading resistance microscopy, infrared atomic force microscopy, tip-enhanced Raman spectroscopy, and so on.

An example of a new analytical approach lies in the application of large-area techniques over areas populated with periodic repeating structures (for example, a sea of fins over 50 by 50 μm areas or larger). These have been found to be useful in providing data beyond the diffraction limit of the respective technique. Examples include secondary ion mass spectrometry (SIMS) in the form of 1.5-D SIMS, x-ray diffraction, critical-dimension small-angle x-ray scattering, and so on.

The demands on the FA labs are then taken to the next level if the respective HVM site is also involved in research and development (R&D). This is realized because the labs are critical in idea development through to process implementation and refinement, as illustrated in Fig. 1. The difference between the FA labs and metrology in this figure stems from the fact that the former is involved in process development (inclusive of evaluating new materials), process qualification, process refinement, through to the examination of process issues, while the latter is primarily concerned with process control, with some degree of issue/yield understanding also included (sometimes in separate departments). This also brings into question the terminology used (that of "FA labs"), as this would tend to describe a subset of their overall scope, that is, implies yield learning only as opposed to materials, device, and process learning.

Along with the FA lab capabilities are the expectations that the analytical techniques provide:

- High level of precision and repeatability
- Fast turnaround/cycle time
- Cost-effectiveness
- High uptime

Reasons for precision/repeatability lie in the fact that the respective process step or steps must be controllable to predefined upper and lower limits, which, in some cases, reach subatomic dimensions. (Although interrelated, device response is dictated by electric fields, not atomic dimensions.) The remaining three items can be tied directly to the financial stakes in semiconductor HVM.

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Larry Wagner, LWSN Consulting Inc.
lwagner10@verizon.net

PARK SYSTEMS LAUNCHES RESEARCH AFM

Park Systems (Suwon, Korea) launched Park NX20 300 mm, the first and only research atomic force microscope (AFM) on the market capable of scanning the entire sample area of 300 mm wafers using a 300 mm vacuum chuck while keeping the system noise level below 0.5 Å root mean square.

The Park NX20 300 mm system is run by SmartScan, Park's new operating software with automatic scan control, and it comes with "batch mode" functionality, where the users can perform a recipe-automated, unlimited number of sequential multiple-site measurements over the 300 × 300 mm area. The automated measurements over a 300 mm wafer dramatically improve user convenience and productivity in the industrial lab setting, where comparisons within site-to-site and sample-to-sample surface morphologies (height, surface roughness measurements) are extremely important.

"Today, large samples of up to 300 mm wafers and substrates are widely used for process development, failure analysis, and production, but so far there has not been an AFM measurement tool that can accurately measure the full area in one load and easily program it to take multiple-site measurements in one click," commented Keibock Lee, Park Systems' President. "Park NX20 300 mm accesses the entire 300 mm wafer in a single loading with low-noise AFM measurements, which opens up a whole new scope of measurement automation on a 300 mm wafer."

Park NX20 300 mm enables AFM inspection and scans over the entire sample area of 300 mm wafers by using a full 300 × 300 mm motorized *XY* stage, so the system can access any location on a 300 mm wafer. Unlike other products currently on the market, Park's NX20 300 mm is the only product that can hold a 300 mm sample. For example, the competitor's system that comes closest to Park's is combined with a 300 mm sample chuck but requires the user to load nine times to access the entire 300 mm wafer area, because the range of the motorized *XY* stage is limited to 180 × 220 mm.

Park NX20 300 mm standard vacuum chuck is designed to hold samples ranging in size from 300 to 100 mm and can even support small coupon samples of arbitrary shapes, using a vacuum hole. Products currently on the market are limited to 200 mm sample sizes and must rely on cutting up the sample to maintain the low noise required by industry, which is cumbersome and makes sharing the AFM a challenge. The new Park NX20 is the perfect solution for shared labs whose samples come in various sizes—small and large—because it supports from large to small coupon samples and is compatible with all the modes and options available to Park's other research AFM products.

For more information: web: parkafm.com; tel: 408.986.1110.

TERAVIEW INTRODUCES IC PACKAGE-INSPECTION SYSTEM

TeraView (San Francisco, Calif.), the pioneer and leader in terahertz technology and solutions, introduced the EOTPR 5000, a fully automated integrated circuit (IC) package-inspection system. Building on the success of the EOTPR 2000, which has an established track record in the industry for rapid fault isolation and manual inspection, the EOTPR 5000 is a fully automated advanced IC package-inspection system that uses TeraView's proprietary electro-optical terahertz pulse reflectometry (EOTPR) technology to detect weak or marginal interconnect quality in high-volume manufacturing environments, which no other technology can currently detect.

Today's advanced IC packages are susceptible to a variety of faults and quality variations, including solder ball defects such as head-in-pillow failures in package-on-package or 2.5-/3-D packages. These weak or marginal interconnect conditions may not be captured by logic or electrical testers even if there is good electrical continuity present. However, due to the EOTPR 5000's superior accuracy and sensitivity, users can now detect minute shifts in impedance changes from weak or marginal interconnects after accelerated life tests or high-temperature cycle tests. The same principle applies to the detection and reduction of manufacturing variations to improve packaging-related

(continued on page 50)

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PRODUCT NEWS

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yield, since the complexity of the advanced IC packages is increasing while the feature sizes are decreasing. The goal of the EOTPR 5000 is to improve the yield and reliability of today's advanced IC packages.

The EOTPR 5000 is truly a one-of-a-kind interconnect quality inspection tool for advanced IC packaging technology in high-volume manufacturing environments. No other tool can inspect and detect like the EOTPR 5000.

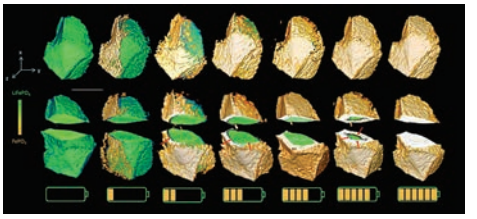
Dr. Don Arnone, TeraView's Chief Executive Officer, commented, "We are excited not only for TeraView but also for the entire terahertz industry to announce the launch of the EOTPR 5000. This product will be the first terahertz system ever to be deployed in a mass-production environment. It will be deployed to detect weak or marginal interconnects in advanced IC packages, which no other testers or inspection equipment can detect. This is a truly revolutionary inspection system for the world's leading IC manufacturers and for outsourced semiconductor assembly and test."

According to Martin Igarashi, Vice President of TeraView's Semiconductor Business, "Until the EOTPR 5000's arrival, IC manufacturers did not have 100% confidence in a so-called 'golden device' or 'known good device'." How would you know that your golden device is truly golden? But with the EOTPR 5000, combined with other existing inspection methods, IC manufacturers now can breathe a sigh of relief that their devices are reliable, and when their devices are put in their customers' smart phones or tablet devices, their confidence level should be significantly higher because of the EOTPR 5000. We are starting beta testing of the EOTPR 5000 at a major IC manufacturer's site in Asia shortly, to demonstrate that this product meets the rigor of the 24/7 IC manufacturing environments. This product will be available for customers in early 2017."

For more information: Alun Marshall; tel: 44 (0)1223 435380; e-mail: marketing@teraview.com.

NEW X-RAY IMAGING TECHNIQUE SLICES THROUGH MATERIALS

Researchers at the U.S. Department of Energy's Brookhaven National Laboratory (Upton, NY) have created a new imaging technique that allows scientists to probe the internal makeup of a battery during charging and discharging, using different x-ray energies while rotating the battery cell. The technique produces a 3-D chemical map and allows the scientists to track chemical reactions in the battery over time in working conditions. Their work was published in the August 12, 2016, issue of *Nature Communications*.



The chemical phase within the battery evolves as the charging time increases. The cut-away views reveal a change from anisotropic to isotropic phase-boundary motion.

Obtaining an accurate image of the activity inside a battery as it charges and discharges is a difficult task. Often, even x-ray images do not provide researchers with enough information about the internal chemical changes in a battery material, because 2-D images cannot separate out one layer from the next. Imagine taking an x-ray image of a multistory office building from above. Desks and chairs would be seen on top of one another, and several floors of office spaces would blend into one picture. It would be difficult to know the exact layout of any one floor, let alone to track where one person moved throughout the day.

"It's very challenging to carry out in-depth study of in situ energy materials, which requires accurately tracking chemical phase evolution in 3-D and correlating it to electrochemical performance," said Jun Wang, a physicist at the National Synchrotron Source II, who led the research.

Using a working lithium-ion battery, Wang and her team tracked the phase evolution of the lithium-iron phosphate within the electrode as the battery charged. They combined tomography (a kind of x-ray imaging technique that displays the 3-D structure of an object) with x-ray absorption near-edge structure spectroscopy (which is sensitive to chemical and local electronic changes). The result was a "5-D" image of the battery operating: a full 3-D image over time and at different x-ray energies.

To make this chemical map in 3-D, they scanned the battery cell at a range of energies that included the "x-ray absorption edge" of the element of interest inside the electrode, rotating the sample a full 180° at each x-ray energy and repeating this procedure at different stages

(continued on page 52)

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as the battery was charging. With this method, each 3-D pixel—called a voxel—produces a spectrum that is like a chemical-specific "fingerprint" that identifies the chemical and its oxidation state in the position represented by that voxel. Fitting together the fingerprints for all voxels generates a chemical map in 3-D.

The scientists found that, during charging, the lithium-iron phosphate transforms into iron phosphate but not at the same rate throughout the battery. When the battery is in the early stage of charging, this chemical evolution occurs in only certain directions. However, as the battery becomes more highly charged, the evolution proceeds in all directions over the entire material.

"Were these images to have been taken with a standard 2-D method, we wouldn't have been able to see these changes," Wang said. "Our unprecedented ability to directly observe how the phase transformation happens in 3-D reveals accurately if there is a new or intermediate phase during the phase-transformation process. This method gives us precise insight into what is happening inside the battery electrode and clarifies previous ambiguities about the mechanism of phase transformation."

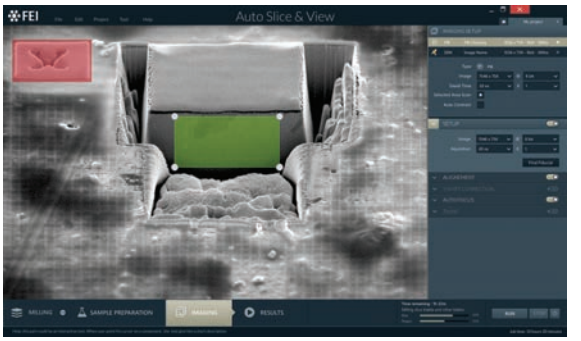
Wang noted that modeling will help the team explore the way the spread of the phase change occurs and how the strain on the materials affects this process.

For more information: web: nature.com/articles/ncomms12372.

FEI ANNOUNCES NEW SLICE & VIEW SOFTWARE

FEI (Hillsboro, Ore.) announced the release of the latest version of its Auto Slice & View 3-D reconstruction software, which makes 3-D imaging faster, easier, more accurate, and cost-effective. The software works with all of FEI's current DualBeam focused ion beam/scanning electron microscope platforms to enable 3-D structure and composition of samples at the nanometer scale. DualBeam users across all disciplines, including materials science, life sciences, semiconductors, and oil and gas, can benefit from the new, enhanced software.

"FEI pioneered the development of the DualBeam and its use to reconstruct 3-D structures," said Jean-Bernard Cazeaux, Vice President of FEI's Applications Software Group. "This latest version of our Auto Slice & View software leverages our extensive experience to provide a better tool to enable users to obtain the results they need in a shortened timeframe and with limited effort. Ultimately, the results provide a better representation of all the information available from the sample volume and significant improvements in laboratory productivity."



FEI's Auto Slice & View 4.0 imaging setup screen

FEI's new Slice & View software 4.0 features several enhancements:

- *Productivity:* Imaging can be combined with analytical capabilities, such as energy-dispersive x-ray spectrometry and electron backscatter diffraction, to ensure that no information is lost in the sectioning of the sample. Automated procedures can be modified on the fly, with the capability of adding analytical signals if an unexpected feature is revealed. Imaging and analysis can be dynamically directed to selected areas of the section or applied only on certain slices to save time. Slice & View analyses can be performed at multiple sites to allow long, unattended runs overnight or on weekends. Advanced tiling and stitching capabilities maintain high spatial resolution over sections larger than a single field of view.
- *Precision and accuracy*: New algorithms help to ensure uniform thickness of the slices as well as precise and reproducible placement of each cut, allowing for higher accuracy.
- *Ease of use:* A redesigned interface optimizes user guidance and ensures that critical information is presented, if needed. A prompted workflow approach streamlines the setup of automated procedures, and any procedure can be tagged as a template to serve as the basis for future analyses.

Current users of version 3.0 can upgrade to the new 4.0 version.

For more information: web: fei.com/software/auto-slice-and-view/.

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November 2016

EVENT	DATE	LOCATION
How to Make the Most of Your AFM Measurements: A Hands-On Laboratory Short Course	11/1-2	Cambridge, MA
Contact: SurfaceChar LLC		
ISTFA Conference & Exposition	11/6-10	Fort Worth, TX
Metallographic Techniques	11/7-10	Novelty, OH
Advanced Metallographic Techniques	11/14-17	Novelty, OH
Practical Fractography	11/30-12/1	Lansing, NY
Contact: ASM International		
Infrared Microscopy	11/7-9	Westmont, IL
Spectral Interpretation	11/10-11	Westmont, IL
Polarized Light Microscopy	11/28-12/2	Westmont, IL
Contact: The McCrone Group		
Image Quality and PeakForce QNM	11/15-17	Santa Barbara, CA
Contact: Bruker Nano Surfaces Division		
Space Coast Expo & Tech Forum	11/17	Melbourne, FL
LED Assembly, Reliability, & Testing Symposium	11/29-12/1	Atlanta, GA
Contact: SMTA		

December 2016

EVENT	DATE	LOCATION
IEEE International Electron Devices Meeting	12/3-7	San Francisco, CA
Contact: IEDM 2016		
Introduction to Metallurgical Lab Practices	12/5-7	Novelty, OH
Metallurgy for the Non-Metallurgist	12/5-8	Novelty, OH
Contact: ASM International		

January 2017

EVENT	DATE	LOCATION
Introduction to Processing	1/5-6	Shanghai, China
Contact: Semitracks, Inc.		
Annual Reliability and Maintainability Symposium	1/23-26	Orlando, FL
Contact: RAMS 2017		
Raman Microspectroscopy	1/24-26	Westmont, IL
Contact: The McCrone Group		
Electrical Safety Workshop	1/31-2/3	Reno, NV
Contact: ESW 2017		

February 2017

EVENT	DATE	LOCATION
Pan Pacific Microelectronics Symposium	2/6-9	Kauai, HI
Contact: SMTA		
Polarized Light Microscopy	2/20-24	Westmont, IL
Contact: The McCrone Group		

March 2017

EVENT	DATE	LOCATION
Compound Semiconductor International Conference	3/7-8	Brussels, Belgium
Contact: CSIC 2017		
Dallas Expo & Tech Forum	3/7	Plano, TX
Houston Expo & Tech Forum	3/9	Stafford, TX
Contact: SMTA		

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"WHAT STARTS HERE CHANGES THE WORLD:" RESEARCH HIGHLIGHTS FROM THE UNIVERSITY OF TEXAS AT AUSTIN, DEPARTMENT OF PHYSICS

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If you've seen the ads, mainly during football games, then you may have heard the motto of the University of Texas at Austin: "What Starts Here Changes the World." Indeed, the University of Texas is one of the leading research universities in the country, with annual expenditures exceeding $600 million (average for the last four years).[1] Some of the research that may be of interest to the failure analysis community is highlighted in this issue, which emphasizes research from the department of physics. In a future issue, research from the Microelectronics Research Center will be discussed.

In the physics department, Professor Mike Downer's group focuses on femtosecond laser spectroscopy in condensed matter and plasmas, which includes the study of kinetic processes and defect structures in semiconductors.[2] His group has developed scanning second-harmonic-generation (SHG) microscopy,[3] which has found applications in the semiconductor industry. Demonstrated applications of SHG to semiconductor materials include:

- Hot carrier injection in silicon-on-insulator materials can be measured without the need for a fabricated device.
- SHG, combined with internal photoemission, is used to determine band offsets and defects in high-k dielectrics (e.g., HfO_2).
- SHG has been used to identify antiphase-boundary defects in epi-GaAs-grown films on silicon substrates.
- SHG is much faster than conventional Raman microscopy for measuring strain in through-silicon vias.[4]

Professor Manfred Fink's group is developing an intense positron source.[5] Positrons are useful for nondestructive analysis of lattice defects in semiconductors; they are particularly effective for identification of lattice vacancy defects. However, the lack of intense sources has kept positron annihilation spectroscopy from being more widely adopted in the industry. In addition, Dr. Fink's group, along with Professor Jacek Borysow at Michigan Technological University, has developed one of the world's most sensitive Raman spectrometers. For example, it has been used to identify trace contamination, such as ammonium nitrate, on silicon surfaces, with detection limits below 1 nmol. It is expected that many other organic and inorganic trace contaminants could be detected with similar or better sensitivity.[6]

Professor John Keto's group,[7] the lab where I used to work, also has extensive experience with Raman techniques and other nonlinear optical phenomena that have been applied in industry for contamination, stress, and thermal analysis. Additionally, an optical third-harmonic-generation microscopy technique developed with Dr. Downer shows promise for super-resolution (sub-Rayleigh) analysis of thin films at dielectric interfaces.[8]

Professor Keji Lai's team has developed a novel near-field microwave impedance microscope.[9,10] Using microwave (gigahertz) frequencies, the probe is unusually qualified to nondestructively determine local dielectric (capacitive) and conductivity (resistive) properties of materials (simultaneously) down to 10 nm resolution; furthermore, it can be easily integrated into an atomic force microscope (AFM). In one application, the researchers were able to show an unexpected implant layer in a SRAM that scanning capacitance microscopy failed to detect.[11]

Other research groups involved with near-field scanning techniques are those of Professor Alex De Lozanne and Professor Chih-Kang "Ken" Shih. Both are some of the earliest practitioners of near-field scanning probe technology. Professor De Lozanne's group[12] uses scanning tunneling microscopy (STM), magnetic force microscopy, and AFM to study nanostructures, thin-film devices,

UNIVERSITY HIGHLIGHT

high-temperature superconductors, and "colossal magnetoresistance" materials. Professor Shih's nanoelectronics material research group[13] uses STM and AFM to study and engineer novel materials at the atomic scale. He, along with Advanced Micro Devices, was one of the first in the industry to use AFM to characterize 2-D dopant profiles.[14] Furthermore, Professors Shih and Keto have developed a near-field scanning optical microscope to analyze optical properties of semiconductor heterostructures.[15]

Finally, Professor Alexander Demkov's group does both theoretical and experimental work on materials important to the semiconductor industry.[16] He has been a contributor to the *International Technology Roadmap for Semiconductors* and was involved in the early development of high- and low-k dielectrics for industry. Recently, he was cited in *EE Times*[17] for developing ferroelectric field-effect transistors that can potentially replace conventional memories such as DRAMs and SRAMs with higher performance and smaller dimensions.

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LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Novel Materials, Packages, Components, and 3-D Integration

Michael R. Bruce, Consultant
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The current column covers peer-reviewed articles published since 2014 on novel materials, packages, components, and 3-D integration. Novel materials include low- and high-k dielectrics, while packaging/3-D integration encompasses topics such as through-silicon vias, multichip modules, packaging materials, components, and so on. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

- A. Alkauskas, M.D. McCluskey, and C.G. Van de Walle: **"Tutorial: Defects in Semiconductors—Combining Experiment and Theory,"** *J. Appl. Phys.,* 2016, *119*, p. 181101.
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- Y. Cho, F. Shafiei, M.C. Downer, et al.: **"Second-Harmonic Microscopy of Strain Fields around Through-Silicon-Vias [TSVs],"** *Appl. Phys. Lett.,* 2016, *108*, p. 151602.
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- J. Dai, P. Mukundhan, C. Kim, et al.: **"Analysis of a Picosecond Ultrasonic Method for Measurement of Stress in a Substrate,"** *J. Appl. Phys.,* 2016, *119*, p. 105705.
- D. Gao, B. Liu, Z. Xu, *et al.*: **"Failure Analysis of Nitrogen-Doped $Ge_2Sb_2Te_5$ Phase Change Memory [Using HRTEM and EDS],"** *IEEE Trans. Dev. Mater. Reliab.,* 2016, *16*, p. 74.
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- T. Jiang, R. Huang, P.S. Ho, et al.: **"Study of Stresses and Plasticity in Through-Silicon Via [TSV] Structures for 3D Interconnects by X-Ray Micro-Beam Diffraction,"** *IEEE Trans. Dev. Mater. Reliab.,* 2014, *14*, p. 698.
- S. Kundu, D. Maurya, M. Clavel, et al.: **"Integration of Lead-Free Ferroelectric on HfO_2/Si (100) for High Performance Non-Volatile Memory Applications,"** *Sci. Rep.,* 2015, *5*, p. 8494.
- K.W. Lee, J.C. Bea, Y. Ohara, et al.: **"Impacts of Cu Contamination on Device Reliabilities in 3-D IC Integration,"** *IEEE Trans. Dev. Mater. Reliab.,* 2014, *14*, p. 451.
- Y. Li, P.K.M. Srinath, and D. Goyal: **"A Review of Failure Analysis Methods for Advanced 3D Microelectronic Packages,"** *J. Electron. Mater.,* 2016, *45*, p. 116.
- M.J. Mutch, P.M. Lenahan, and S.W. King: **"Defect Chemistry and Electronic Transport in Low-k Dielectrics Studied with Electrically Detected Magnetic Resonance,"** *J. Appl. Phys.,* 2016, *119*, p. 094102.
- S. Ogawa, R. Asahara, Y. Minoura, et al.: **"Insights into Thermal Diffusion of Germanium and Oxygen Atoms in HfO_2/GeO_2/Ge Gate Stacks and Their Suppressed**

ABOUT THE COVER

a) Scanning electron microscopy image of a crystalline corrosion product extracted from a water-cooled laser diode. Material analysis indicated that the corrosion was from an introduction of potassium bicarbonate on copper metallization. *Photo by Luigi Aranda, Raytheon Failure Analysis Lab, Second Place Winner, Black & White Images.*

b) Conducting failure analysis on wafers in the semiconductor industry often requires analysis of defects on the backside of the wafer, which can cause focal issues on scanner toolsets. This defect is an example of a particle that was not removed and has had several films deposited over top of it. *Photo by Joseph Ziebarth, IM Flash Technologies, LLC, Second Place Winner, Color Images.*

c) "Fixing a Broken Heart." An etch artifact on a bond pad after subjecting the unit to ball bond removal. *Photo by Rony R. Celetaria, Analog Devices Gen. Trias, Inc., Third Place Winner, Black & White Images.*

d) The optical image shows silver dendritic growth on a ground lead (or pin) of a transistor outline can device. The dendrites originated from the braze alloy and penetrated through the plating layer. The likely cause is improper storage conditions (excessive moisture) of the part. *Photo by Martin Serrano, Raytheon Failure Analysis Lab, Third Place Winner, Color Images.*

e) "The Sea Serpent's Pac-Man." Solderable metal Pac-Man structure is not sealing the top of the passivation layer, allowing entrance of contamination under the nickel. This creates a porous or spongy nickel appearance due to corrosion of the layer by an aged or pH-imbalanced gold bath used in the electroless nickel immersion gold process. *Photo by Debra L. Yencho, Texas Instruments, Third Place Winner, False Color Images.*

f) "A View from Space: River Patterns and Lakes." The image shows a moisture bubble emanating from a cracked ceramic capacitor body after a cross-sectional procedure. The false color was added to this scanning electron microscopy image by using postprocessing software. False color is often useful for accentuating material differences and features. The resulting image is reminiscent of a satellite image. *Photo by Andrew Ozaeta, Raytheon Failure Analysis Lab, Second Place Winner, False Color Images.*

All images from the 2015 EDFAS Photo Contest.

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NOTEWORTHY NEWS

2017 IRPS CONFERENCE

The IEEE International Reliability Physics Symposium's (IRPS) annual conference will be held **April 2 to 6, 2017,** at the Hyatt Regency in Monterey, Calif.

The deadline for submission of paper and poster abstracts is October 15, 2016. IRPS 2017 is soliciting increased participation in the following areas: system reliability; middle-of-the-line; extrinsic defect impact on yield and reliability; and commercial off-the-shelf components in high-reliability applications, including screening, derating, case studies, design considerations, and so on.

The IRPS Conference is sponsored by the IEEE Reliability Society and IEEE Electron Device Society. For more information, visit the IRPS website at irps.org.

GUEST COLUMNIST

TRAINING IN AN ERA OF INDUSTRY CONSOLIDATION AND AUTOMATION

Christopher Henderson, Semitracks, Inc.
henderson@semitracks.com

Writers have spilled a lot of ink during the past two years regarding the consolidation of the semiconductor industry. Of course we read the usual comments: jobs will be lost due to redundancy, growth for our industry is over, etc. How is this era of consolidation going to affect those of us working in failure analysis labs throughout the industry? Here is my take on this concern.

While the industry has indeed consolidated, it is not completely clear how many engineering jobs will be lost. Certainly, there are economies of scale within the finance, human resource, purchasing, and logistics operations of these companies. There may also be some economies of scale (in the long run) on the manufacturing side as well. However, product engineering is one area in which it is difficult to achieve an economy of scale. The activities associated with new product introduction, test engineering, reliability, qualification, and failure analysis have been, and remain, difficult areas to consolidate. As companies combine, they generally do not reduce the number of products they sell. This should bode well for our discipline.

The more interesting trend is automation. In theory, automation could lead to a reduction in jobs. The automation of tasks should allow fewer analysts to accomplish more analysis work. Is this really the case though? While we have benefited from the development of new failure analysis techniques that have helped productivity, there has not been wholesale automation of failure analysis work. The fault isolation of complex systems-on-chip can run into weeks for more challenging problems. Part of the reason for this is that the chips we are analyzing are also increasing in complexity. The integrated circuitry is more complex, the packages are more complex, and the test routines are more complex. Automation in this area simply does not keep up with the increase in complexity. This phenomenon is also true in the electronic design automation industry. The design of chips has not decreased because the complexity has increased as much or faster than we can improve the design tools, algorithms, and design flow.

> "HOW IS THIS ERA OF CONSOLIDATION GOING TO AFFECT THOSE OF US WORKING IN FAILURE ANALYSIS LABS THROUGHOUT THE INDUSTRY?"

Here is another example: We have not increased the throughput on decapsulation. The reason for this is primarily due to the increase in complexity of our products from a packaging perspective. We simply do not understand all of the parameters around package geometries and materials to do this effectively. Furthermore, we continue to introduce new packages and materials at an accelerating rate. Therefore, I don't see failure analysis succumbing to automation anytime soon, as might be the case with, for example, Fed-Ex or UPS couriers or taxi drivers. If the rate of change in our industry slows markedly, then we may see more automation, but that is likely to be some time from now.

So, if we don't see big workforce changes in our industry due to consolidation or automation, how do we think about our jobs? The one thing we cannot be is complacent. If we do not work to improve our skills, then we do run the risk of job loss through the failure of our company due to unsolved problems that leave our company uncompetitive. Even though automation may not directly take our jobs, we do need to embrace automation of various tasks. Right now, this may mean learning about automatic test pattern generation diagnosis, or learning how to automate a portion of the transmission electron microscope lift-out process. This involves learning more software. An increasing amount of our analysis work will be done through a computer screen, rather than through manipulation with our hands. Computer skills and a willingness to learn new computer-based skills will be essential.

For many of you, consolidation means that you will be

(continued on page 64)

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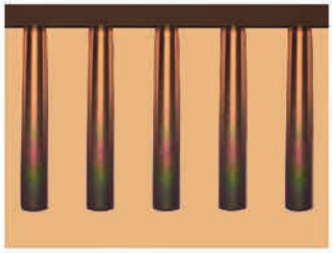

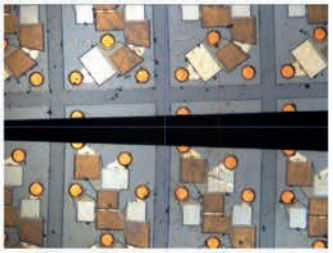

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TRAINING IN AN ERA OF INDUSTRY CONSOLIDATION AND AUTOMATION *(continued from page 62)*

analyzing a wider variety of components. This means you need a broader knowledge base. Rather than knowing a single wafer fab process, you may need to know several, or even several dozen. Rather than knowing about one particular package type, you may need to know several, or even several dozen. The fundamentals will still matter, so be sure to continue your learning to understand the chip design process, how to test integrated circuits, reliability issues, failure mechanisms, packaging design and materials, and how to tackle yield issues. As always, we here at Semitracks Inc. stand ready to assist you in this effort through in-person as well as online training courses. Electronics manufacturers highly covet the knowledgeable failure analyst who can lead a team effort to rapidly and effectively solve problems. Position yourself for one of these roles.

ABOUT THE AUTHOR

Christopher Henderson received his B.S. degree in physics from the New Mexico Institute of Mining and Technology and his M.S.E.E. from the University of New Mexico. He is the President and one of the founders of Semitracks Inc., a U.S.-based company that provides education and training to the semiconductor industry. Chris also teaches courses in failure analysis, reliability, and semiconductor technology for the semiconductor industry. From 1988 to 2004, he worked at Sandia National Laboratories, where he was a Principal Member of the Technical Staff in the Failure Analysis Department and the Microsystems Partnerships Department. His job responsibilities have included reliability, failure and yield analysis of components fabricated at Sandia's Microelectronics Development Laboratory, research into the electrical behavior of defects, and consulting on microelectronics issues for the Department of Defense. He was the General Chair of ISTFA 2007 and IRPS 2016. Chris has published more than 25 papers at various conferences in semiconductor processing, reliability, failure analysis, and test. He has received two R&D 100 Awards and two Best Paper Awards. Prior to working at Sandia, Chris worked for Honeywell, BF Goodrich Aerospace, and Intel. Chris is a senior member of IEEE and a member of the EDFAS and IRPS Boards of Directors.

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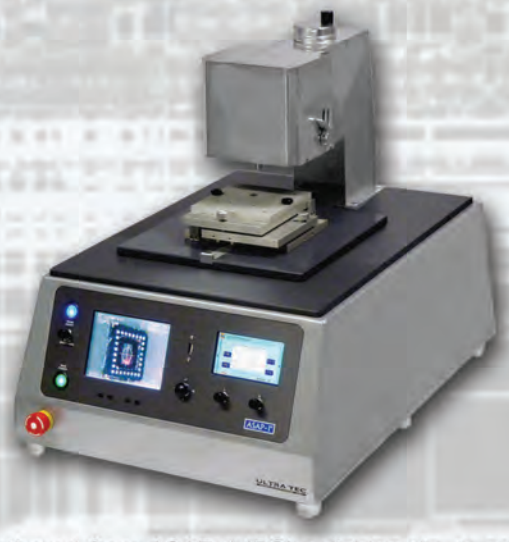
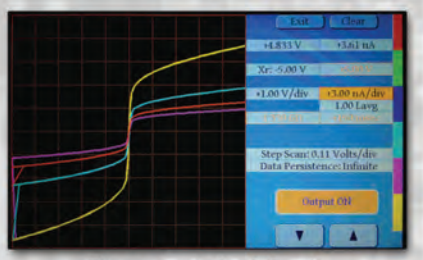
REALTIME FA

The Convergence of Sample Prep & Analytical Methods



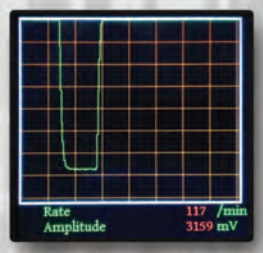
PEEC is a patent-pending system upgrade that uses electronic data, gathered from ASAP-1 IPS' polishing tip, to provide REALTIME through-silicon characterization of the device under test (DUT) -- thus achieving a specific remaining silicon micron thickness (RST) in the low single digits, and below. PEEC is suitable for dies which have already been thinned below 20 microns and offers PARAMETRIC, PLOT and OSCILLOSCOPE modes to achieve a higher level of confidence than traditional "cut-image-then-cut-some-more" techniques, by removing the need to continually transfer the part between polisher and microscope. An Auto-Trip can be set to turn off the thinning process at a specific point.

PEEC Provides The Analytical Techniques, Your Part Provides The Answer!



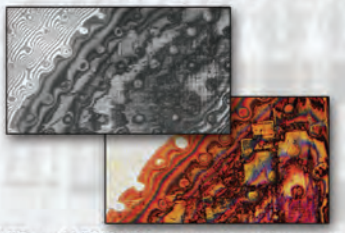
Parametric Mode

ULTRATHIN with Confidence



Oscilloscope

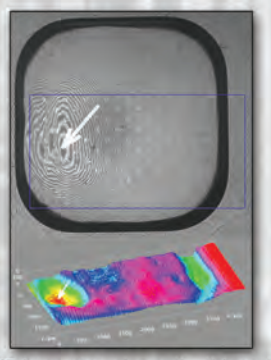
Plot Screen



NIR and VISIBLE Images show the same position as the Plot screen for silicon breach

An integrated lab approach uses on-line and off-line tools to achieve the best results

Compare Surface Scans with Through-Wafer Measurements



NIR image top shows the thinnest area on a thinned- deliberately tilted die. Lower image shows a C-SPM scan made on ASAP-1 IPS of the same area showing a consistent point of minimum RST.

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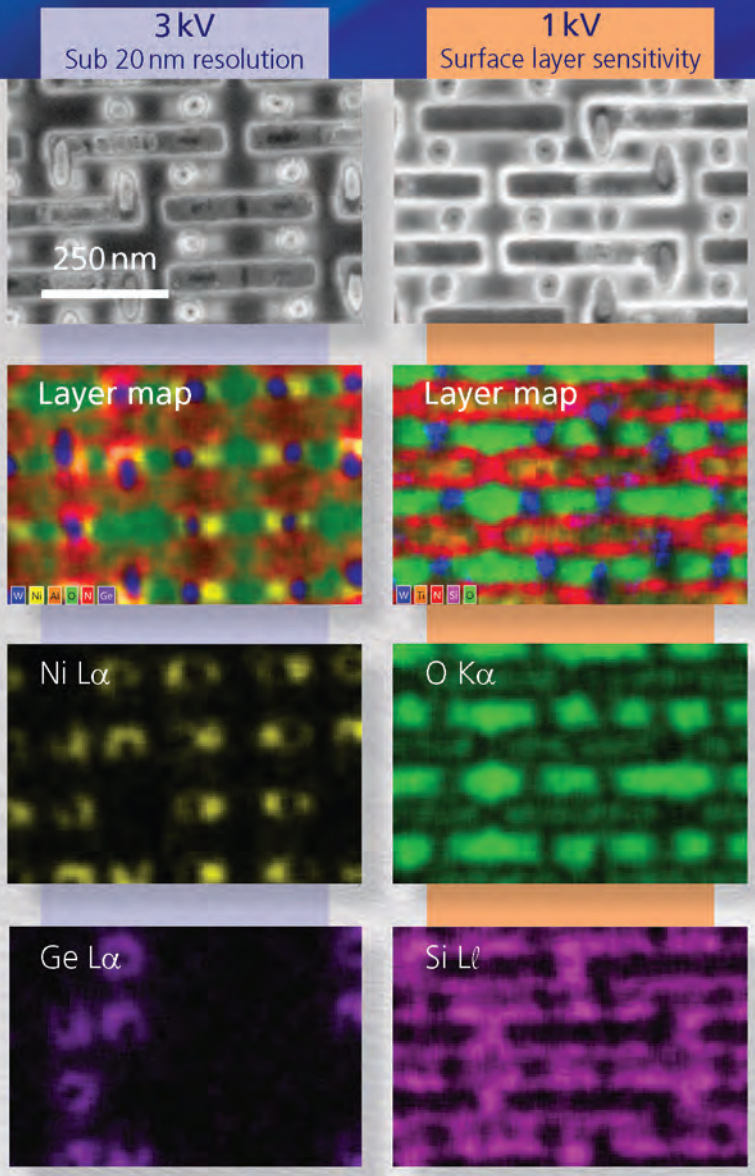

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