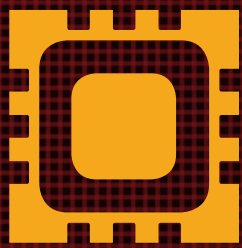


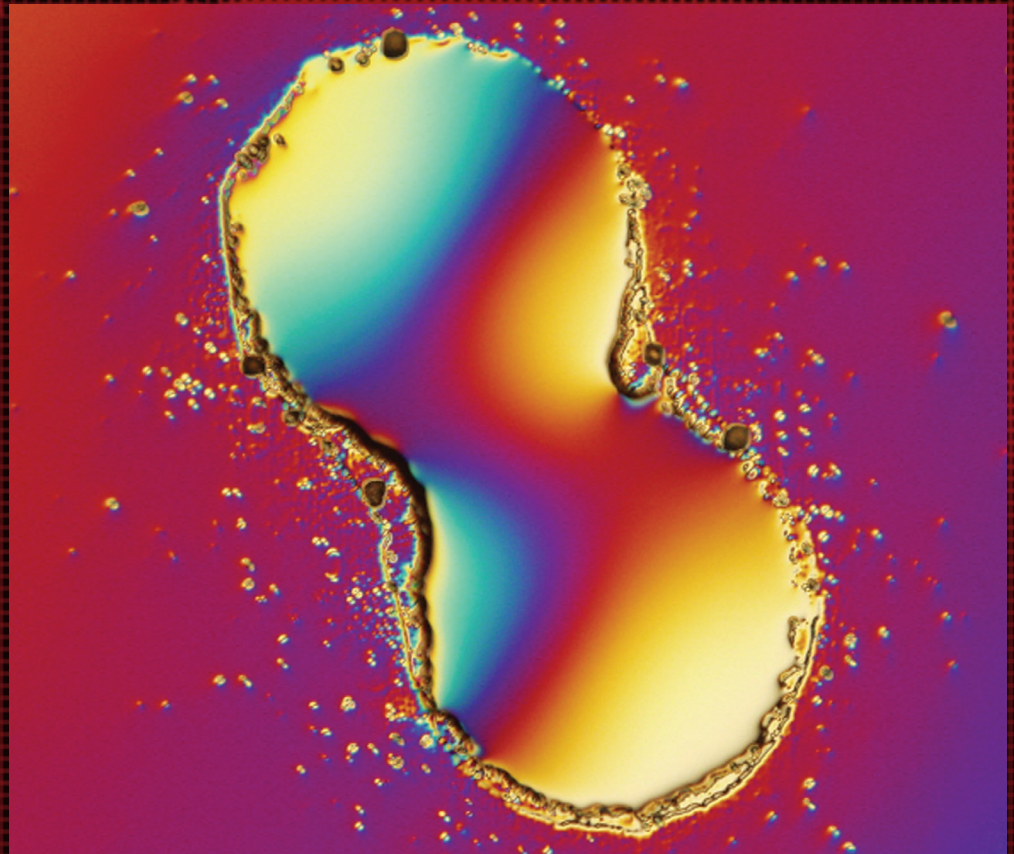
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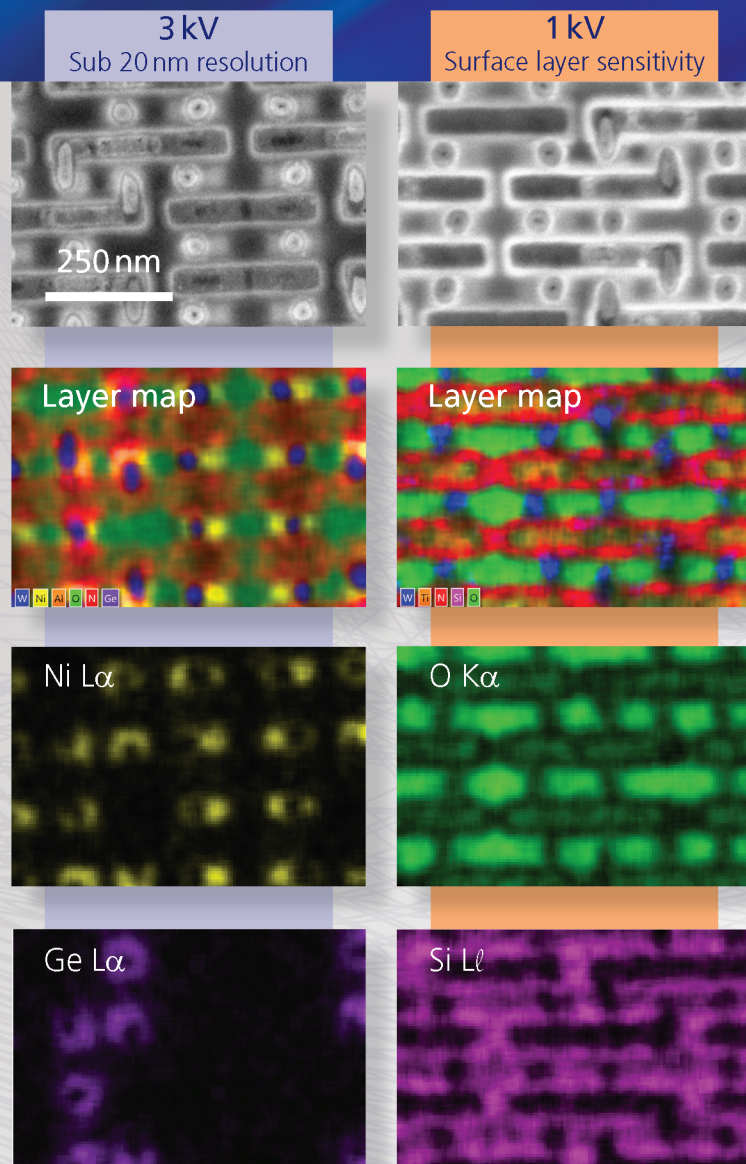
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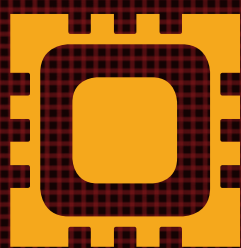
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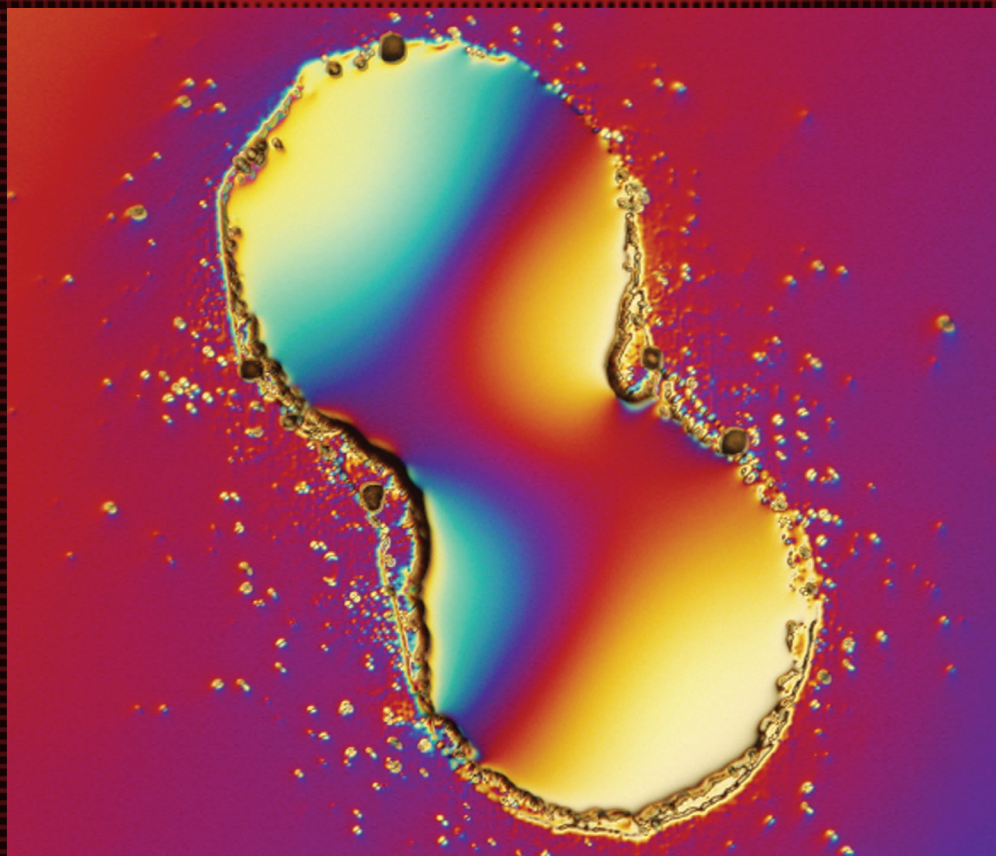


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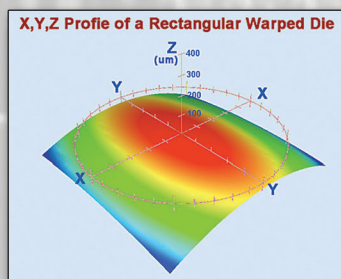
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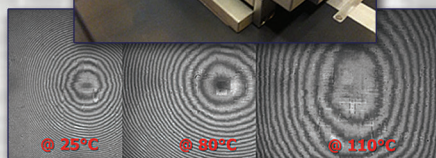
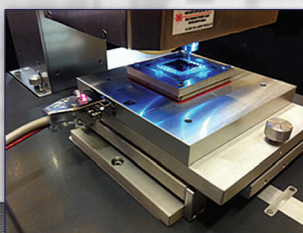


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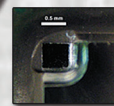
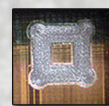
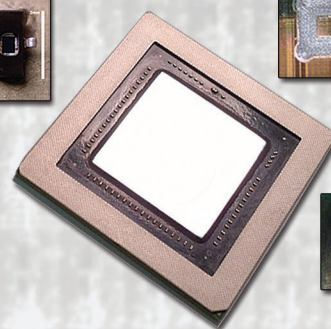
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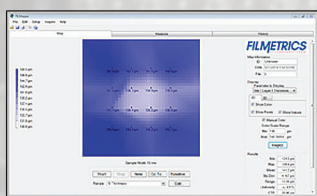
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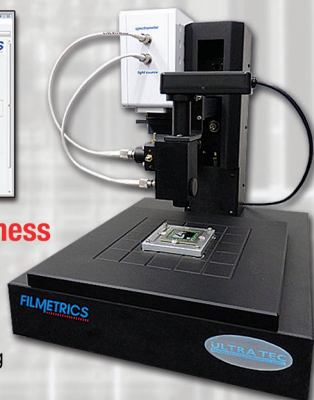
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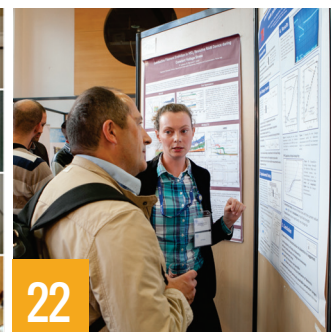
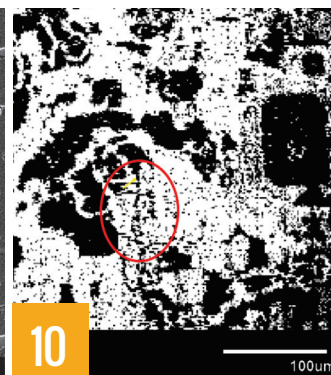
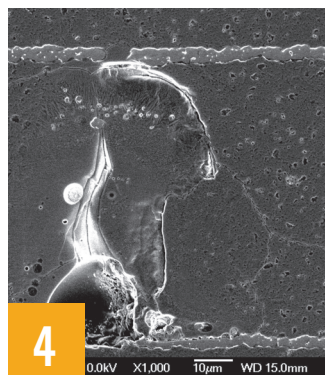
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John Bescup

Passive components remain an integral part of today's circuit design. Read about the unlikely failure mode of a high-voltage leaded-ceramic-chip capacitor for downhole application.

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S.H. Goh, B.L. Yeoh, G.F. You, Y.H. Chan, Zhao Lin, Jeffrey Lam, and C.M. Chua

This article details the fundamentals behind EeLADA, a technology evolution in extracting relevant signals for debugging soft and hard failures.

18 Manageability Challenges for Internet of Things

Yen-Kuang Chen

The Internet of Things concept is the "next big thing," but what are the obstacles to achieving that vision? Device failure, sensitivity, scalability, middleware, and user interaction are challenges for this evolving technology.

22 ESREF 2015 in Toulouse

Marise Bafleur and Philippe Perdu

This review includes highlights from the 26th ESREF symposium, which focused on aeronautic, space, and embedded systems in 2015.

ABOUT THE COVER

In situ solid immersion fabrication lenses created by randomly scattering polyethylene spheres across the backside of a die, then melting the spheres to form microscopic etch masks. The sample was plasma etched, and the plastic was removed. The sample was polished using colloidal silica. The lens shapes formed naturally due to the dynamics of polishing. The photo was taken using differential interference contrast. *Photo by Mark Kimball, Maxim Integrated Circuits. First Place Winner in False Color Images, 2015 EDFAS Photo Contest.*

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PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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GUEST EDITORIAL |

WHO IS A FAILURE ANALYSIS ENGINEER?

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MISSION STATEMENT OF FA

Failure analysis (FA) is an activity that serves to improve business and minimize losses for a company and its customers. The core business of FA is to *solve problems* for our customers by identifying both the root cause of errors made in production or design and by suggesting actions to rectify that cause. All our other activities (developing new methods, buying/maintaining equipment, refining skills) are pursued solely as a means to further the core business goal of solving our customers' problems.

PHILOSOPHY OF FA

Failure analysts should strive to be masters of their craft. This means they should be skilled in applying multiple FA techniques and/or FA tools.

Failure analysis is a craft. The failure analyst applies his/her understanding of the IC together with skill in applying various FA techniques, which may imply using multiple FA tools, to bring the investigation to a successful conclusion.

The key ingredient in successful FA, apart from a solid theoretical background and a logical, inquisitive nature, is for the failure analyst to have access to a "toolbox" of techniques. The results of each of these assets can shed a new and different light on the problem. It is by combining the outcomes of these FA techniques, together with what is already known about the problem, that subsequent steps are guided toward the solution. Therefore, it is a requirement that a failure analyst, when fully trained, should be the master of a range of skills and tools and should be able to apply them judiciously to reach the end goal: solving the customer's problem.

Each technique shall be mastered by multiple failure analysts in the group. An analysis is conducted, as far as is practicable, by one analyst applying various techniques, rather than passing the problem from one "limited-scope" expert to another.

This second aspect to the philosophy means that multiple engineers and technicians must be trained in each technique. That is, for a well-run FA lab, there is no technique that only one person can perform. This applies to the major fault-localization and sample-deprocessing techniques.

This goal has three important beneficial effects:

- It results in the ability to discuss the approach and results with peers who are fully versed in the technique and who may suggest alternative

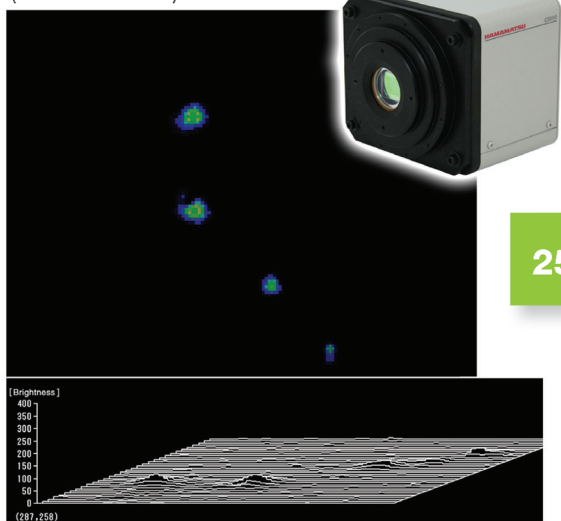
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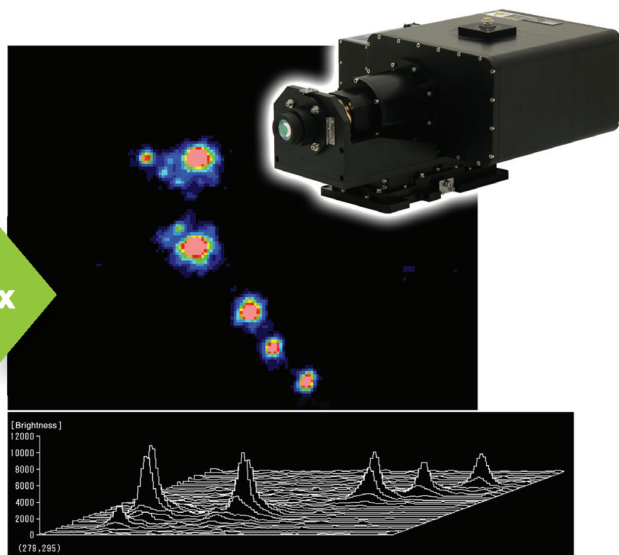
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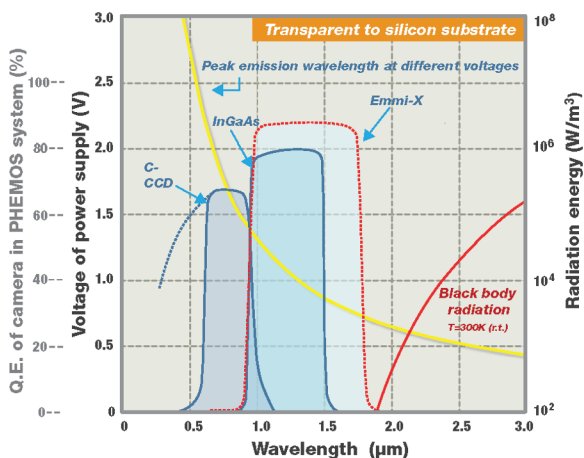
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HIGH-VOLTAGE CAPACITOR FAILURE ON A DOWNHOLE OILFIELD PCB

John Bescup, Weatherford
John.Bescup@Weatherford.com

INTRODUCTION

Often in technical discussions within the failure analysis community, passive components are overlooked in favor of novel analysis methods or emergent challenges to semiconductor reliability. However, passive components still occupy a vast amount of real estate in today's circuit designs and are not poised to disappear anytime soon. With that in mind, this article presents a case study of a failed high-voltage leaded-ceramic-chip capacitor that met its demise through an unlikely failure mode, which highlights the importance of well-trained operators behind the inspection equipment deployed to prevent latent defects.

DOWNHOLE APPLICATION

The capacitor to be examined in this article was intended for use in the high-vibration and high-temperature realm of oil drilling, which has a set of reliability concerns familiar to automotive and aerospace engineers. The components on these printed circuit boards (PCBs) will ride behind the drill bit, penetrating deep into the harsh environment of the Earth's crust, where they will help perform measurements to evaluate the rock formations around them. That information is communicated in real-time to engineers on the surface who are guiding the drilling string toward its intended target. Because of the abusive operating conditions and the harsh penalties for electronics failures, all components must be thoroughly vetted and their failure modes understood.

During the qualification of a new board design, a high-voltage ceramic-chip capacitor had failed by shorting itself. This part is rated for high temperature and has leads soldered onto its terminations with a high-melting-point solder. In many circuit designs, a single shorted capacitor may not influence the overall functionality and may escape completely undetected; however, this particular component played a vital role, directly impacting board functionality. Surprisingly, this part had already

“OFTEN IN TECHNICAL DISCUSSIONS WITHIN THE FAILURE ANALYSIS COMMUNITY, PASSIVE COMPONENTS ARE OVERLOOKED IN FAVOR OF NOVEL ANALYSIS METHODS OR EMERGENT CHALLENGES TO SEMICONDUCTOR RELIABILITY.”



undergone qualification studies on a different PCB with similar operating conditions and had been in use for some time. So, why had this particular unit failed?

EXTERNAL ANALYSIS

During electrical troubleshooting, a technician had identified a suspect appearance on the terminations of this capacitor. When the component was replaced with a brand new part, board functionality was restored and testing continued without incident. The failed component was given an initial optical inspection, which revealed two points of interest:

- Metal migration from the termination onto the capacitor face was observed from both sides of the part.
- The high-melting-point solder, which held the leads in place, had clearly reflowed and was showing heat-stress discoloration.

Both of these conditions can be seen in the optical images in Fig. 1.

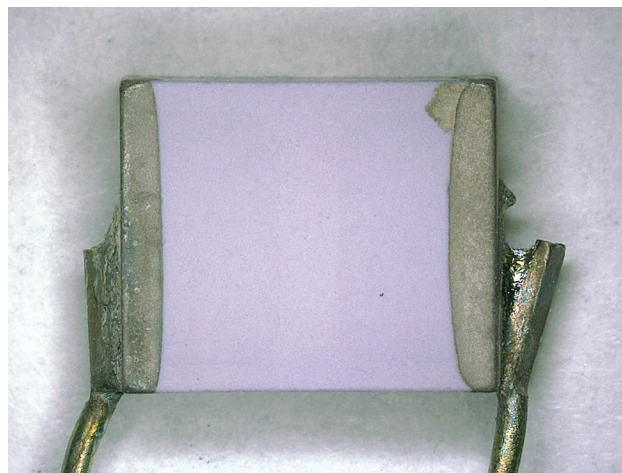
Metal migration via dendritic growth mechanisms is a threat particularly where high-voltage conditions exist, such as for this 2000 V capacitor. However, an examination of all sides of the capacitor quickly determined that the dendrite growth had not progressed far enough to create an external bridge between the terminations. To

determine the nature of the dendritic growth, energy-dispersive spectroscopy (EDS) was performed. By creating the series of element maps shown in Fig. 2, it was determined that silver had migrated onto the capacitor face. The other principal component of the termination material, palladium, had remained completely in place. As foreshadowing, note that the internal capacitor plates also contain silver.

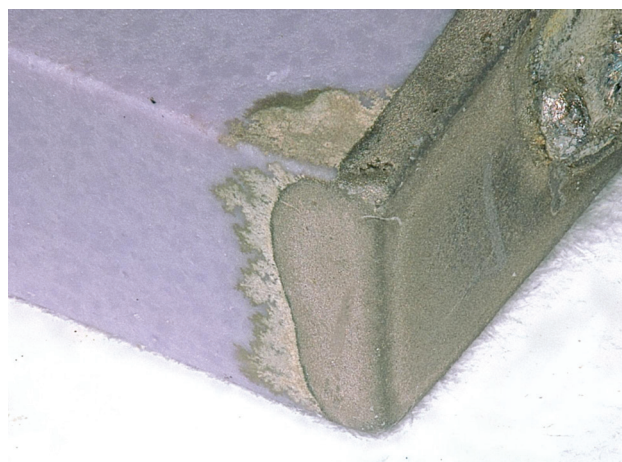
While the capacitor was in the scanning electron microscope (SEM) chamber, elemental quantification data were also gathered on the solder to verify that it had the intended composition. Because components in the oil-drilling industry are pushed into very extreme operating environments, a restriction of hazardous substances exception allows these boards to use leaded solder. A rectangular-area EDS spectrum acquired over the discolored area where the lead joins the cap termination showed 75/23 lead/tin, with the balance being silver. This is a close-enough match to the expected composition to rule out the possibility that the solder joint had been contaminated with a low-temperature solder during manufacture. Because component and PCB manufacturers who provide high-temperature assembly always offer low-temperature products as well, the possibility of inadvertently mixed solder alloys is a constant threat to reliability that must be guarded against. Consulting the tin-lead phase diagram, the liquidous point of 75% lead solder is just above 500 °F, so our termination certainly experienced some heat in order to discolor and partially reflow.

NONDESTRUCTIVE INTERNAL ANALYSIS

Before going further, it is necessary to understand a bit more about the construction of this particular component.



(a)



(b)

Fig. 1 (a) Optical image showing overall view of the failed capacitor. Note dendrite growth at upper right and the reflowed termination solder with heat-stress discoloration on the right side. (b) Closeup of dendritic growth from termination onto the cap face

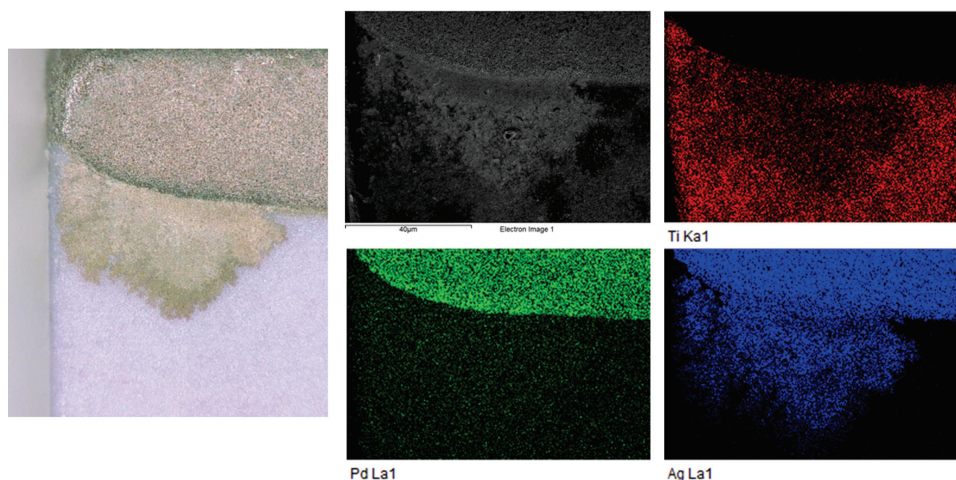


Fig. 2 EDS mapping of the dendrite growth. Starting at top-middle image and going clockwise: SEM grayscale image, red titanium map, blue silver map, green palladium map, and color optical image

Most capacitors use two sets of plates, with one connected directly to each termination. For high-voltage parts such as this one, manufacturers often add a third set of “floating” plates in the center of the part that are not directly connected to anything. This effectively creates two capacitors in series. The advantage of this arrangement is a little extra assurance that if a void or a particle of debris were present inside the capacitor dielectric, causing a short between the termination plates and the floating plates, there would still be another set of plates preventing the part from being completely shorted. Furthermore, to create a short on a capacitor built this way, it would be necessary for the left set of termination plates to bridge with the floating plates in the center and the right-hand set of termination plates to also be shorted with that *exact* same floating plate. Statistically speaking, the likelihood of this scenario is low. For this reason, the contention that this capacitor was shorted internally because of voiding-related plate bridging was viewed with strong skepticism.

Acoustic microscopy is often used by capacitor manufacturers to screen out parts that have been compromised by voids or debris in the dielectric material between plates. Although air is technically an insulator, voids in the capacitor dielectric can facilitate several failure modes that otherwise would not be possible. Migration of the plate metal can occur, as already seen on the outer surface, and humidity can condense under the high-temperature conditions in which this part will be operating. Most of the time, ultrasonic inspection is relatively straightforward and forgiving in the sense that even when parameters are not perfectly optimized, it is still possible to spot any notable defects. Among the many imaging modes available on a modern acoustic microscope, two time-tested methods will find nearly any defect in a typical capacitor: bulk scan and loss-of-back-echo (LOBE) scan. Because high frequencies of ultrasound cannot propagate through

air, even incredibly small pockets of air are very effective at reflecting an ultrasonic signal sent into the capacitor. The LOBE technique uses this concept to advantage by depicting the shadows where the ultrasonic signal was blocked when the microscope captures a backside image of the part. In this way, features such as diagonal cracks, which scatter the sound without returning it to the transducer, can still be spotted. So, the name of the imaging mode describes exactly how it works: Any echo that is lost by the time it reaches the back surface of the part tells the operator something. The LOBE scan in Fig. 3(a) shows a few dark areas, which can be checked against forthcoming scans.

The other main inspection method used to search for defects in cap dielectric is bulk scan, where the image is generated by only those reflections originating from inside the part, purposely excluding the front and back surface reflections. In this imaging mode, bright reflections represent air gaps inside the bulk of the dielectric. Figures 3(b) and (c) show two bulk scans of the shorted capacitor. When creating these images, the transducer is typically focused halfway between the front and back surface, which, in this case, was measured to occur at a time of flight (TOF) equal to 13.9 μs . However, when this accepted convention is used, the resultant image shows no voids at the locations indicated by the LOBE scan. After repeating the scan with a higher and lower TOF, the operator discovered that different sets of voids were revealed, depending on the transducer focus. The particular combination of materials used in this dielectric material is restricting the acoustic depth of field. This is not normally the case, and it gives a plausible reason why acoustic inspection at the time of manufacture may have missed a set of voids that did not appear when the acoustic microscope was configured according to customary settings for bulk scan inspection. The image in Fig. 3(c), which was created with a TOF equal to 10.2 μs , reveals

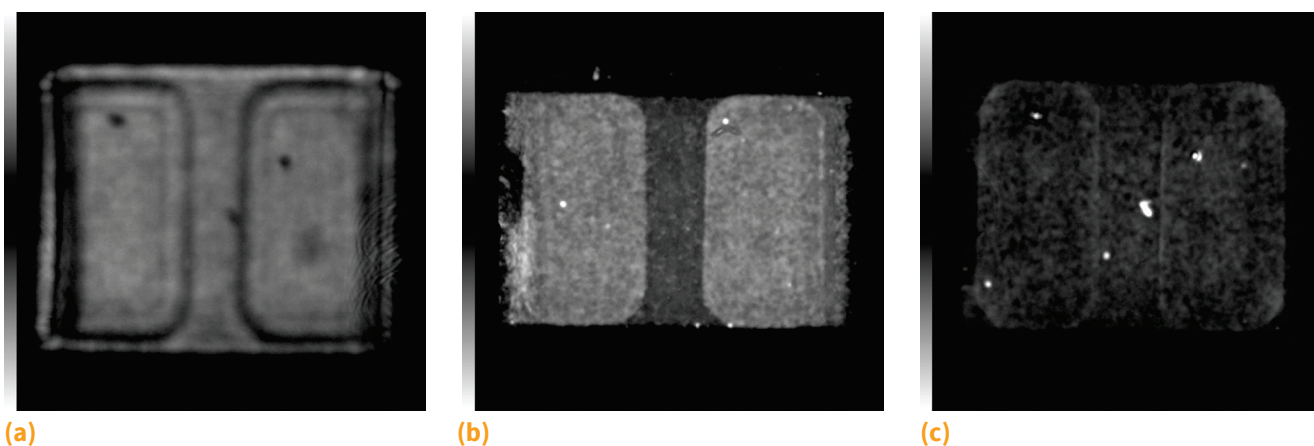


Fig. 3 (a) LOBE acoustic image. (b) Bulk scan acoustic image with TOF at 13.9 μs . (c) Bulk scan acoustic image with TOF at 10.2 μs

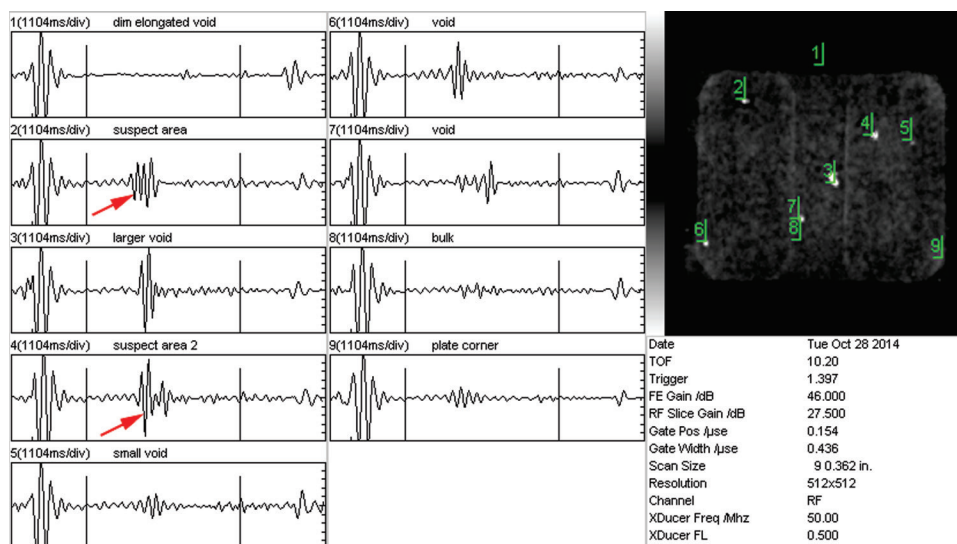


Fig. 4 Acoustic waveform capture displaying many points of interest. Red arrows highlight echoes from two voids at a nearly identical depth from opposite sides of the capacitor.

a set of voids where dark shadows in the corresponding LOBE image (Fig. 3a) had indicated. Two of these will be of particular interest moving forward.

As mentioned previously, to create a short between two terminations, there must be a short path from both terminations to the same center plate. To determine if this scenario were possible with the voids seen in acoustic imaging, a closer examination of the waveforms used to build these images is needed. The image in Fig. 4 shows a variety of waveforms sampled from the failed part. Red arrows on the waveform from positions 2 and 4 point out echoes from two voids at the same position in time, which also corresponds to depth in acoustics. These two voids also have an unusual appearance, with dark halos surrounding them, which increases interest in them. X-ray inspection was also performed on this capacitor, although as an inspection method it is better suited for finding large cracks beneath the terminations, where acoustic

microscopy has difficulty seeing. In this case, nothing noteworthy was found via x-ray, so the decision was made to proceed with cross sectioning and finding out exactly what acoustic inspection had seen.

CROSS SECTIONING AND SEM ANALYSIS

Using the acoustic images as a guide, the failed capacitor was cross sectioned to obtain a direct look at the two suspect voids and to verify which plates they contacted. A composite optical image shown in Fig. 5 depicts both voids, although they were not physically visible at the same time because of the direction of the cross sectioning. In this image, a blue line has been superimposed along the length of one of the floating plates to illustrate that, indeed, both of these voids make contact with the same floating plate.

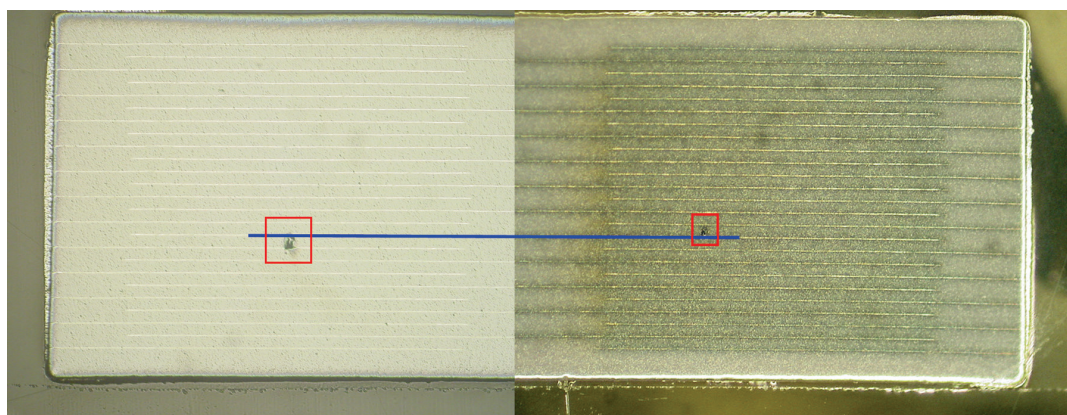
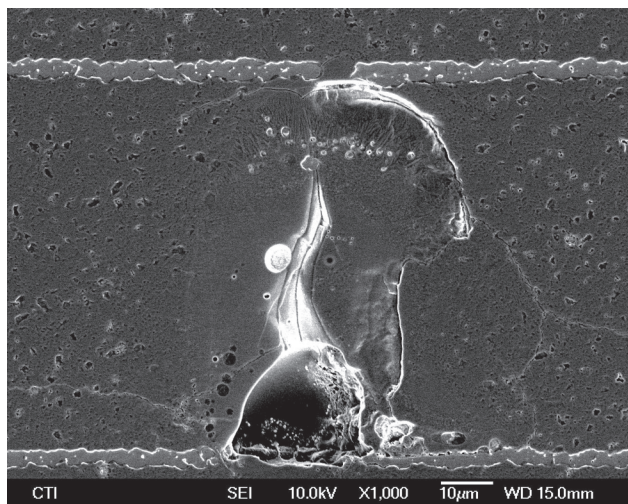
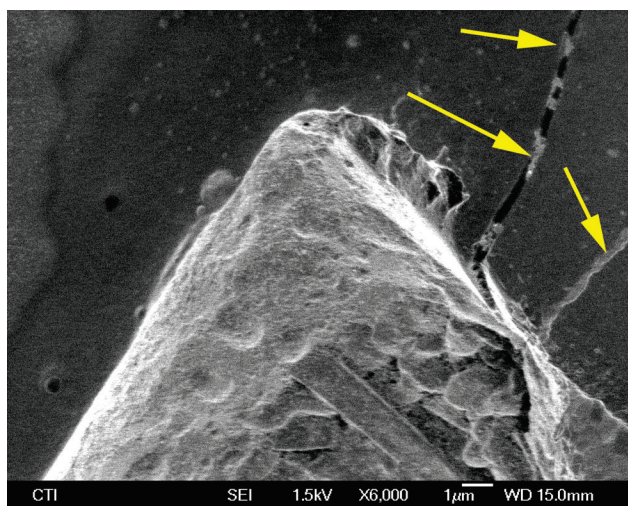


Fig. 5 Composite optical image showing cross-sectioned views of the two voids previously identified by acoustic inspection. The voids are highlighted with red rectangles; a blue line traces the connection to the center floating plate that these voids share.



(a)



(b)

Fig. 6 (a) SEM closeup showing a void that stretches completely between a termination plate and a floating plate. (b) SEM closeup with yellow arrows highlighting metal migration within cracks that extend from the larger void cavity between plates

To inspect the voids at higher magnification, the SEM was used. A detailed view of the void from the left half of the optical view is shown in the SEM image in Fig. 6(a). In close-up images, it can be noted that the capacitor plate material has either melted or migrated into the air gap in the dielectric material. As previously noted, silver—a major component in the plates—can certainly migrate, as the EDS inspection showed. Both voids had a network of fine cracks extending from the air cavity, likely induced by expansion and contraction as the part was exposed to high

temperature during testing. Although these cracks are small in scale, the metal from the plate material is clearly seen filling in these cracks, as noted by the yellow arrows in Fig. 6(b). This metal ultimately created the electrical pathway that led to the capacitor failure.

SUMMARY

After investigating the capacitor with a variety of methods, it was seen that internal shorting via silver migration was the failure mode. It is believed that this was a latent defect caused by voids in the dielectric that had been present from the time of manufacture. Through some combination of time, electric potential, trapped humidity, and elevated operating temperature, the plate material migrated into these voids and created a short path to the same floating plate. Acoustic imaging proved to be the best method for detecting the point where this failure had occurred, although it was also clear that, in this case, a single-pass inspection with the conventionally accepted parameters was not able to find the voids of interest.

ACKNOWLEDGMENT

The author would like to thank his colleagues Fardin Farzaneh, Chris Yarbrough, and Bobby Hooghan for all their assistance.

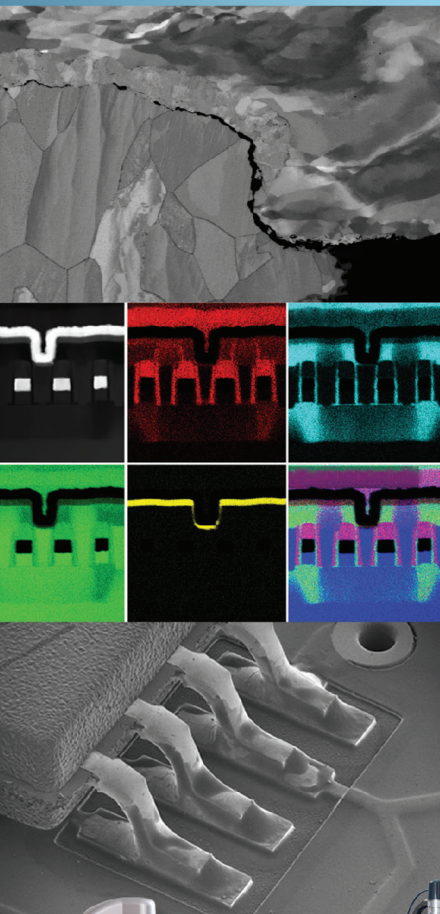
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John Bescup is an electrical engineer for Weatherford. He has more than 10 years of failure analysis experience, with an emphasis in acoustic imaging. His day-to-day routine includes diagnosing a variety of nonfunctional hardware, covering the gambit of failure analysis

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TAKE A CLOSER LOOK AT ELECTRICALLY-ENHANCED LADA: SETUP

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INTRODUCTION

On sub-28 nm process technology, silicon patterning conformance to design, especially front-end-of-line, has run up against the limits of physics, bringing about a paradigm shift from defect-limited hard failures to increasing occurrences of design-margin soft failures as a result of the shrinking process window. Therefore, the role of soft defect localization (SDL) techniques in yield engineering has become more important. It is common to speak of SDL and laser-assisted device alteration (LADA) when such failures need to be investigated.

LADA uses a continuous-wave 1064 nm photo-current-inducing laser to temporarily alter transistor characteristics through the silicon substrate. The outcome is a flip in the tester pass-fail state. The position of the scanning laser is correlated to the state transition and registered for signal image acquisition.^[1] Such an approach is well known to be effective for localization of speed path degradation^[2] and subtle process defects.^[3] The application of LADA extends beyond such spatial localization with the innovation of time-resolved LADA (TR-LADA), which is capable of extracting temporal information from the failures by using a 1064 nm pulsed laser to “probe” different test cycles in each test loop.^[4] It offers new insights, such as failure mode identification^[5] and knowledge of propagation delays.^[6] In some cases, an improved LADA signal spatial resolution has also been observed.^[7] The current state-of-the-art in TR-LADA is based on a 50 ps pulse-width laser that enables the interrogation on a single test cycle. As a matter of fact, both LADA and TR-LADA signals can be attributed to either potential sites of existing issues or devices with low threshold to laser stimulation, the latter also known as artifacts. There is no means to intuitively differentiate between the two by merely monitoring the transition of test pass-fail states. This is the main motivation behind the innovation of electrically-enhanced

LADA (EeLADA).^[8,9] It works by the concept of eliminating these artifacts by extracting fail information from all LADA events in terms of failing pins/cycles and comparing them against the actual fail information derived from testing the bad unit.^[7] In this way, only the LADA signals relevant to the actual failure will be displayed. This methodology also presents an advancement that overcomes LADA’s traditional limitation on soft failures and creates new possibilities for hard failure defect localization. The concept of EeLADA can be realized in a number of ways, and two such approaches will be discussed.

WHAT IS ELECTRICALLY-ENHANCED LADA?

Figure 1 shows a block diagram illustrating the EeLADA concept. In general, although the setup refers to a wafer-level configuration, it applies to package level as well. Unlike a typical synchronous LADA setup where the tester generates a trigger in the event of a flip in the test state, EeLADA integrates an additional comparator module to determine the trigger pulse generation. The integrated circuit (IC) device under test is activated by the tester, which refers to the test pattern for the biasing conditions. A test pattern is defined by a three-dimensional matrix of test vectors that correspond to specific pin names and cycle numbers. The test vectors may represent inputs or outputs. Inputs serve as driving signals into the IC, and outputs, also called compare test vectors, provide the expected states to determine a test pass-fail.

Prior to debug on EeLADA, the bad IC is tested, and a standard failure log containing details of the compare fail vectors and the respective fail pin/cycles is obtained. This is referred to as the reference failure log, as shown in Fig. 1, and is called the reference failure signature. The comparator module receives this fail log and commits it to memory. As the tester activates the soft failing IC and the

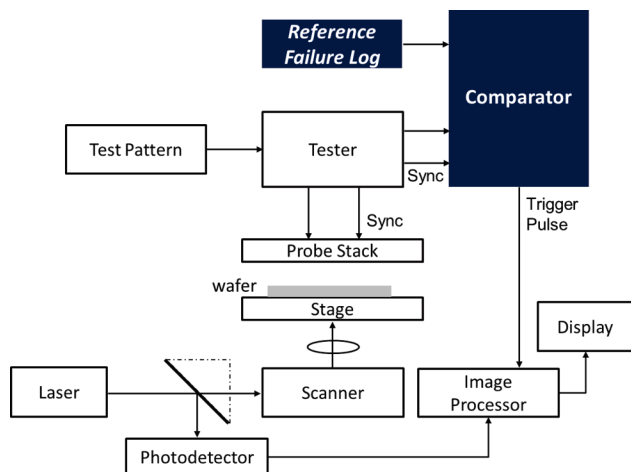


Fig. 1 Block diagram of EeLADA concept

laser stimulates the region of interest, the test outcome is compared against the reference failing signature at each pixel. In the event of a match, a trigger pulse is generated by the comparator module and sent to the image processor. This is how LADA signals that are not directly relevant to the reference failing signature are negated on the display.

HARDWARE APPROACH

Figure 2 shows a block diagram illustrating a hardware implementation of EeLADA. As apparent in the earlier section, the essence of the concept lies in the realization of the task of the comparator logic. A first-in-first-out (FIFO) buffer array of sufficient depth functions as the memory to capture the reference fail signature. Electrical channels on the prober interface board that relate to the failing pins (based on the reference fail signature) are wired out and passed into another set of FIFO buffer arrays to capture the pin output state at each test cycle. A pulse

that is generated by the tester within each test period synchronizes a counter with the test cycle. The counter increments the shifting of the FIFO arrays and coordinates the comparator logic circuit to access the FIFO states at the failed cycles for matching. As an illustration, a passing IC is tested, and waveforms captured at the points labeled “A” (tester pin output) and “B” (signal into counter) are observed on an oscilloscope. An example based on a few test cycles is shown in Fig. 3. An instance of a test cycle is denoted by a bounding box, and the arrow indicates the expected compare vector (H). The output pin attains a voltage high, which is correct.

The results of another simple experiment accomplished on memory built-in self-test are presented in Fig. 4. The sample under test is a good IC. Figures 4(a) and (b) show the LADA and EeLADA signals, respectively, on three embedded memory arrays. With selective pin/cycle matching, only one of the memory arrays is revealed,



Fig. 3 Synchronizing signal and output pin waveforms viewed from an oscilloscope

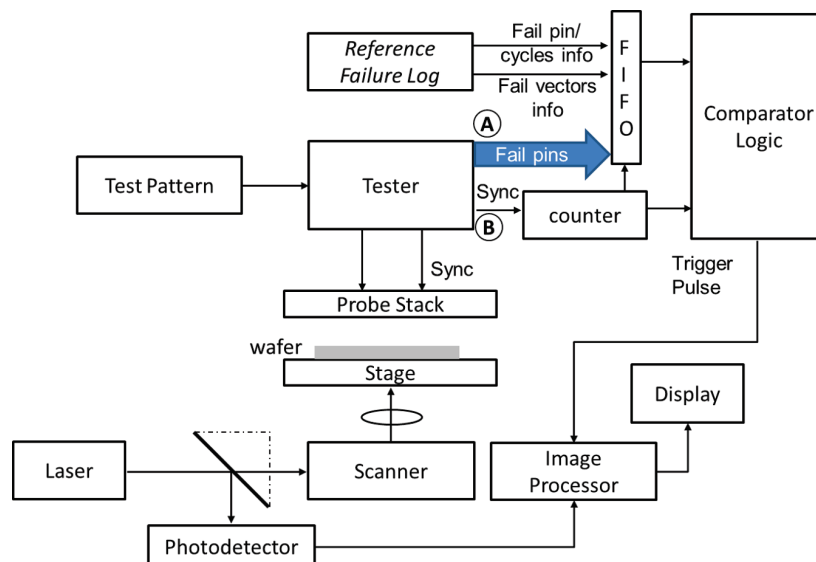


Fig. 2 Hardware implementation of EeLADA

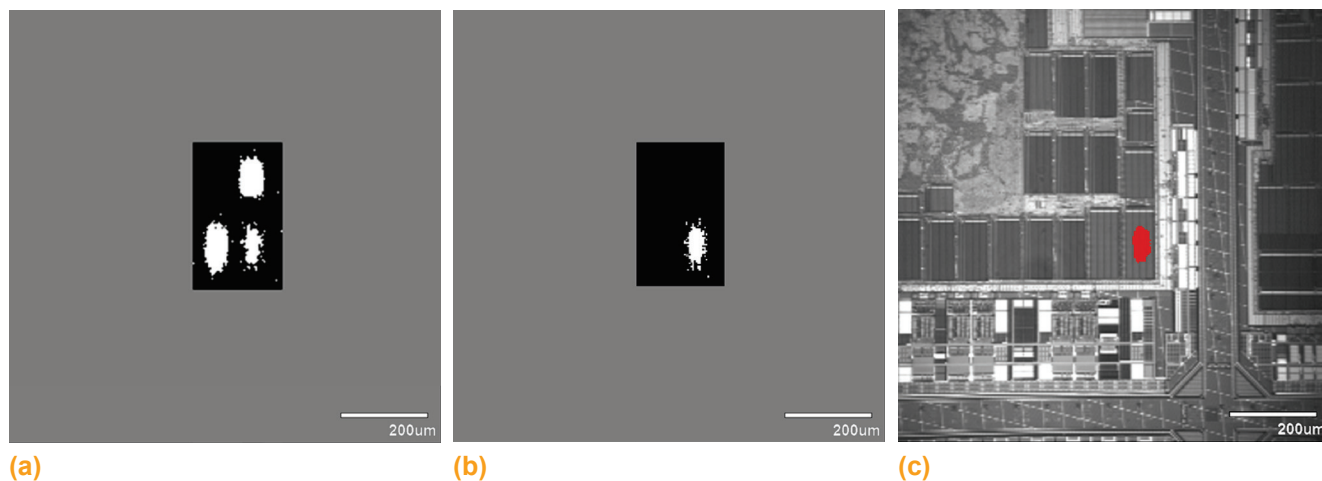


Fig. 4 (a) Conventional LADA signals. (b) EeLADA signals. (c) Overlay image

with the rest “electrically filtered.” Figure 4(c) shows the overlay image. This result demonstrates the feasibility of the technology.

Additionally, it should be noted that the criteria for matching can be determined by the user. For example, a trigger pulse can also be generated as long as one of the current fail vectors matches to any of the failed vectors in the reference signature. In this case, more signals are expected to be observed in the image as compared to an exact match, because the comparison scheme is less stringent.

SOFTWARE APPROACH

Another approach to realize EeLADA is illustrated by the block diagram in Fig. 5. Unlike the hardware approach, there is no comparator logic involved to assess a match situation. Instead, a graphical user interface (GUI) receives the original test vectors as well as details of the failing signature to generate a technical test pattern dedicated for defect localization. To explain the methodology,

consider a simple case of a failure signature consisting of only a failed vector that corresponds to a certain fail cycle and pin. Assuming this specific compare vector is failing, a “High” is expected; that is, it attains a “Low” on the test. The original vectors that correspond to the failing signature are inverted. In this case, instead of expecting a “High,” the test now expects a “Low” for this compare vector to pass. Therefore, the test will fail by default when the technical test pattern is employed. As the laser induces LADA signals that give rise to failing compare vectors other than the inverted vector, the test state remains unchanged. Conversely, when the LADA signal matches the failing signature, there is a state change to pass, and a match trigger signal is provided directly from the tester to the image processor. Similar to the hardware implementation, the match criteria are, in fact, controllable. In this approach, they are determined by the way the original pattern is manipulated to produce the technical pattern. Figure 6 shows a screenshot of the GUI dashboard. The UI enables a user to provide inputs to manipulate the original

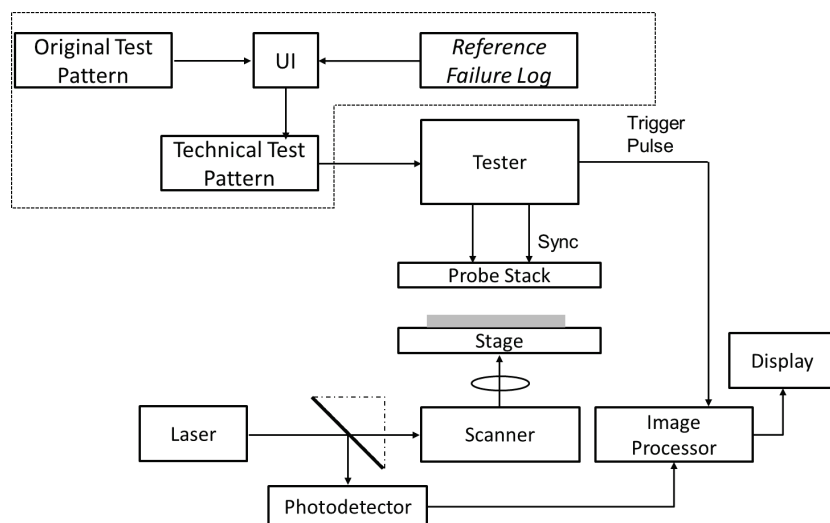


Fig. 5 Block diagram representing software implementation of EeLADA

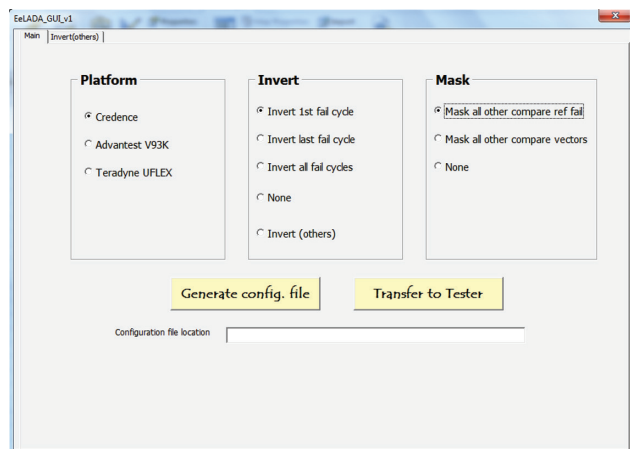


Fig. 6 EeLADA software implementation graphical user interface

pattern based on the failure signature. A configuration file is then generated out of the UI and transferred to the tester to execute the process. There are three selection panels on the GUI for user inputs. The tester platform determines the format of the configuration file. Fundamentally, there are two steps involved in manipulating the compare vectors in the original pattern. First, the user may choose whether to invert all or partially invert the compare fail cycles according to the failing signature. The last option is to execute no vector inversion. In the second step, the mask select option enables the user to mask out the remaining compare fail vectors (within the reference failed vectors but not inverted in the first step), the remaining compare vectors (not a part of the reference failed vectors), or not mask anything.

Vectors invert	Vectors mask	None	Mask all other compare vectors (within ref. fail)	Mask all other compare vectors (not within ref. fail)
Invert all fail cycles				
Invert selective				
Invert 1 st fail cycle				
Invert last fail cycle				
None				

Most stringent Least stringent

Fig. 7 Variations of technical test pattern

		IO pins					
		A0	A1	A2	A3	A4	A5
Cycles	1	H	L	L	L	H	H
	2	H	L	H	H	H	L
	3	L	L	H	H	L	L
	4	H	H	L	H	L	H
	5	L	L	H	H	H	L
	6	L	H	H	L	L	H
	7	H	L	L	H	H	H

(a)

		IO pins					
		A0	A1	A2	A3	A4	A5
Cycles	1	H	L	L	L	H	H
	2	H	L→H	H	H	H	L
	3	L	L	H	H	L	L
	4	H	H	L	H→L	L	H
	5	L	L	H	H	H	L
	6	L	H	H	L	L	H
	7	H	L	L	H→L	H	H

(b)

		IO pins					
		A0	A1	A2	A3	A4	A5
Cycles	1	H	L	L	L	H	H
	2	H	L	H	H	H	L
	3	L	L	H	H	L	L
	4	H	H	L	H	L	H
	5	L	L	H	H	H	L
	6	L	H	H	L	L	H
	7	H	L	L	H	H	H

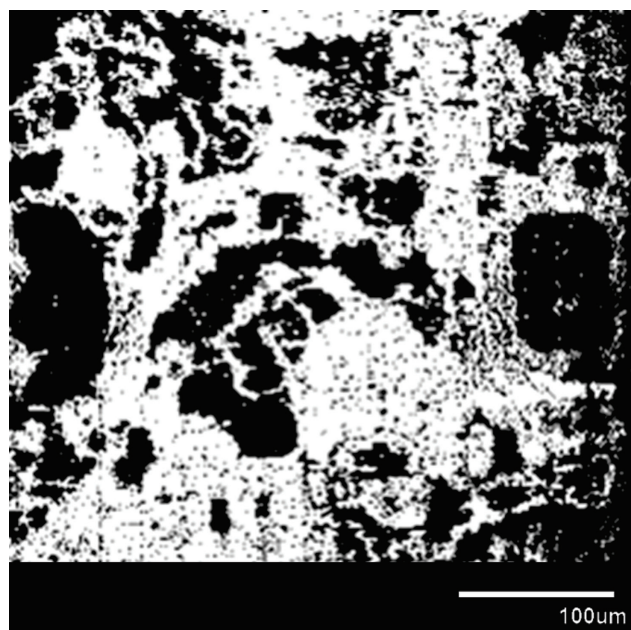
(a)

		IO pins					
		A0	A1	A2	A3	A4	A5
Cycles	1	H	L	L	L	H	H
	2	H	X	H	H	H	L
	3	L	L	H	H	L	L
	4	H	H	L	X	L	H
	5	L	L	H	H	H	L
	6	L	H	H	L	L	H
	7	H	L	L	X	H	H

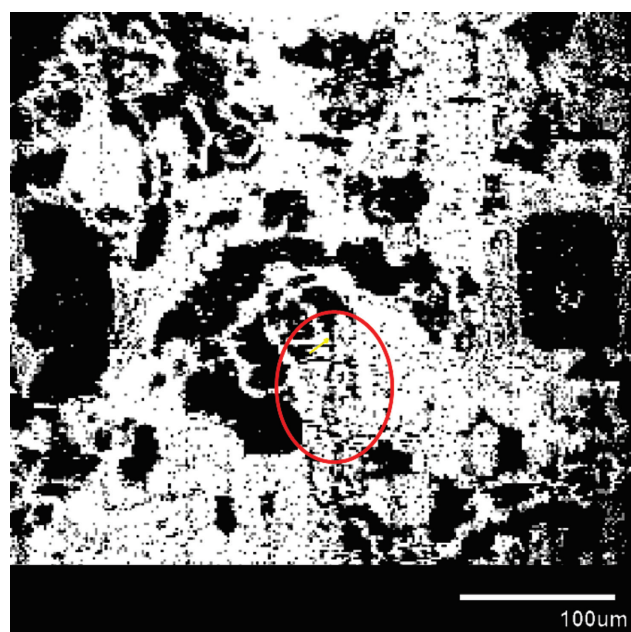
(b)

Fig. 8 (a) Most-stringent and (b) least-stringent technical test patterns

Figure 7 presents a matrix defining the different variants of compare vector manipulation and their corresponding stringency. As an illustration, Fig. 8(a) and (b) show the case of the most- and least-stringent scenarios, respectively. The compare vectors highlighted in red are failing on a bad IC. Following the most-stringent match criteria, all these compare vectors are inverted in the technical pattern. This is the case described in the beginning of this section. To demonstrate the methodology, the same experiment that was performed earlier following the hardware approach is repeated, but this time applying the software approach. The EeLADA



(a)

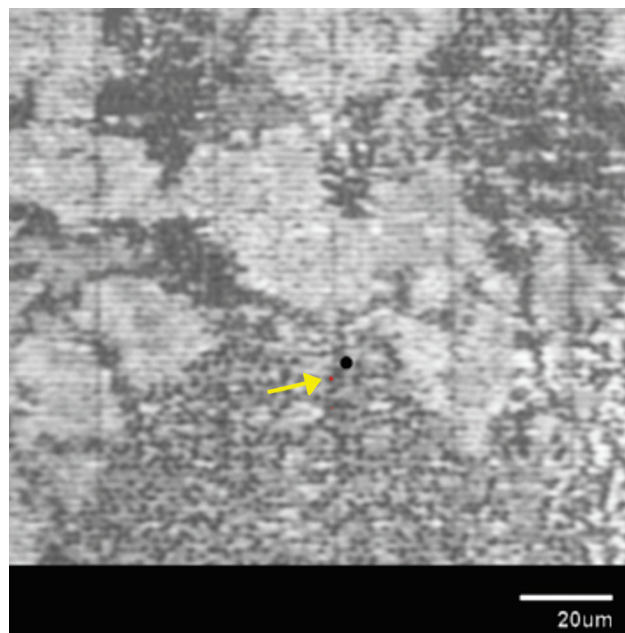


(b)

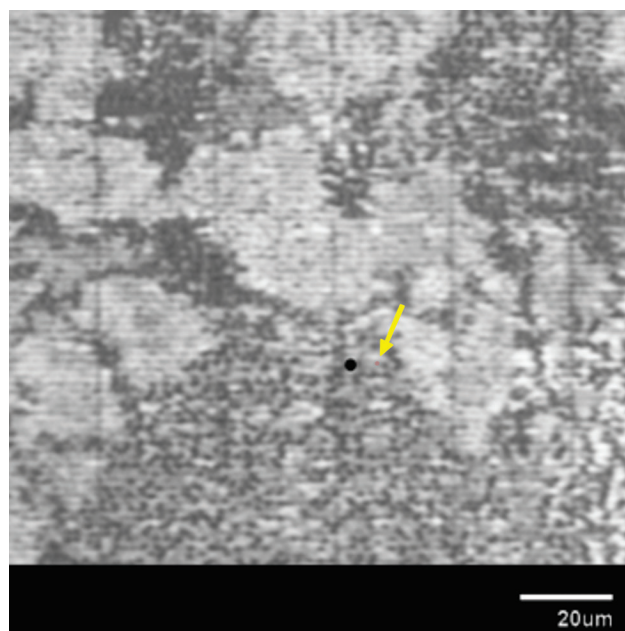
Fig. 9 (a) Conventional LADA signals. (b) EeLADA based on least-stringent technical test pattern

signals obtained are similar to Fig. 4(b). This validates the method.

Consider the least-stringent case next, using another experiment based on some random logic of an IC. The compare vectors are masked in the technical pattern according to a failed IC's failure signature, and the EeLADA signals acquired on a passing IC are shown in Fig. 9(b). Figure 9(a) shows the conventional LADA signals (pass-to-fail state transition) acquired using the original test pattern for comparison. Some signals appear to be missing



(a)



(b)

Fig. 10 EeLADA signal overlay images based on (a) first fail cycle and (b) last fail cycle invert technical test pattern. The black dot denotes the location of a programmed defect. Arrow points to signal.

in Fig. 9(b), because laser stimulations at these locations do not result in a fail. This is the effect of masking the compare vectors.

Another experiment was performed by creating a programmed defect in the active area of some random logic using a 1340 nm wavelength laser through the silicon substrate. The device is tested, and the fail log is collected. Figure 10(a) shows the EeLADA overlay image for the case of inverting only the first fail cycle of the failure signature, and Fig. 10(b) shows the case of inverting the last fail cycle on the technical pattern. It should be remembered that EeLADA is performed on a passing IC. The black dot denotes the exact programmed defect location. The arrows pinpoint the EeLADA signals. It is evident that although the signal does not precisely coincide with the defect, the observation within the vicinity of 10 μm is sufficient to guide and achieve physical failure analysis success on the bad die. The results from this experiment demonstrate the potential of employing EeLADA for hard defect localization. More comprehensive studies are necessary in this aspect.

HARDWARE VERSUS SOFTWARE APPROACH

While both hardware and software approaches are able to realize the concept of filtering LADA signals, it is worth highlighting again that the manner of operation is significantly different. The latter method is not as straightforward, but the outcome is congruent, as evidenced earlier. The idea of matching is more intuitive by using the comparator circuit. For EeLADA inspection time, the hardware approach has a slight advantage, because the dwell time per pixel is shorter since it is no longer necessary to incorporate wait times for the accommodation of synchronizing and pass/fail pulses in a single test loop. However, the flipside in this method lies in the use of cables that may not be suited for IC testing speeds above 50 MHz.

ABOUT THE AUTHORS



S.H. Goh received his B.Eng. and Ph.D. degrees in electrical and computer engineering from the National University of Singapore. His doctorate research on simulation and implementation of the aplanatic refractive solid immersion lens was awarded a conference Best Paper and was part of a team project that received the 2009 Singapore President's Technology Award. Dr. Goh is currently with Globalfoundries, Product, Test, and Failure Analysis Division, Singapore, where he leads a team responsible for product failure diagnostics and advanced methodologies to accelerate yield ramp. His main focus is on development of dynamic fault isolation techniques, wafer-level fault isolation methods, and leveraging cross-functional domain knowledge of design, test, and failure analysis to enhance yield learning. His work has been published in conference proceedings and journals. Dr. Goh is also an active contributor to IPFA and ISTFA technical committees.

CONCLUSION

Whenever a LADA event occurs due to a state transition from fail to pass, the signal relevance to the exact failing signature is obvious. However, the reverse is not true. Therefore, signals that arise from a pass-to-fail state transition are more concerning. Normally, they can involve various combinations in terms of failing pins and cycles, be it conventional LADA or TR-LADA. EeLADA is an evolution that resolves this ambiguity to extract relevant signals for analysis. The fundamentals behind EeLADA have been detailed in this article. Although EeLADA appears to be a derivative of LADA, in practice, EeSDL will work as well. As a final takeaway, it is worth a moment to pause and review the custom way IC failures are debugged. Should defect localization always be performed directly on failed dice? The preliminary demonstration of the EeLADA application to hard defect localization is an exemplary example of deviating from this rule of thumb.

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B.L. Yeoh graduated from the University of Technology, Malaysia, with a B.E. degree in electrical engineering. In 2006, he joined Intel Microelectronics Malaysia as a failure analysis engineer, where he specialized in memory testing and failure analysis during his five-year tenure. He is currently employed as a Member of the Technical Staff at Globalfoundries Singapore. His field of interest focuses on device fault isolation using a wide range of industry-standard electrical failure analysis tools, such as photon emission microscopy and laser scanning microscopy techniques (OBIRCH, TIVA, dynamic laser stimulation, etc.). His current research interests focus on exploring soft defect localization and laser-assisted device alteration techniques for different failure-type diagnostics in the semiconductor industry.

G.F. You holds a B.S. degree in physics from Fu Dan University, China; an M.Eng. degree in electrical engineering from Nanyang Technology University, Singapore; and a Ph.D. degree in the same field from the National University of Singapore (NUS). Currently, he specializes in wafer-level tester-based failure debug in Globalfoundries' Product/Test and Yield Engineering Department, Singapore. His experiences include dynamic fault isolation techniques, such as frequency mapping and soft failure localization. Prior to joining Globalfoundries, Dr. You worked as a research fellow at NUS.



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MANAGEABILITY CHALLENGES FOR INTERNET OF THINGS

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There is no longer much argument around the Internet of Things (IoT) concept as the “next big thing,” but consensus remains elusive around the next level of questions and discussion: Why is the IoT going to be so great, and what are the obstacles to achieving that vision?

The IoT is already delivering valuable benefits in the nascent stage of its development. However, I would argue that “IoT Version 1.0” has not yet been realized, and the magnitude of this revolutionary innovation will not become clear until then.

Getting to that point will require addressing a variety of user pain points, perhaps the most glaring of which is device failure. Mainstream adoption of and reliance on the IoT demands a scenario in which one or more disparate devices may fail but the overall system continues to function. Perhaps the system would not function as well as when the failed devices were operational, but it would continue. In the meantime, the failed device could be recognized and repaired without the user experiencing a disruption in service and with a return to optimal system performance.

In addition to more functionally reliable devices, IoT 1.0 will require an intelligent middleware layer for multivendor device management. Achieving such a layer will require global collaboration across the IoT’s diverse stakeholders.

WHEN WILL THE IoT REALLY BE THE IoT?

I began working on the IoT six years ago, and at that time, I didn’t have a clear definition of what the IoT is or would be.

Even today, different people have different definitions of the IoT. For some, the IoT is having things connected to a smartphone and enabling capabilities such as remotely locking/unlocking the front door. For others, the IoT is having a device connected to the internet, streaming data to the cloud, and having the cloud perform intelligent analytics to help humans make intelligent decisions. However, such definitions are still predicated on the notion of a small number of devices connected through the internet to individual humans, who, at the very least, are kept in the loop for all the real decision-making.

My definition of the true IoT—IoT 1.0, if you will—is when heterogeneous, multiple connected devices are working together to our benefit and without us having to make all of the decisions (Fig. 1). The IoT will deliver more benefits with more and more devices working together without human interaction, which both naturally impedes IoT scalability and adds complexity to our lives.

For example, mental wellness is an area that especially interests me. In the IoT 1.0, devices that measure various bio signals, such as heart rate and temperature, could be




Description	Stages	Examples
Device that can be connected to the smartphone	IoT 0.5	
Intelligent decisions are made (in the cloud mostly)	IoT 0.9	
Heterogeneous, multiple connected devices are working together	IoT 1.0	

Fig. 1 When heterogeneous, multiple connected devices are working together without humans making all of the decisions, we will attain IoT 1.0.

in used in combination with other intelligence to better understand a person's mental as well as physical health state in relation to various stress factors. If a wearable sensor was linked with the user's calendar, the system may be able to connect the dots and realize that the reason a user is stressed is because there is a key meeting coming up in 15 minutes. Without the link to the calendar, while the device may be able to do numerous measurements of the human body, the overall system would not have any context for the results.

Another compelling use for the IoT 1.0 vision is the capability for devices to work together through the system to make someone (like me) more comfortable on a day when they are ill. Perhaps a device would note that my skin temperature is rising, detecting a fever, and know that I prefer a warmer room when I am feverish. With the IoT 1.0 providing a link between the device monitoring my temperature and the devices regulating climate control in my home, the system could adjust my environment to make it more comfortable without any direct interaction from me.

With the notion of multivendor, heterogeneous devices linked to one another and able to act in concert, the benefits of the IoT 1.0 for humans become quite easy to imagine. For example, we all have numerous keys, and many of us have garage-door openers, but do we really need these things in the emerging IoT world? Could a system recognize us and let us into our homes securely and conveniently without a key or garage-door opener? It would be great if, when my car approached the driveway of my home, the system sensed my approach and automatically opened the garage door. When I leave the house, it should be able to close the door, lock it automatically, and turn on the home-security systems, because it knows I am gone.

Across security and access control, utility management

“MY DEFINITION OF THE TRUE IoT—IOT 1.0, IF YOU WILL—IS WHEN HETEROGENEOUS, MULTIPLE CONNECTED DEVICES ARE WORKING TOGETHER TO OUR BENEFIT AND WITHOUT US HAVING TO MAKE ALL OF THE DECISIONS.”



(lighting, electric vehicles, energy efficiency, garden and home appliances), healthcare and assisted living, audio/visual services, entertainment, and so on, the benefits to such a vision of the IoT are clear. However, challenges must be addressed to achieve an IoT 1.0 in which heterogeneous, multiple connected devices work together to my benefit without me controlling everything.

The single most problematic set of pain points inhibiting realization of the IoT 1.0 vision today may be device failures. Communication and battery issues can undo whole systems and their potential benefits. Plus, there's usually a limited user interface for debugging. Without a better solution for managing and adapting to device failure, the IoT will continue to be more of a technological novelty or curiosity than a major underpinning of daily life around the globe.

MY IoT@HOME

I recently counted over 100 commercially available connected devices in my house. *One hundred!* Presence sensors, motion sensors, electronic lock, lighting control, water sensors, garage-door opener, cameras, sirens, smart meters, smoke detectors, and so on (Fig. 2). For example, I have a very heavily connected and guarded front porch: four cameras, three motion sensors, three infrared lights,

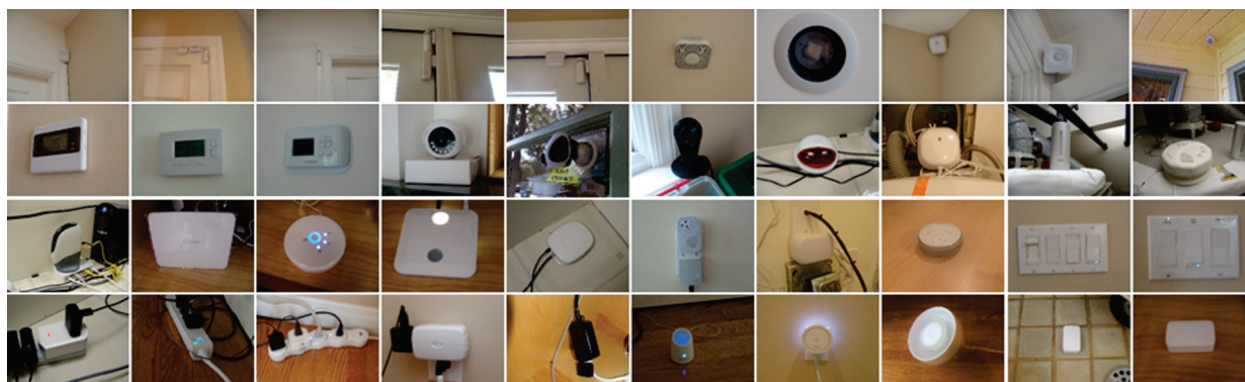


Fig. 2 In my IoT@Home, apps and devices provide benefits, but such a large number of devices creates the issue of device failure, which requires a significant amount of debugging time.

and three open/close sensors. In addition, I use more than 20 apps in my home.

So many devices and so many apps unquestionably bring me a great deal of personal benefit; however, so many devices and apps create issues, too. The biggest challenge I face in my personal “IoT@Home” is that I constantly need to fix one thing or another. Each device has an approximate average failure rate of once per year. So, if just one device fails per week, that leaves me in a regular mode of debugging my system, and that keeps me really, really unhappy.

Device failures currently comprise a problem with only 100 devices in my home, but what happens when the forecasts for IoT proliferation come to pass and I have 300 or 400 connected devices in my home? Most home users simply are not interested or are incapable of dealing with each individual fault across devices in a system that is so quickly growing in complexity, interconnectivity, and the sheer number of devices.

TOWARD A SOFTWARE-DEFINED IoT

Implicit in the issue of device failures are at least a couple of calls to action for the industry that is building out the IoT 1.0 around the world. Device manufacturers can strive to make more-reliable devices, and, of course, they already are and always will be striving to do so. Certainly, this is a necessary pursuit.

However, even if devices are made more reliable, the truth is that some rate of device failure is inevitable. The IoT 1.0 will deliver its greatest benefits when users are able to experience the IoT while remaining almost naïve to the applications and devices that enable the experience. The system should still be able to operate, even when individual devices run into a faulty state.

This need tees up the requirement for an intelligent middleware to minimize human effort and automatically monitor and control the overall system, recognize individual failures, and hand over capabilities among devices as necessary. There needs to be an intelligent mapping of devices within the virtual space of the IoT 1.0. This cyber-physical intersection will be critical to a resilient system.

At the Intel-NTU Connected Context Computing Center, for example, we are working on a proactive management framework, “WuKong,” that works to limit IoT user interaction to simply sending requests to applications and defining context and high-level policy. The new middleware layer intelligently maps the logical relationship to physical devices, and, when devices fail or are replaced, the middleware automatically re-maps a logical relationship to the physical devices (Fig. 3).

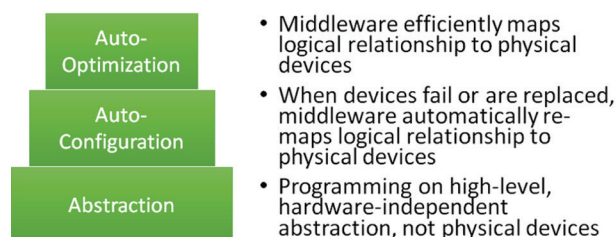


Fig. 3 Middleware will enable a software-defined IoT, minimizing human intervention.

Furthermore, programming is performed on high-level, hardware-independent construction—not the specific physical devices—so that programs can be written once and then run everywhere across the IoT. Moving the devices/services around becomes easier. Finally, if the user’s intention is properly communicated to the middleware, then the user should not be concerned with finely adjusting the device sensitivities.

Sensitivity is another area of pain. For example, today a motion sensor set too sensitive on my front porch may detect a car passing on the street in front of my home and trigger useless picture-taking by my home-security system; the same motion sensor set not sensitive enough may ignore someone walking on my front yard. With a better, more intelligent middleware that understands the security goals of the user, the middleware should make sensitivity decisions per device based on the user’s greater system-level intention, as opposed to simple, preset thresholds for each device.

Such a middleware layer is being designed ultimately to enable a software-defined IoT that would minimize human intervention and relieve the pain point of managing devices. It is one of the places where the IoT demands open, cross-discipline collaboration to rapidly and fully bring about the benefits envisioned. I invite you to visit <http://iot.ieee.org/iot-scenarios.html> to weigh in on the Intel-NTU Connected Context Computing Center’s concept for intelligent IoT middleware and other emerging IoT scenarios.

CONCLUSION

Collaboration is the key for a large system such as the IoT 1.0 to function optimally. Many different components across diverse application domains must be able to seamlessly interoperate, and each application domain has insights that must be taken into account for the greatest potential benefit of the IoT to be realized. Technologies must and will advance so that the system is still able to operate even in the reality of device failure.

CALL TO ACTION

IEEE is a proven forum for stakeholders globally to collaborate for the benefit of humanity. IEEE is the world's largest professional association dedicated to advancing technological innovation and excellence for the benefit of humanity, with more than 426,000 members in more than 160 countries (over 50% of whom are from outside the United States).

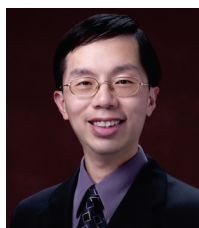
The IEEE IoT Initiative (<http://iot.ieee.org>), for example, has released a document intended to establish a baseline definition of IoT in the context of applications that range from small, localized systems constrained to a specific

location, to a large global system that is geographically distributed and composed of complex subsystems. The IEEE IoT Initiative invites global involvement from parties interested in advancing the definitions within the IoT.

In addition, the IEEE Standards Association has a number of standards, projects, and events that are directly related to creating the environment needed for a vibrant IoT (<http://standards.ieee.org/innovate/iot/index.html>).

Collaboration through such globally open activities will help ensure that the IoT indeed turns out to be the “next big thing.”

ABOUT THE AUTHOR



Yen-Kuang Chen is a principal engineer at Intel Corporation. His research areas span from emerging applications that can utilize the true potential of the IoT to computer architecture that can embrace emerging applications. Dr. Chen has 60+ U.S. patents, 20+ pending patent applications, and 90+ technical publications. He is one of the key contributors to Supplemental Streaming SIMD Extension 3 and Advanced Vector Extension in Intel microprocessors. Dr. Chen has served as a program committee member of more than 50 international conferences on IoT, multimedia, video communication, image processing, VLSI circuits and systems, parallel processing, and software optimization. He is a steering committee member of *IEEE Internet of Things Journal*, the past chair of the IoT Special Interest Group of the IEEE Signal Processing Society, the Editor-in-Chief of *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, and the Distinguished Lecturer of the IEEE Circuits and Systems Society. Dr. Chen received his Ph.D. from Princeton University and is an IEEE Fellow.



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Whether networking at events or accessing information through *EDFA*, *ISTFA* proceedings, or journals, our members have the edge. Now it's time to introduce EDFAS to others in the industry who would like to take advantage of these career-enhancing benefits. Help us help the industry by expanding our membership and offering others the same exceptional access to information and networking that sets EDFAS apart. To reacquaint yourself with and introduce others to the EDFAS member benefits, visit asminternational.org/web/edfas/membership.



Vincent LARATTA ©

ESREF opening session

ESREF 2015 IN TOULOUSE

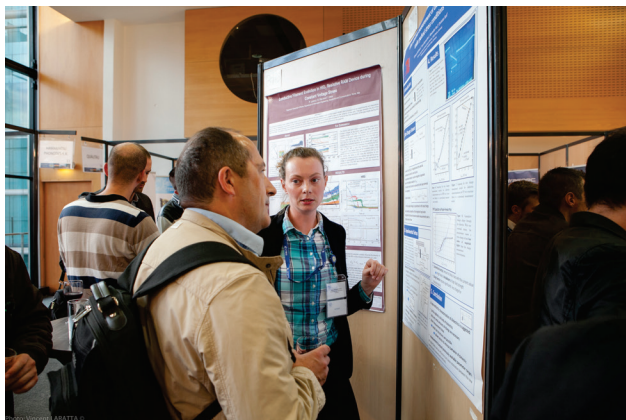
Marise Bafleur, ESREF 2015 Conference Chair
 Philippe Perdu, ESREF 2015 Conference Co-Chair
marise@laas.fr
philippe.perdu.cnes@gmail.com

The 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2015) was held October 5 to 9, 2015, in Toulouse, France. This was the first time the conference was hosted by the city of Toulouse, which is a world center for aeronautics (Airbus), the European capital of the space industry, and France's leader for embedded electronic systems. The ESREF 2015 Organizing Committee, led by Conference Chair Marise Bafleur (LAAS, France), assembled more than 100 volunteers to successfully stage the conference, which saw a record attendance of more than 400.

This international symposium continued to focus on recent developments and future directions in quality and reliability management of materials, devices, and

circuits for micro-, nano-, and optoelectronics. It provided a European forum for developing all aspects of reliability management and innovative analysis techniques for present and future electronic applications through twelve sessions:

- Session A: Quality and Reliability Assessment—techniques and methods for devices and systems
- Session B1: Silicon Technologies and Nanoelectronics—hot carriers, high-k, gate materials
- Session B3: Silicon Technologies and Nanoelectronics—electrostatic discharge, latch-up, radiation effects
- Session C: Failure Analysis
- Session D1: Microwave and Power Wide-Bandgap Semiconductor Devices



Poster session

- Session D2: Photonic
- Session D3: Photovoltaic and Organic Devices
- Session E1: Packaging and Assembly
- Session E2: MEMS, MOEMS, NEMS, and Nano-Objects
- Session F: Power Devices
- Session G: Space, Aeronautic, and Embedded Systems
- Session H: European FIB User Group (EFUG)

To draw new attendees and offer returnees an attractive conference, the organizers expanded the topical structure of the conference. Each topic was embedded with invited papers, tutorials, workshops, an oral session, a posted area for the oral presenters during the session breaks, and a poster session. The layout of the conference was set up to allow each attendee to build his or her optimal schedule by topic or by specific interest without overlaps. For example, it was possible to follow an expert

training track with two keynotes, ten tutorials, and nine invited papers. Hélène Fremont and François Marc (IMS, France), Technical Program Chairs; Peter Jacob (EMPA, Switzerland) and Giovanni Busatto (University of Cassino, Italy), Tutorial Chairs; and Mauro Ciappa (ETH Zürich, Switzerland), Thomas Zirilli (Freescale, France), and Fulvio Infante (Intraspec Technologies), Workshop Chairs, did an incredible job of building the best topical tracks.

Local attendance was also targeted. The Local Events Committee, chaired by Alain Bensoussan and André Durier (IRT Saint Exupéry, France), brought regional inputs to foster local attendance on aeronautic, space, and embedded systems, which was a hot topic during the conference. An opportunity was also provided for students from the area to participate in a Student Research “Speed-Dating” session. The award for the best one, “Evidence for Proton Diffusion in H⁺ Irradiated DFB and VCSEL Commercial Laser Diodes” by Giulia Marcello (Department of Electrical and Electronic Engineering, University of Cagliari, Italy), was presented during the gala dinner. Another boost for local attendance was a specific fee schedule for companies, with the capability to split the fees into half-days.

The ten workshops and the exhibition at the heart of the conference provided enhanced networking activities in a pleasant atmosphere. Interaction between the attendees and the 21 exhibitors was optimized by integration of exhibitor flash presentations to underline a specific technique. These flash presentations were fully integrated into the failure analysis track. All of the catering (coffee break, lunches, and cocktails on Monday) was held at



The ESREF exhibition

the Expo, and the twelve Expo-only hours presented the opportunity for attendees to network with key vendors representing the core business area in the fields of reliability and failure physics and analysis of electron devices and systems. Tuesday's cocktails at Capitole, the Toulouse city hall, and the gala dinner at the space museum (Cite de l'espace) were also excellent networking opportunities.

With up to four parallel tracks, the conference was very dense with rich content. During Monday afternoon's opening session, the first keynote speaker, Sylvestre Maurice (IRAP, France), presented a fascinating talk entitled "ChemCam Instrument on the *Curiosity* Rover: From R&D to Operations on Mars; Be Reliable or Die." The ChemCam project started as an R&D program at the French space agency CNES in 2001, was selected by NASA in 2005, was launched in 2011, and has operated on the *Curiosity* rover on Mars since 2012. It consists of a high-energy laser that, at a distance, creates plasma on Mars' soils and rocks to infer their elemental composition. He presented how the anomaly of a laser diode used for instrument autofocus was handled. The failure of this diode did not allow adjustment of the ablation laser pulses on rocks, forcing operators to multiply them. The software solution developed by the ChemCam team achieved autofocus by another process, thus restoring the entire system's agility. This feedback will be incorporated into the next SuperCam instrument.

The second keynote, by Ramesh Karri (Polytechnic Institute of New York University), focused on a very important topic, "Towards Hardware Cyber Security." Hardware security and trust are important design objectives, similar to power, performance, reliability, and testability. He highlighted why hardware security and trust are important objectives from the economics, security, and safety perspectives. Important messages from this talk included: (1) understanding simple "gotchas" when traditional design for test (DFT), test, and validation techniques are used (scan chains, JTAG, system-on-chip test, assertion-based validation); (2) understanding how traditional DFT, test, and validation techniques can be used to improve hardware security and trust; and (3) understanding "design-for-trust" approaches that can provide testability without compromising security and trust.

The opening session concluded with the Best Papers from sister conferences:

- *ISTFA 2014 Outstanding Paper*: "Localization of Weak Points in Thin Dielectric Layers by Electron Beam Absorbed Current (EBAC) Imaging" by Jörg Jatzkowski, Michél Simon-Najasek, and Frank Altmann (Center for Applied Microstructure Diagnostics, Fraunhofer

Institute for Mechanics of Materials, Halle, Germany)

- *IPFA 2015 Best Paper*: "UTB GeOI 6T SRAM Cell and Sense Amplifier Considering BTI Reliability" by Vita Pi-Ho Hu, Pin Su, and Ching-Te Chuang (Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Taiwan)
- *IRPS 2015 Best Paper*: "Platform Qualification Methodology: Face Recognition" by Ghadeer Antanius, Rutvi Trivedi, and Robert Kwasnick (Intel Corporation, USA)

Monday ended with a buffet served in the exhibition area.



Catering in the exhibition area

It is not possible to include all the topical tracks (up to four) held from Tuesday to Friday, but the following describes the one dedicated to failure analysis. It began with the invited speaker, Ludwig Balk (University of Wuppertal, Germany). In his talk, "EOBT: From Past to Future," Professor Balk reviewed optical and electron beam techniques and provided a view into future development requirements.

Next came the regular papers and posters session, with many interesting and varied subjects:

- "Nitrogen-Vacancy Centers in Diamond for Current Imaging at the Redistributive Layer Level of Integrated Circuits"



Cocktails in the Salle des Illustres at Capitole, the Toulouse city hall

- “Scanning Acoustic GHz-Microscopy versus Conventional SAM for Advanced Assessment of Ball Bond and Metal Interfaces in Microelectronic Devices”
 - “New I.R. Thermography Methodology for Failure Analysis on Tantalum Capacitors”
 - Comprehensive 2-D Carrier Profiling of Low Doping Region by High-Sensitivity Scanning Spreading Resistance Microscopy (SSRM) for Power Device Applications”
 - “Unsupervised Learning for Signal Mapping in Dynamic Photon Emission”
 - “Use of a Silicon Drift Detector for Cathodoluminescence Detection”
 - “Failure Analysis on Recovering Low Resistive Via in Mixed-Mode Device”
 - “RF Functional-Based Complete FA Flow”
 - “Improvement of Signal-to-Noise Ratio in Electro-Optical Probing Technique by Wavelets Filtering”
 - “Visualization of Gate-Bias-Dependent Carrier Distribution in SiC Power-MOSFET Using Super-Higher-Order Scanning Nonlinear Dielectric Microscopy”
 - “Electrical Model of an Inverter Body Biased Structure in Triple-Well Technology under Pulsed Photoelectric Laser Stimulation”
 - “Die Crack Failure Mechanism Investigations Depending on the Time of Failure”
 - “Latent Gate Oxide Defects Case Studies”
 - “Top-Down Delayering to Expose Large Inspection Area on Die Side-Edge with Platinum (Pt) Deposition Technique”
 - “Auger Electron Spectroscopy Characterization of Ti/NiV/Ag Multilayer Back-Metal for Monitoring of Ni Migration on Ag Surface”
 - “Magnetic Imaging for Resistive, Capacitive, and Inductive Devices: From Theory to Piezo Actuator Failure Localization”
 - “Microscopic Investigation of SiO₂/SiC Interface Using Super-Higher-Order Scanning Nonlinear Dielectric Microscopy”
 - “Thermoreflectance Mapping Observation of Power MOSFET under UIS Avalanche Breakdown Condition”
 - “Characteristics and Early Failure of PCB Embedded Power Electronics”
 - “Fault Isolation in a Case Study of Failure Analysis on Metal-Insulator-Metal Capacitor Structures”
 - “High-Resolution X-Ray Computed Tomography of Through-Silicon Vias for RF MEMS Integrated Passive Device Applications”
 - “Compact Thermal Modeling of Spin Transfer Torque Magnetic Tunnel Junction”
- The failure analysis track also had three embedded workshops:
- Advanced tools and techniques flash presentations: mini-workshops on methods and tools for failure

analysis and reliability; fault isolation and defect localization; sample preparation; nondestructive testing and physical characterization; and nanoscale electrical measurement

- Technical seminar: “Chip-Level Advanced Failure Analysis Case Studies,” organized by gold sponsor Sector Technologies
- EUFANET Workshop, organized by Jérôme Touzel (Infineon, Germany) and Olivier Crépel (AIRBUS Group Innovations, France)

The failure analysis track concluded Wednesday morning with the EFUG session, which had the following interesting presentations:

- “Focused High- and Low-Energy Ion Milling for TEM Specimens”
- “TEM Sample Preparation of an SEM Cross Section Using Electron Beam-Induced Deposition of Carbon”
- “Fabrication of Advanced Probes for Atomic Force Microscopy Using Focused Ion Beam”
- “Plasma FIB: Enlarge Your Field of View and Your Field of Applications”
- “Formation of Coupled Cavities in Quantum Cascade Lasers Using Focused Ion Beam Milling”

This session was followed by the EFUG Workshop, organized by Hugo Bender (IMEC, Belgium).

At the end of the conference, four awards were made:

- *Best Paper*: “System-Level Process-Voltage-Temperature Variation-Aware Reliability Simulator

Using a Unified Novel Gate-Delay Model for BTI, HCI, and GOBD” by Taizhi Liu, Chang-Chih Chen, Soonyoung Cha, and Linda Milor. This paper will be presented at the 27th IEEE International Reliability Physics Symposium (IRPS 2016) in Pasadena, Calif.

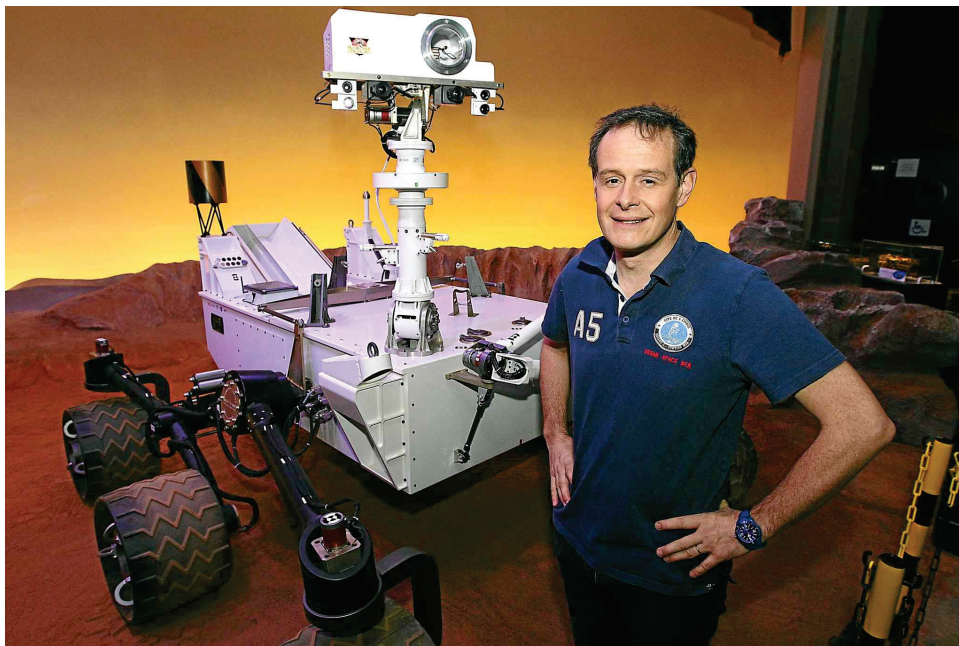
- *Best Paper*: “Effects of Buffer Compensation Strategies on the Electrical Performance and RF Reliability of AlGaIn/GaN HEMTs” by David Bisi et al. This paper will be presented at the 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2016) in Singapore.
- *Best Paper*: “Unusual Defects Generated by Wafer Sawing: An Update, Including Pick & Place Processing” by Peter Jacob. This paper will be presented at the 42nd International Symposium for Testing and Failure Analysis (ISTFA 2016) in Fort Worth, Texas.
- *Best Poster*: “A Way to Implement the Electro-Optical Technique to Inertial MEMS” by Kevin Melendez et al.

This review cannot end without a specific mention of the pre- and postconference program with lab tours. The Laboratory for Analysis and Architecture of Systems (LAAS) lab tour on Monday morning included:

- The LAAS clean room, consisting of a 1500 m² facility with classes ranging between 100 and 10,000. Its manufacturing equipment is devoted to micro- and nanotechnologies for electronics and optoelectronic devices.
- ADREAM, an experimental building devoted to experiments concerning energy-savings and green-energy



Social event at the space museum



Keynote speaker Sylvestre Maurice and the ChemCam on the Mars *Curiosity* rover

use, together with the deployment of sensor networks and robots

The other Monday morning tour was of the ITEC lab, a well-equipped platform shared by CNES, Thales, Elemca, and Intraspac Technologies. The tour was organized around demo workshops at the heart of component analysis:

- The FIB
- Sample preparation
- Electrical testing
- X-ray computed tomography
- Do you like MEMS?
- Light emission and laser tests
- Electron backscatter diffraction: microscopy for material analysis
- Defect localization
- Microscopes

There were also industry tours on Friday afternoon, including:

- TRAD Tests and Radiations, which provided a complete tour of the entire radiation assurance chain: radiation analysis, electronic components and material testing, radiation software development, and training courses
- Freescale Discovery Lab, which has the goal of targeting disruptive innovation, from project selection to proof-of-concept development and innovation protection

A big thank you is extended to all the volunteers, to the efficient and excellent LAAS team support, and to all the

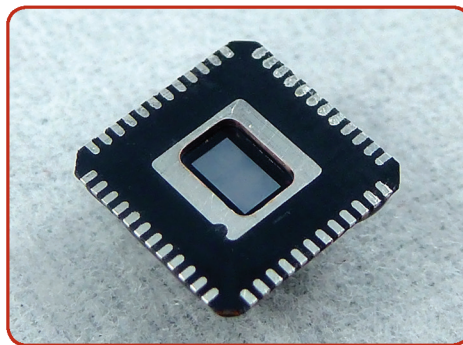
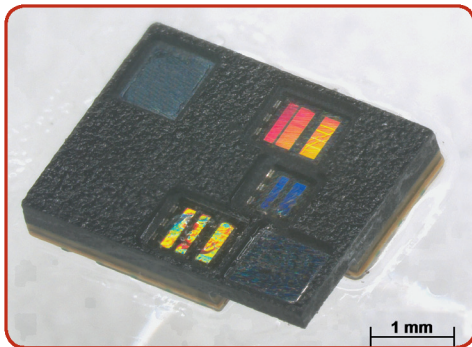
participants and attendees who created this memorable event.

Don't miss the 27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2016), which will be held September 19 to 22, 2016, in Halle (Saale), Germany. ESREF 2016 will have a specific focus on reliability issues in automotive electronics.

Matthias Petzold (Fraunhofer Institute for Microstructure of Materials and Systems, Center for Applied Microstructure Diagnostics) has the great pleasure of inviting you to meet the experts in electronics reliability and failure analysis at ESREF 2016: "With regard to current technology developments and market trends in the automotive industries, it is very impressive to note how fast electronics became one of the most decisive factors for today's and future automotive applications. New trends, such as assisted driving and connected cars, electric vehicles, or progress in motor and safety management, are highly dependent on increasingly more complex semiconductor-based systems. In turn, these new application fields are significantly affecting the technology roadmaps of the electronics industry. There is no doubt that these thrilling developments will also pose many new and very challenging demands specifically on electronics robustness and reliability. Thus, while ESREF 2016 will continue to consider the full spectrum of reliability topics in electronics, it will additionally address the field of automotive electronics reliability as its special topic."

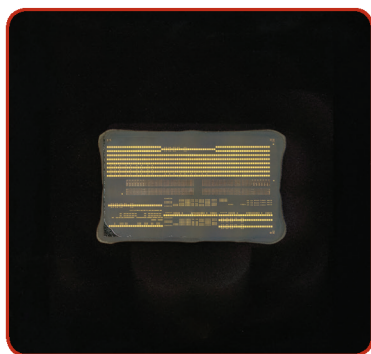
Mark your calendars for this event, and visit the ESREF website at esref.org for updated information. ■

Small Device Preparation

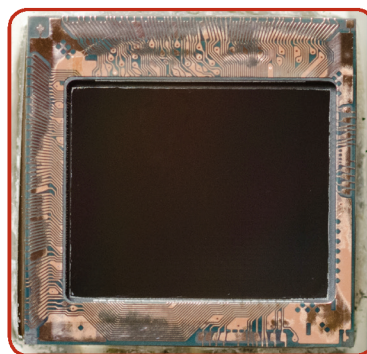


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- TSV exposure



- Targeted stacked die exposure

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Advancing Technology Through Sample Prep

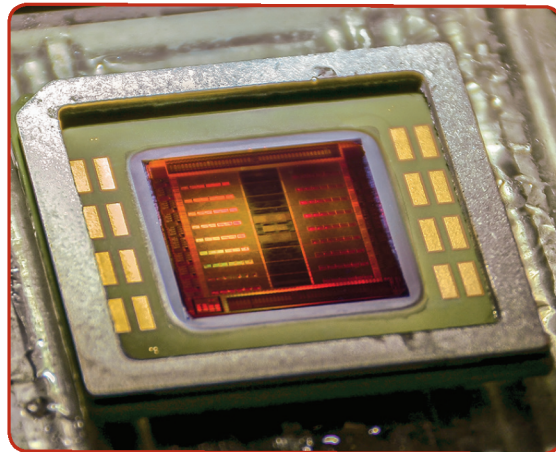
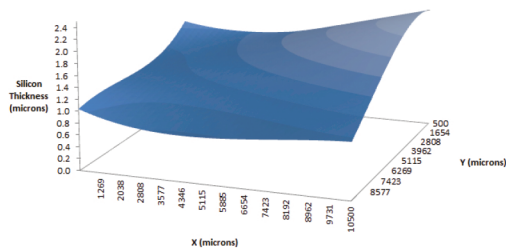


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Where: Selected entries will be displayed and prizes awarded November 6-10, 2016, at the 42nd International Symposium for Testing and Failure Analysis (ISTFA) Conference and Exposition in Fort Worth, Texas.

Categories: No more than one image per person allowed in each category

I. Color Images Only (*Optical Microscopy*)

II. Black & White Images Only (*Optical Microscopy/SEM/TEM/X-Ray/UV Micrographs/Other*)

III. False Color Images Only (*SPM/SAM/Photon Emission/Other*)

Images will be judged on failure analysis relevance (35%), aesthetics (35%), and novelty of the technique or mechanism (30%).

Deadline: Entries must be submitted by September 2, 2016.

Entries: Submit by e-mail to photocontest@edfas.org (subject line: EDFAS Photo Contest).

Format: Submissions should be made through e-mail only, with one picture attached. Each submission must be in a standard format (PNG, JPEG, TIFF, BMP, etc.). Please provide your highest-resolution image. The preferred submission is a .jpg or .tif, five inches wide at 300 dpi resolution.

Along with the picture, the e-mail should include the name of the submitter, category of submission, mailing address, phone, fax, e-mail address, and a description of the micrograph (not exceeding 50 words). The picture should not have any contact information embedded.

Copyright & Permissions: Entrants are responsible for obtaining any releases or any other permission or license necessary for the submission of their work for this contest and future publication. EDFAS and ASM International will have the right to exhibit, reproduce, and distribute in any manner any or all of the entries. The entries will not be returned to the submitters.

Prizes: **1st place** in each category receives a wall plaque and one-year complimentary EDFAS membership.

2nd and 3rd places in each category receive award certificates and one-year complimentary EDFAS memberships.

The top 10 entries in each category will be displayed at ISTFA 2016 in Fort Worth, Texas.



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Format: MPEG or AVI format with a maximum size of 50 MB. The video should be 3 minutes or less. Audio and subtitles are allowed. A short description should also be submitted along with all of your complete contact information.

Categories: **Failure Analysts:** Anyone working in the failure analysis field

Students: Students currently studying in fields related to failure analysis (physics/electrical engineering/chemistry/materials science, etc.)

Exhibitors

Deadline: September 30, 2016

Entries: Go to <https://asm.confex.com/asm/istfa16/cfp.cgi>

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Prizes: **1st place** receives a complimentary registration to a future ISTFA conference and a 1st place winner plaque.

2nd place receives a \$25 gift card and award certificate.

3rd place receives an award certificate.

(Note: 2nd place will be awarded if total submissions are more than 10; 3rd place will be awarded if total submissions are more than 15.)

The top 10 entries in each category will be displayed at ISTFA 2016 in Fort Worth, Texas.

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ISTFA 2016 |



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ISTFA 2016 PREVIEW

Martin Keim, ISTFA 2016 General Chair
Mentor Graphics Corporation
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Fort Worth skyline at night



Selecting the theme of the symposium is one of the great privileges of the General Chair. The theme binds together the individual aspects of the symposium, focuses the activities, and sets the overall tone for the entire week. Selecting the theme is also something that can cause sleepless nights for the General Chair...

ACTING ON “THE NEXT-GENERATION” THEME

“The Next Generation” is the theme I chose for the 42nd International Symposium for Testing and Failure Analysis (ISTFA). It places up-front-and-center the “crisis” we are facing. After I announced the theme at the EDFAS General Meeting during ISTFA 2015, fellow engineers came to me to passionately express their concern that not enough new engineers are entering the field of failure analysis, and those who are need lots of extra training.

The most recent symposia began instituting programs to counter this trend. For 2016, we are intensifying our efforts to attract new engineers as well as offer opportunities for students to present their work and engage in

discussions with experts in the field. These interactions benefit both sides tremendously. A student’s mind may be placed on a path toward researching something extraordinary, and you, the expert, may have met your future new hire. The ISTFA Organizing Committee plans to offer special prizes as a way of acknowledging contributions from students.

In preparation for ISTFA’s Panel Discussion and keynote speaker, we dug deeper into what is “out there”—something that shows the failure analysis community working solutions to the next-generation problem. We were successful in finding several such examples. In his keynote address, Prof. Dr.-Ing. Christian Boit from the Technische Universität Berlin, former director of failure analysis at Infineon Technology and General Chair of ISTFA 2002, will make the case that it is possible for a university to equip engineers with great skills and knowledge, ready to enter the workforce in the demanding failure analysis world. His students successfully find internships and employment at tier-1 semiconductor companies not only in Europe but

(continued on page 34)



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SAVE THE DATE!

THE NEXT GENERATION FA ENGINEER

Failure analysis engineers are constantly challenged by next generation technology, materials, and equipment. Learn from experts, network with people who can support your work, explore the latest apps and tools for the lab, and keep up with the industry at ISTFA 2016. The expo floor at ISTFA, the largest FA equipment exposition in the country, is also a big draw because all the top companies are represented. Mark your calendar to attend ISTFA and see where the industry is headed for the next generation FA engineer.

INTERESTED IN EXHIBITING OR CUSTOM SPONSORSHIP PACKAGES?

Contact Christina Sandoval, Global Exhibition Manager at christina.sandoval@asminternational.org or 440.338.5151 ext. 5625.

[VISIT ASMINTERNATIONAL.ORG/ISTFA2016 TO LEARN MORE]

Organized By:





The conference hotel, the Omni Fort Worth

also in the United States. The Panel will follow “The Next-Generation” theme with additional participants from the semiconductor industry and failure analysis labs. Look forward to an exciting Panel Discussion.

OUTSTANDING TECHNICAL PROGRAM

The technical program also underwent small changes, based on attendees’ feedback from previous years. One such change is an opening address, in selected sessions, from well-known experts. These experts will discuss, for example, the next generation of technology that lies just beyond today’s horizon. As in previous years, the Technical Program Chair and her team of session chairs, co-chairs, and reviewers will have a hard time selecting the very best papers to be presented from among the many, many excellent submissions we received. Thank you all for your contributions. The technical program of ISTFA 2016 will be another fantastic one. As in previous years, the technical program of paper presentations is accompanied by posters, User Group meetings, short courses, as well as tutorials. The latter also underwent an in-depth review



Fort Worth Convention Center

of the value that each tutorial provides to the attendees, and changes are being implemented. Look for all of these updates in the advanced program, which will be published at a later date on the ISTFA web page at istfa.org.

EXPO AND NETWORKING

ISTFA is well known for its extensive Exposition. In 2016, you can again expect more than 60 companies to exhibit their latest tools and technologies. The Tools-of-the-Trade Tour returns, so register early! Also returning are the Expo-only hours, which allow you to stroll about the Expo floor and maybe pursue one of the sweet desserts that will be served.

The numerous networking opportunities are another great benefit of ISTFA. The Social Event in Portland last year set the bar very high. Many positive comments were received by the Organizing Committee. However, I am confident that “Billy Bob’s Texas” will be at least as good. Ever wanted to learn to line dance or ride a bull?

You must experience all this in person. I invite you to come to Fort Worth, Texas, on November 6 to enjoy five days of ISTFA and its theme of “The Next Generation.”

Advertise in *Electronic Device Failure Analysis* magazine!

For information about advertising in *Electronic Device Failure Analysis*, contact Kelly Thomas, CEM.CMP,
National Account Manager; tel: 440.338.1733; fax: 614.948.3090;
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edfas.org

ISTFA 2016 EXHIBITORS



ISTFA/2016®

ISTFA 2016 EXHIBITORS as of 6-20-16

BOOTH #	COMPANY	BOOTH #	COMPANY
122	Advanced Circuit Engineers, LLC	120	Materials Analysis Technology Inc.
504	Advantest Corporation	306	Mentor Graphics
125	Akrometrix LLC	518	MESOSCOPE Technology Co., Ltd.
201	Allied High Tech Products, Inc.	124	MUEGGE GmbH
114	Anasys Instruments	322	Nanolab Technologies
231	Angstrom Scientific Inc.	111	Neocera, LLC
419	Applied Beams	501	Nikon Metrology
423	Attolight AG	416	Nippon Scientific Co., Ltd.
222	Balazs NanoAnalysis	311	Nisene Technology Group
421	Barnett Technical Services	127	Nordson DAGE
313	Bruker	412	Olympus America, Inc.
211	Carl Zeiss Microscopy, LLC	401	Oxford Instruments America
301	Checkpoint Technologies, LLC	101	Park Systems Inc.
409	Electron Microscopy Sciences	225	Quantum Focus Instruments Corp.
117	Evans Analytical Group	121	Quartz Imaging Corp.
126	EXpressLO LLC	415	Robson Technologies, Inc.
106	FEI Company	500	Sage Analytical Lab
208	Gatan, Inc.	216	SAMCO Inc.
207	Hamamatsu Corporation	331	SELA USA Inc.
223	HDI Solutions-Hitachi	324	SEMICAPS
224	HiLevel Technology, Inc.	210	Sonoscan, Inc.
524	Hi-Rel Laboratories	115	South Bay Technology
305	Hitachi High Technologies America, Inc.	204	SPI Supplies
118	ibss Group Inc.	109	Synopsys Inc.
113	Imina Technologies SA	425	Ted Pella, Inc.
414	IXRF Systems, Inc.	317	Tescan USA, Inc.
200	JEOL USA, Inc.	105	TMC Ametek
103	JIACO Instruments	221	ULTRA TEC Mfg., Inc.
411	Keysight Technologies	321	ULTRA TEC Mfg., Inc.
330	Kleindiek Nanotechnik	427	XEI Scientific, Inc.
420	LatticeGear LLC	116	YXLON Feinfocus
212	Left Coast Instruments/RKD Engineering	112	Zurich Instruments AG



BOARD OF DIRECTORS NEWS

EDFAS BOARD OF DIRECTORS REPORT

Bill Vanderlinde, EDFAS Secretary, IARPA
william.vanderlinde@iarpa.gov

The EDFAS Board of Directors held its annual three-hour strategic planning extended teleconference on Tuesday, April 26, 2016. Board President Cheryl Hartfield reported on the many recent accomplishments. A new Mission Statement was adopted reflecting an emphasis on global influence and taking a role in driving FA technology advances, a new “EDFAS Product Roadmap” was initiated, a Virtual Content List was created and champions were assigned, Sweta Pendyala was appointed Volunteerism Chair, and three new EDFAS awards were created. Opportunities for the coming year include improving the job board, EDFAS networking, enhanced digital content, and engaging new and existing volunteers.

ISTFA General Chair Martin Keim reported that preparations for ISTFA 2016 are on schedule, with a record number of abstracts submitted. Held in Fort Worth, Texas, ISTFA 2016 will be themed “The Next Generation.” ISTFA 2016 will be at the same location and on consecutive weeks with the International Test Conference, providing opportunities for collaboration and shared attendees.

EDFAS Finance Officer Chris Henderson reported that EDFAS had a good year financially, with revenue favorable to plan, largely due to a successful ISTFA 2015 event.

Membership Chair Tom Moore requested ASM deliver a five-year plan based on the committee’s recommendations for improving the value of EDFAS membership.

EDFA magazine Editor Felix Beaudoin reported that the magazine continues to have strong technical content and solid advertising revenues. Please contact Felix if you are interested in writing an article!

Results of the EDFAS Board officer elections were announced: Zhiyong Wang, President; Lee Knauss, Vice President; Jay Demarest, Finance Officer; William Vanderlinde, Secretary; and Cheryl Hartfield, Immediate Past President. Two open Member-at-Large positions will be filled by a vote of the full EDFAS membership in June. Five very well-qualified candidates are running for these two positions.

The Board continues to pursue international collaborations, virtual content, and social media using web-based technologies. They are also seeking to better leverage EDFAS volunteers and are looking to implement FA tool road-mapping.

The Board of Directors strives to strengthen the visibility and credibility of our Society by providing value to EDFAS members and, through its volunteers, beneficial contributions to our industry. Your engagement in EDFAS is highly encouraged. Please feel free to connect with any Board member to discuss your ideas or interest in volunteering in the Society.



NOTEWORTHY NEWS

ESREF 2016

The 27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF ’16) will take place **September 19 to 22, 2016**, in Händel-Halle, Halle (Saale), Germany. The conference continues to focus on recent developments and future directions in quality, robustness, and reliability research of materials, components, integrated electronic circuits/systems, and their nano-, micro-, power-, and optoelectronics devices. ESREF provides the leading European forum for developing all aspects of reliability management and failure prevention for present and future electronics. ESREF 2016 will have a specific focus on reliability issues in automotive electronics.

For more information, visit esref2016.org.



GUEST EDITORIAL

CONTINUED FROM
PAGE 2

approaches or techniques. This is essential in cases where difficult problems are encountered or new phenomena are observed.

- Clues that were observed early in the investigation, but whose significance was not initially realized, can be taken into account when *one analyst* performs various steps. This is in contrast with a scheme where each “expert” sees only a small piece of the puzzle, with incomplete knowledge of what else was seen.
- It facilitates high flexibility in utilizing total available resources and capabilities for the benefit of the customers, not to mention the wider scope and possibilities/challenges for personal development of failure analysts.

FA PROCESS AND TASKS OF THE FAILURE ANALYST

The failure analyst must act as a troubleshooter, work together with the customer, and strive to understand all aspects of the problem that may have an impact on the root cause.

It is the task of the failure analyst to cast a sufficiently wide net when investigating a problem. That is, the analyst must actively question the assumptions made

by the customer on possible causes and respectfully but firmly insist on data that test various hypotheses, so as not to “take anybody’s word for it.” The failure analyst is responsible for guiding the investigation to the root cause, not just for performing the analysis steps the customer may have in mind.

To do this, the analyst must be multilingual, mastering the mother tongue of FA engineering and speaking fluently the languages of front- and back-end processes, design, and test. Last but not least, the failure analyst must excel in communication skills worthy of leading a problem-solving team and ultimately speaking the end-customer’s language.

If all of these qualities were met, an FA engineer becomes a forensic investigator, not just revealing the physical cause but also explaining what led to the failure and therefore solving a much bigger puzzle for the benefit of the company and its end-customer.

JOIN THE CONVERSATION

“The Next Generation of FA Engineer” is the topic of the ISTFA 2016 Panel Discussion. Please join the conversation in Fort Worth!



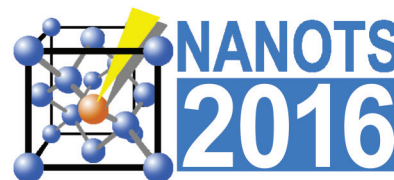
NOTEWORTHY NEWS

NANOTS 2016

The 36th annual NANO Testing Symposium (NANOTS 2016) will be held **November 9 to 11, 2016**, at the Senri Life-Science Center in Toyonaka, Osaka, Japan. NANOTS is one of the leading technical symposia for discussing solutions that improve the testing process of nanoscale devices and materials. The three-day event will consist of a symposium with a special invited talk, a special session, technical sessions, a commercial session, an equipment exhibition, and an evening session.

NANOTS is sponsored by the Institute of NANO Testing in cooperation with the Institute of Electronics, Information, and Communication Engineers, the Japan Society of Applied Physics, the Reliability Engineering Association of Japan, and the Union of Japanese Scientists and Engineers.

For more information, visit the NANOTS website at www-nanots.ist.osaka-u.ac.jp/en.



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PRODUCT NEWS

PRESS RELEASE SUBMISSIONS:
MAGAZINES@ASMINTERNATIONAL.ORG

Larry Wagner, LWSN Consulting Inc.
lwagner10@verizon.net

FEI LAUNCHES APREO HIGH-PERFORMANCE SEM

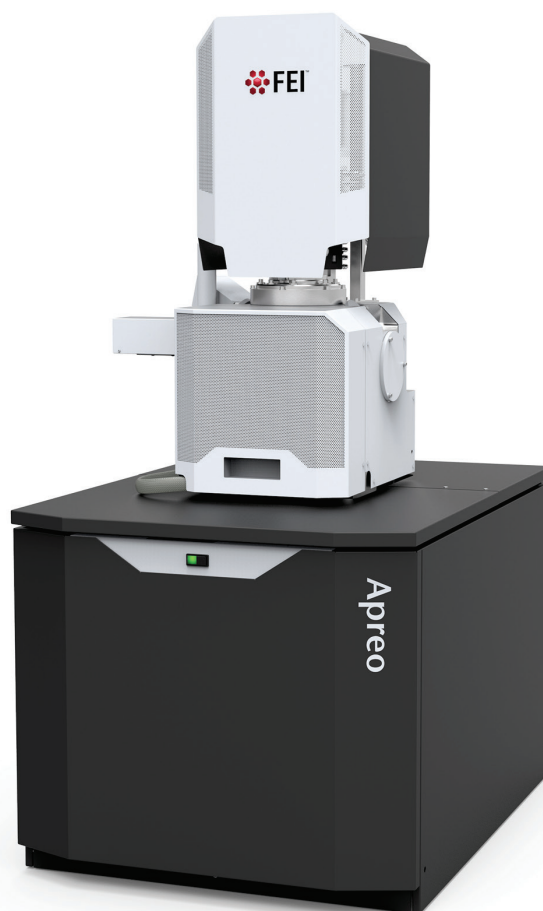
FEI (Hillsboro, Ore.) announced the new Apreo scanning electron microscope (SEM), offering an industry-leading range of applications. Apreo offers exceptional versatility in fields ranging from materials and life sciences to research in semiconductors, energy, and chemistry.

Researchers and developers must obtain as much microscopic information as possible from their samples. They want to be able to see materials contrast and determine the chemical or crystallographic properties of a wide range of samples, such as conductors, insulators, and those that are magnetic- or beam-sensitive. Researchers want to operate over a wide range of conditions, including high or low vacuum and at different tilt angles. Apreo provides this capability.

Due to its proprietary compound final lens design, the Apreo SEM is capable of resolution down to 1.0 nm at 1 kV without the need for beam deceleration, providing high performance on nearly any sample, even if it is tilted or topographic.

Trisha Rice, Vice President and General Manager of FEI's Materials Science Business, said, "Apreo was specifically designed to be the midrange SEM tool of choice. Its feature set and ease of use should put it at the top of the list for our research and industrial laboratory customers who require high performance, broad versatility, and easy operation over a wide range of applications for users with varying levels of expertise."

Apreo offers backscatter detection at the lowest beam currents, at any tilt angle, on sensitive samples and at TV-rate imaging, so materials contrast is strong. Detector segments can be individually addressed, which allows researchers to optimize for angular contrast or for signal intensity and to extract the information that matters most. It provides a wide range of approaches for dealing with insulating samples, including a low-vacuum capability with a chamber pressure of up to 500 Pa. Finally, Apreo is an excellent tool for analytics, with ports for up to three energy-dispersive x-ray spectrometry (EDS) detectors, coplanar EDS, and electron backscatter diffraction. It also



FEI's Apreo high-performance SEM

has analytics-compatible low vacuum and beam currents up to 400 nA.

The Apreo software provides user guidance and point-and-click navigation using an in-chamber camera, making it easy for even novice users to obtain excellent results. High-productivity labs will appreciate the capability to load multiple samples quickly and easily without tools.

For more information: web: fei.com/apreo.

RENISHAW OFFERS CONFOCAL RAMAN MICROSCOPE

The new inVia Qontor is the most advanced Raman microscope offered by Renishaw (Gloucestershire, U.K.). Building on the market-leading inVia Reflex, the inVia

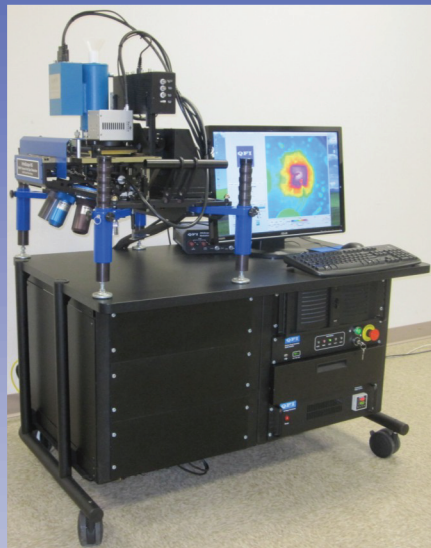
(continued on page 42)

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Application requirements drive configuration decisions.

QuantumScope™ failure analysis microscopes and InfraScope™ temperature measurement microscopes are available in a variety of configurations. Flexibility has always been a core design principle at QFI. We understand the need to consider both current and projected applications when establishing the appropriate capability set for any analytical equipment. QFI systems are generally compatible with field upgrade to address changing requirements. We invite you to discuss your specific analytical needs. Please let us know how we can assist you via the contact information listed below.



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Fax: +1 (760) 599-1242

e-mail: sales@quantumfocus.com

<http://www.quantumfocus.com>



PRODUCT NEWS

CONTINUED FROM
PAGE 40

Qontor adds a new dimension to the performance and ease of use for which inVia is renowned.

The inVia Qontor includes the addition of Renishaw's latest innovation, LiveTrack focus-tracking technology, which enables users to analyze samples with uneven, curved, or rough surfaces. Optimum focus is maintained



Renishaw's inVia Qontor Raman microscope

in real-time during data collection and white light video viewing. This removes the need for time-consuming manual focusing, prescanning, or sample preparation.

The inVia Qontor, equipped with LiveTrack, enables the acquisition of accurate and reproducible spectra from samples with extensive topographic variations. Because a sample's topography no longer limits Raman imaging capability, LiveTrack opens up the analysis of a whole new range of samples and applications.

With LiveTrack, focusing is dynamic. LiveTrack provides continuous feedback to the sample stage, which adjusts to follow the height of the sample. This ensures that the laser maintains focus during data collection and when manually moving the sample during white light video viewing. Optimum focus is maintained across uneven, sloping, or dynamic samples, limited only by the maximum travel of the stage.

The inVia Qontor enables the analysis of samples that were previously impractical to study or would have required extensive sample preparation. For example, uneven geological samples that normally require sectioning and polishing can now be analyzed without any sample preparation.

Tim Smith, Renishaw Applications Scientist, said, "Acquiring in-focus Raman images of your whole sample is now a reality. Users can track the surface live while

acquiring surface or even subsurface Raman data and later view the Raman image and surface topography of their sample in 3-D. This innovation not only saves time but, in some cases, allows us to analyze samples that were previously impossible to study."

The inVia range of microscopes is trusted worldwide to deliver outstanding performance and reliable results for even the most challenging experiments. The inVia Qontor Raman microscope's cutting-edge technology reduces overall experiment times and makes it easy to analyze even the most complex samples.

For more information: web: renishaw.com.

NORDSON DAGE ANNOUNCES QUADRA X-RAY INSPECTION

Nordson DAGE (Aylesbury, Buckinghamshire) announced the launch of its fourth-generation ultra-high-resolution off-line x-ray system, the Quadra series. With its in-house proprietary QuadraNT tube, Aspire FP detector, Gensys inspection software, and QuadraGen power supply, Nordson DAGE offers the future of x-ray image resolution, reliability, performance, and throughput.

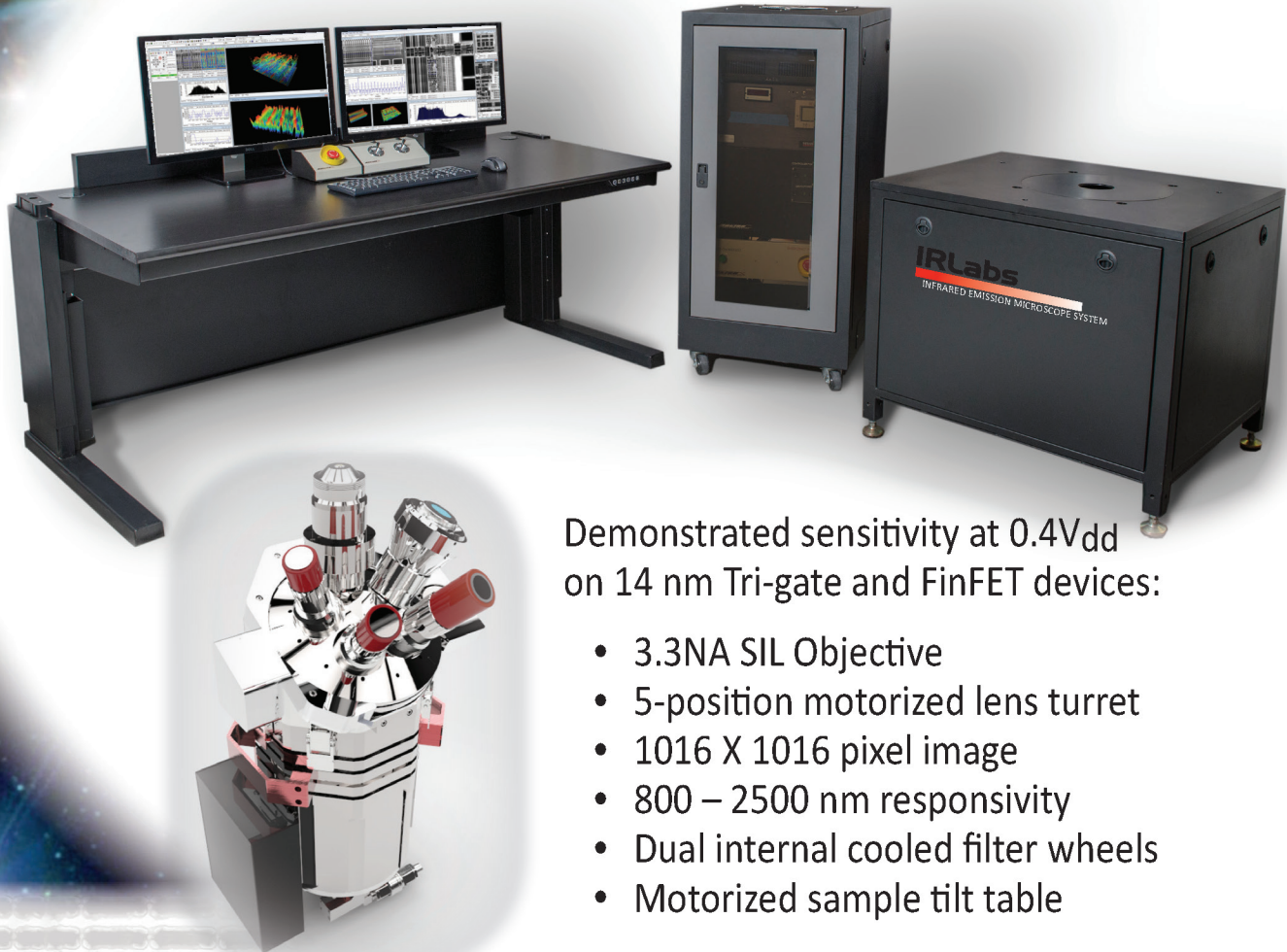
Nordson DAGE's flagship system, the Quadra with 0.1 μm submicron feature recognition, comes equipped with two 4 K ultrahigh-definition (UHD) displays. Their 8 million pixels fully show the 50 μm pixel pitch and 6.7 MP image size of the Aspire FP detector. The 4 K UHD offers up to 4 times the detail compared to standard high-definition display screens and supports 68,000 \times total magnification. Submicron-level features can be seen without a loss of detail.

The Quadra, with industry-leading core technology, offers high performance and ease of use for 2-D and 3-D x-ray applications. The 0.35 μm feature recognition up to 10 W of power, with optional 20 W, makes Quadra 5 the leading choice for printed circuit board and semiconductor package inspection.

Ben Peacock, Business Director of X-Ray Systems, commented, "The launch of the Quadra series x-ray systems marks the start of a new and exciting chapter in inspection solutions for the electronics industry. We have continued to build on our solid foundation of leading-edge technology development while maintaining a real focus on our customers' needs. Further vertical integration of the key elements within the systems has enabled us to remain

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Extended Wavelength IREM-IV Photon Emission Microscope

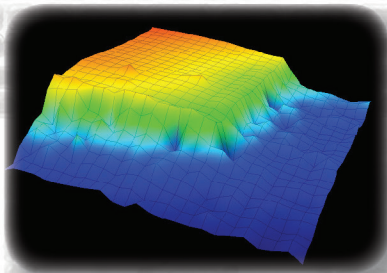


Demonstrated sensitivity at 0.4V_{dd}
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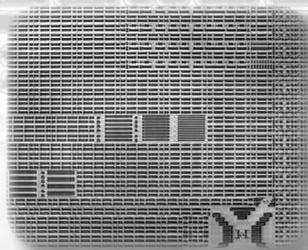
NEW! LASER SURFACE PROBE

Measure device tilt and profile



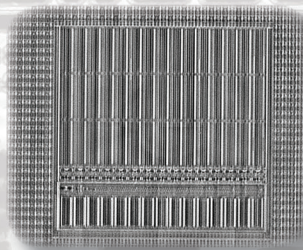
HIGHEST RESOLUTION

3.3 NA SIL Objective



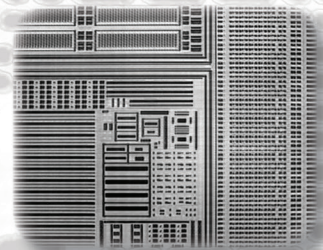
MOST SENSITIVE

22nm Tri-Gate Device



LARGEST FIELD OF VIEW

Custom Optics



PRODUCT NEWS

CONTINUED FROM
PAGE 42

competitive while pushing performance boundaries. We really believe the best has just become better, and we are looking forward to demonstrating the enhancements of the new Quadra systems to the electronics market.”

For more information: web: nordson.com.

WAVERUNNER 8000 OSCILLOSCOPES ADD ONETOUCH CONTROL

Teledyne LeCroy, Inc. (Chestnut Ridge, NY), a Teledyne Technologies company, introduced the WaveRunner 8000 oscilloscopes with bandwidths from 500 MHz to 4 GHz. WaveRunner 8000 has the industry’s widest and deepest



Teledyne LeCroy’s WaveRunner 8000 oscilloscope

collection of tools, making it very powerful. WaveRunner 8000 marks the debut of the next-generation MAUI (most advanced user interface), bringing enhancements to the oscilloscope industry’s premier user interface. The addition of OneTouch to MAUI makes measurement setup very intuitive and easy, providing users with dramatically faster time-to-insight into complex signal abnormalities.

“Teledyne LeCroy’s WaveRunner oscilloscopes have delivered exceptional value to customers in the midrange of the oscilloscope space for nearly two decades,” said Tom Reslewic, Chief Executive Officer of Environmental and Electronic Measurement Instrumentation. “The new WaveRunner 8000 oscilloscopes continue this legacy by delivering unprecedented performance, powerful tools for debugging, and unparalleled ease of use—all at very reasonable prices.”

The WaveRunner 8000 and MAUI with OneTouch extend Teledyne LeCroy’s long tradition of user-interface innovation. MAUI with OneTouch has revolutionary drag-and-drop actions to copy and set up channels, math functions, and measurement parameters without lifting a finger. Along with the standard collection of math, measurement, debug, and documentation tools and application-specific packages, the new WaveRunner 8000 provides all the power and capability required to deliver faster time-to-insight with easy access to all the oscilloscope functions.

For more information: web: teledynelecroy.com/wr8000/.

NOTEWORTHY NEWS

EOS/ESD SYMPOSIUM

The 38th Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium will be held **September 11 to 16, 2016**, at the Hyatt Regency Orange County in Garden City, Calif. The symposium is focused on discussing the issues and providing the answers to electrostatic discharge in electronic production and assembly. Attendees will gain beneficial electrostatic knowledge, learn solutions to electrostatic issues and obstacles, discover new and emerging technologies, network with ESD professionals, and develop valuable peer and industry contacts.

The EOS/ESD Symposium is sponsored by the EOS/ESD Association and co-sponsored by IEEE’s Electron Devices Society, EMC Society, and Reliability Society.

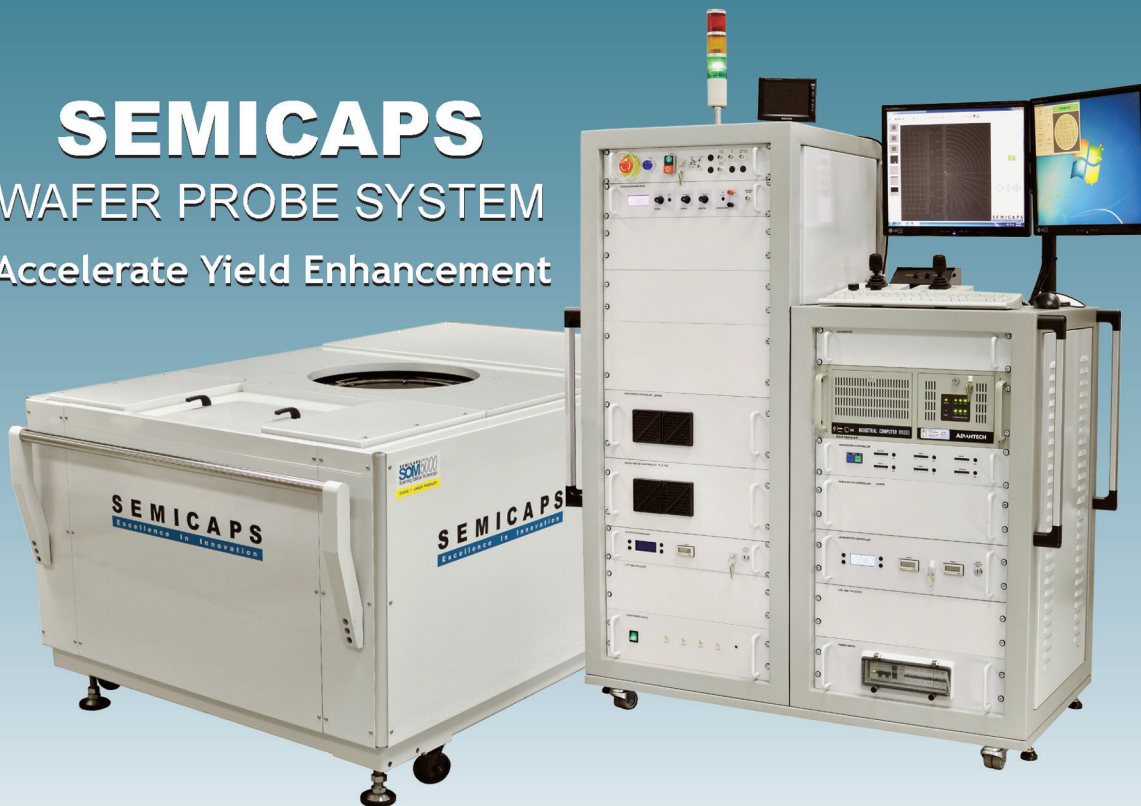
For more information, visit the EOS/ESD Association’s website at esda.org.

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SEMICONDUCTOR ONLINE TRAINING

EDFAS offers online training specialized for semiconductor, microsystems, and nanotechnology suppliers and users. These online training courses are designed to help engineers, technicians, scientists, and managers understand each of these dynamic fields. This one-year subscription provides access to several courses covering semiconductor failure analysis, design, packaging, processing, technology, and testing. Find out more by visiting edfas.org and clicking on Education.

August 2016

EVENT	DATE	LOCATION
Digital Fluorescence Microscopy	8/2-4	Westmont, IL

Contact: McCrone Group

Medical Device Design Validation and Failure Analysis	8/4-5	Novelty, OH
Science and Technology of Materials	8/8-9	Novelty, OH
Metallurgy for the Non-Metallurgist	8/15-18	Novelty, OH

Contact: ASM International

Hands-on Failure Analysis Workshop	8/15-19	Spokane, WA
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Contact: Hi-Rel Laboratories

September 2016

EVENT	DATE	LOCATION
38th Electrical Overstress/Electrostatic Discharge Symposium	9/11-16	Garden Grove, CA

Contact: EOS/ESD Association, Inc.

Semiconductor Reliability and Qualification	9/12-15	San Jose, CA
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Contact: Semitracks, Inc.

Fractography	9/12-15	Novelty, OH
Practical Fractography	9/14-15	Lansing, NY
How to Organize and Run a Failure Investigation	9/19-20	Foothill Ranch, CA
Introduction to Metallurgical Lab Practices	9/19-21	Novelty, OH
Principles of Failure Analysis (3-day)	9/21-23	Foothill Ranch, CA

Contact: ASM International

International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems	9/19-20	Storrs, CT
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Contact: DFT 2016

September 2016 (cont'd)

EVENT	DATE	LOCATION
Polarized Light Microscopy	9/19-23	Westmont, IL

Contact: McCrone Group

37th International Electronics Manufacturing Technology & 18th Electronics Materials and Packaging Conference	9/20-22	Penang, Malaysia
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Contact: IEMT & EMAP

Accelerated Stress Testing & Reliability Conference	9/28-30	Pensacola Beach, FL
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Contact: ASTR 2016

October 2016

EVENT	DATE	LOCATION
Metallographic Interpretation	10/3-6	Westlake, OH

Reverse Engineering: A Material Perspective	10/10-12	Novelty, OH
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Metallurgy for the Non-Metallurgist	10/10-13	Novelty, OH
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Contact: ASM International

Hands-on Failure Analysis Workshop	10/3-7	Spokane, WA
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Contact: Hi-Rel Laboratories

Electronics Packaging Symposium	10/6-7	Binghamton, NY
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Contact: EPS 2016

International Integrated Reliability Workshop	10/9-13	Fallen Leaf Lake, CA
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Contact: IIRW 2016

EOS/ESD Factory Symposium in Finland—Tutorials	10/10-11	Helsinki, Finland
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Contact: EOS/ESD Association, Inc.

October 2016 (cont'd)

EVENT	DATE	LOCATION
Transmission Electron Microscopy	10/11-13	Westmont, IL
Sample Preparation Techniques	10/11-13	Westmont, IL
Scanning Electron Microscopy	10/24-28	Westmont, IL
Contact: McCrone Group		
MS&T 2016 Conference & Exposition	10/23-27	Salt Lake City, UT
Contact: ASM International		

November 2016

EVENT	DATE	LOCATION
ISTFA 2016 Conference & Exposition	11/6-10	Fort Worth, TX
Metallographic Techniques	11/7-10	Novelty, OH
Contact: ASM International		
Infrared Microscopy	11/7-9	Westmont, IL
Spectral Interpretation	11/10-11	Westmont, IL
Contact: McCrone Group		

All Your Critical FIB/SEM Needs From One Key Supplier



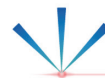
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ASTR 2016

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Web: www.dfts.org

EOS/ESD Association, Inc.

Tel: 315.339.6937
e-mail: info@esda.org
Web: esda.org

EPS 2016

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Tel: 607.777.4769
e-mail: sbpark@binghamton.edu
Web: binghamton.edu/ieec/symposium/index.html

Hi-Rel Laboratories

Kristy White
Tel: 509.325.5800
e-mail: kristy@hrlabs.com
Web: hrlabs.com/index.php?id=training.php#1001

IEMT & EMAP

Hafiza Hamid
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e-mail: iemt-emap2016@crest.my
Web: http://ewh.ieee.org/r10/malaysia/cpmt/Home/iemt/2016/iemt2016.html

IIRW 2016

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INVENTOR'S CORNER |

THE ART AND SCIENCE OF INVENTION: BECOMING A BETTER INVENTOR

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Over the years I have been a fairly prolific inventor, with more than forty U.S. patents issued. When people hear this number, they often ask, “How can you be so inventive?” I sometimes answer, “I listen to the noise in my head and throw out the obvious nonsense.”

However, upon pondering this question for some time, I realized that the inquirers were in fact asking the wrong question. The greater question is: “Why do they think they are **not** inventive?”

Let’s start the answer to that question with a definition of *invention*. Most of the dictionary definitions are a bit circular. The one I like is “an act or instance of creating by exercise of the imagination.” Creating implies something new. U.S. patent law makes some fairly strong statements about what *new* means in regards to obtaining a patent. However, an invention can simply be something new to you. Some of my favorite inventions never made it to becoming a U.S. patent.

One “invention” that I recall with fondness occurred during a lunch meeting where several start-up companies were pitching their ideas to potential angel investors. One company was promoting low-sugar sodas with flavors such as cucumber and lavender as a nonalcoholic, fine-dining beverage option. The company had placed several bottles of its sodas on each lunch table for the assembly to try. As the representatives began their pitch, I picked up a bottle, noticed it did not have a twist-off cap, and looked around for an opener.

Not finding one, I looked at nearby tables and saw others going through the same search pattern. Not one to be deterred by such an oversight, I picked up a table knife and used it to gently pry the cap off the bottle.

Upon seeing me drinking the soda, others at my table and nearby tables began asking how I had opened the bottle. I showed them how to do it, and the technique was passed around the room. Comments of “How did you figure that out?” and “How did you know that would

work?” came my way. Let’s take a look at these two questions.

The “figuring it out” had to do in part with understanding how a bottle opener works. It is basically just a pry bar with a fulcrum set in the front that is placed in the middle of the cap. The back pry surface is placed under the rim of the cap. Leverage is used to stretch out a segment of the bottom part of the cap until its grip is pulled away from the bottle rim and the cap is released. Use of a medium-soft metal for the cap is part of the overall success of both attachment and removal.

It also did not hurt that I recalled an old John Wayne movie in which beer bottle caps were removed by placing the cap rim against the edge of the bar and banging it with one’s palm. Warning: Damage to the bar occurs, and a lot of beer goes flying, making for unhappy bartenders.

So, the combination of understanding and the recognition that anything which applies sufficient force to the bottle cap is an opener led to a search of the table for a suitable lever. In this case, a table knife came to mind.

I imagined using the tip of the table knife to slip under the cap edge, pry up a small portion, move the knife tip to an adjacent section, and repeat until the cap released. How did I know this idea would work? I didn’t. But the worst that could happen would be to mar the knife or maybe look a little foolish prying away at the cap. So, I ran a test of my prototype bottle opener and met with success.

Children use their imaginations to create all the time. As adults, we are too often taught away from this process—it is “too childish.” Moreover, acting on these flights of fancy involves risk: the invention may not work. As we age, we tend to become more conservative and risk-averse. The first part of invention is to allow oneself to truly “listen to the noise in your head.” That noise is your imagination at work. Your imagination is still there, trying to get your attention. With practice, you can learn to let it out, although I advise not doing so while driving.



INVENTOR'S CORNER |

The second part of invention is learning to observe things in a more general sense. A bottle opener is generally a pry bar. The primary purpose of a knife is to cut things into smaller pieces, but knives can be readily repurposed:

- They make an acceptable emergency screwdriver.
- Prior to forks and spoons, they were the primary eating tool.
- They are a great tool for cleaning crevices.

As adults, we tend to focus on and accept the given use. As children, we play with the alternatives without concern of looking foolish.

My first patentable invention (U.S. Patent 4,611,912) was a laser distance-measurement tool, or ladar. (*Ladar* is a take-off on *radar*, with *laser* substituting for *radio*.) The invention sticks in my mind in part because I had never heard of a ladar until I invented one. It also represents the above principles coupled with one more: turning a problem into an advantage.

At the time of the invention, my coworker and I had been asked to attend a presentation on these new things called laser diodes that were coming out of Japan. During the presentation, the diode manufacturer was forced to admit that the lasers would chirp in frequency while they were modulated. This was a potentially big problem for many applications, but my coworker and I could hardly contain our excitement. After asking a few questions about the nature of this chirp, we moved on. When outside the

meeting, I asked my coworker, “Are you thinking what I’m thinking?” Sure enough, we had both come up with the idea of a heterodyne chirped radar approach to range-finding distance, but using a laser instead of microwaves. My personal patenting career (as well as a rapid shift into becoming a ladar expert) took off by taking what, to everyone else in the room, was a detrimental effect and turning it into an asset.

As a task toward making yourself more inventive, see what you can come up with as a substitute for that remarkable bit of technology called a pencil. What is so remarkable about a pencil?

- It leaves marks on a multitude of surfaces with minimal pressure.
- The marks are fairly permanent but can be erased if necessary.
- It fits nicely into one’s hand.
- It can be readily resharpened to make narrow lines.

Note that your “invention” does not need to be earth-shattering or a viable substitute for a pencil. The point of the task is to encourage yourself to let go and rethink a very common item, that is, release your imagination.

“Listening to the noise in your head” is not an idle pastime. It exercises your imagination, serves as the pathway to turning a problem into a solution, and makes you a better inventor.



NOTEWORTHY NEWS |

ITC 2016

The International Test Conference (ITC) will be held **November 15 to 17, 2016**, at the Fort Worth Convention Center in Fort Worth, Texas. ITC is the world’s premier conference dedicated to the electronic test of devices, boards, and systems and covers the complete cycle from design verification and validation, test, diagnosis, failure analysis, and back to process, yield, reliability, and design improvement. At ITC, test and design professionals can confront the challenges the industry faces and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

ITC, the cornerstone of TestWeek events, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including formal paper sessions, tutorials, panel sessions, case studies, a lecture series, commercial exhibits and presentations, and a host of ancillary professional meetings.

ITC is sponsored by the IEEE. For more information, visit itctestweek.org.





LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Beam-Based Analysis Techniques

Michael R. Bruce, Consultant
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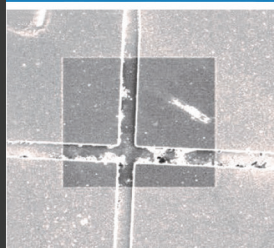
The current column covers peer-reviewed articles published since 2014 on beam-based analysis techniques, including atomic, electron, neutron, ion, and x-ray beam technologies. These technologies typically offer the highest resolution, sometimes down to the atomic level; in addition, focused ion beams are fundamental to modifying electronic circuits. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

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How to Identify and Solve Your SEM Contamination Problem

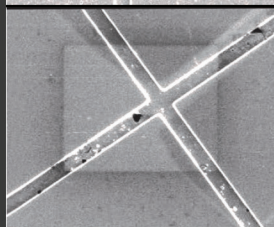


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NOTEWORTHY NEWS

2017 IRPS CONFERENCE

The IEEE International Reliability Physics Symposium's (IRPS) annual conference will be held **April 2 to 6, 2017**, at the Hyatt Regency in Monterey, Calif.

The deadline for submission of paper and poster abstracts is October 15, 2016. IRPS 2017 is soliciting increased participation in the following areas: system reliability; middle-of-the-line; extrinsic defect impact on yield and reliability; and commercial off-the-shelf components in high-reliability applications, including screening, derating, case studies, design considerations, and so on.

The IRPS Conference is sponsored by the IEEE Reliability Society and IEEE Electron Device Society. For more information, visit the IRPS website at irps.org.





GUEST COLUMNIST |

2.5- AND 3-D TSV TECHNOLOGY APPLICATIONS AND FAILURE ANALYSIS CHALLENGES

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The semiconductor industry has followed Moore's law in the last four decades. However, transistor performance improvement will be limited, and designers will not see doubling of frequency every two years. The need for increased performance and further miniaturization has driven the development of advanced packaging solutions, such as fan-in wafer-level chip-scale packaging, fan-out wafer-level packaging, wire-bonded stacked dice, and package-on-package. These technologies are used in mass production and provide significant benefits in form factor but may not give the desired improvement in die-to-die bandwidth. Recently, 3-D integrated circuits (ICs) that employ vertical through-silicon vias (TSVs) for connecting each die have been proposed. It is an alternative solution to existing package-on-package and system-in-package processes.

The use of 3-D chip stacking with TSV technology promises future improvements, such as reduced signal delay and greater bandwidth, along with the possibility of allowing heterogeneous integration of process technologies, a small form factor, and higher speeds with lower power consumption than designs with multiple chips on a printed circuit board. In addition, compared with traditional 2-D multicore or many-core architectures, the 3-D IC can address the major memory bandwidth problem by stacked memory architecture. In June 2015, Advanced Micro Devices launched the first 2.5-D TSV Fiji product (Radeon Fury), which incorporates DRAMs stacked vertically on each other (high bandwidth memory) and 22 discrete dice manufactured by various companies that are integrated into one single package. It is the first TSV with microbumps for die stacking used in the graphics market with implementation of high-volume manufacturing. The 2.5-D TSV Fiji product has delivered faster performance than the previous-generation GDDR5 technology.

Tremendous work has been done so that products can be manufactured using 3-D silicon integration technology. Many challenges have been addressed, including design complexity, electrical signal integrity, thermal management, heterogeneous die integration, manufacturing

"RECENTLY, 3-D INTEGRATED CIRCUITS (ICs) THAT EMPLOY VERTICAL THROUGH-SILICON VIAS (TSVs) FOR CONNECTING EACH DIE HAVE BEEN PROPOSED. IT IS AN ALTERNATIVE SOLUTION TO EXISTING PACKAGE-ON-PACKAGE AND SYSTEM-IN-PACKAGE PROCESSES."



yield, reliability, and quality. To resolve issues and find solutions, failure root-cause analysis is very critical to ensuring successful 3-D IC silicon integration.

Current failure analysis techniques and tools are well established to support 2-D products. However, they have not been widely developed for 2.5- and 3-D TSV products, and there are still many unresolved challenges.

One of the first challenges to be addressed is TSV inspection. Typical TSV dimensions are 5 to 10 μm in diameter, with aspect ratios preferably around 10 or more. It is not an easy task to etch and properly fill TSVs having such large aspect ratios. Some of the new challenges are metrology and inspection for TSVs and wafer backside processing control, as well as multilevel dice stacking. Currently, visual inspection with infrared interferometry is the common methodology used in manufacturing production; however, it cannot capture all defects, such as TSV voids or insulator defects (pinholes) inside the TSVs. Research revealed that high-frequency scanning acoustic microscopy (SAM) (gigahertz range) and 3-D x-ray-based inspection systems can be used for detecting TSV voids approximately 1 μm or more in diameter. Another new approach for destructive analysis inspection of TSV defects is the plasma focused ion beam (FIB), which can produce high throughput with approximately 50 \times faster milling rates compared to conventional dual-beam FIB for preparing a cross section. Several FIB vendors, such as FEI,

Tescan, and Zeiss, have made significant progress in the plasma FIB technique.

Real-time x-ray (RTX) inspection is a very common and widely used FA technique for 2-D products; however, it does not work well for 3-D geometries. Nanofocus and microfocus 3-D RTX has been successfully applied to 3-D TSVs. 3-D x-ray tomography with sufficient resolution (X, Y, Z), throughput, and price is necessary to enable routine nondestructive inspection of critical defects at the assembly site. How to improve the resolution and throughput is a challenge for the 3-D RTX technique.

Time-domain reflectometry (TDR) has been successfully used to isolate open/short package-level failures. With technology shifting to 3-D TSVs, conventional TDR is reaching its resolution limits. Recently, a terahertz TDR called electro-optical terahertz pulsed reflectometry (EOTPR), with a promising resolution of $<10\text{ }\mu\text{m}$, was applied to 2.5- and 3-D IC products. EOTPR has demonstrated increased distance-to-defect accuracy. The key factor in using EOTPR to isolate 3-D IC failures is setting up full 3-D device-under-test modeling.

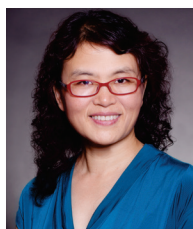
Conventional thermal emission techniques, such as optical-beam-induced resistance change and thermal-induced voltage alteration, are limited for isolating package-level short failures due to vertical Z resolution. Lock-in thermography (LIT) is a new technique that has been developed for on-die defect localization through homogeneous-covering package material. Moderate lock-in frequencies ($<25\text{ Hz}$) yielded sufficient layer resolution in the vertical direction. The challenge of LIT for 2.5- and 3-D TSVs is setting up reference measurements. Some failure analysis results suggest that increasing LIT frequencies ($>100\text{ Hz}$) can obtain clear differentiation of relevant layers and align measurement results with theory calculation. Lock-in thermography as a new technique can fulfill failure analysis requirements for the 3-D IC approach. Magnetic field imaging is another fault isolation technique that has been applied to 2.5- and 3-D TSVs. It uses magnetic current imaging to allow current 3-D

mapping and extraction of geometrical information about current location at every chip level in a 3-D stack. Yet to be resolved are the challenges of isolating silicon transistor defects through the silicon backside to overcome interferences induced by 3-D TSVs and backside metallization for conventional photon emission microscopy, time-resolved emission, and laser voltage probing techniques.

Last but not least, the challenge of using SAM for 2.5- and 3-D TSVs has been raised. It is very difficult for acoustics to penetrate stacked thin dice with mixed interconnects and silicon vias. Conventional SAM resolution XY is approximately $25\text{ }\mu\text{m}$, and penetration depth is approximately $0.1\text{ }\mu\text{m}$. Currently, ongoing SAM development that includes time-domain analysis, transducer development, and higher power pulses to improve penetration depth with high resolution has been achieved, and some of these advancements have been applied to 2.5-D TSVs. However, many challenges remain.

Collaboration is needed between academic institutes, industry, and equipment vendors to develop new techniques and tools to meet 3-D IC failure analysis requirements and to provide solutions for overcoming the challenges of making 3-D stacked ICs a reality.

ABOUT THE AUTHOR



Lihong Cao was a Senior Manager at Advanced Micro Devices, where she was responsible for global package failure analysis to support new product and package development, qualification, production, and customer issues. She also was in charge of new failure analysis technique development and the roadmap for package failure analysis. Dr. Cao specializes in new package development, assembly, and failure analysis for a variety of products. She received her Ph.D. in materials science and engineering. She has published more than 100 technical papers and holds several U.S. patents.

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NOTEWORTHY NEWS

IEDM CONFERENCE

The 2016 IEEE International Electron Devices Meeting (IEDM) will be held **December 5 to 7, 2016**, at the Hilton San Francisco Union Square in San Francisco, Calif. IEDM is a forum for reporting breakthroughs in technology, design, manufacturing, physics, and the modeling of semiconductors and other electronic devices. Topics range from deep-submicron CMOS transistors and memories to novel displays and imagers, from compound semiconductor materials to nanotechnology devices and architectures, from micromachined devices to smart-power technologies.

The IEDM is sponsored by the IEEE Electron Devices Society. For more information, visit the IEDM website at ieee-iedm.org.



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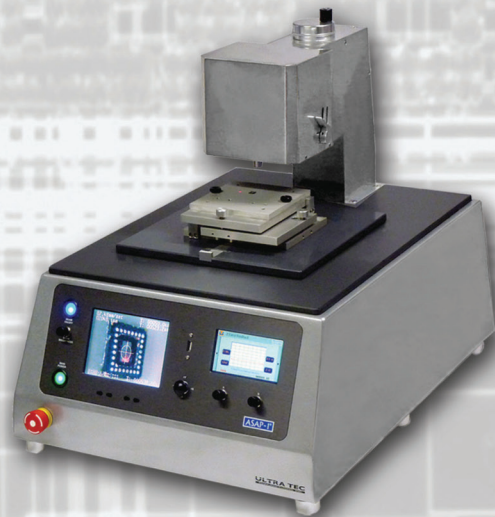
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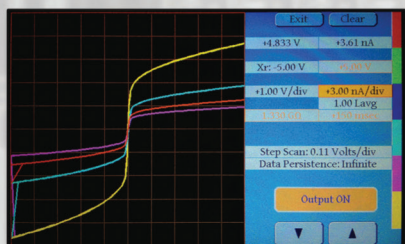
REALTIME FA

The Convergence of Sample Prep & Analytical Methods

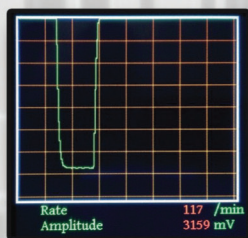


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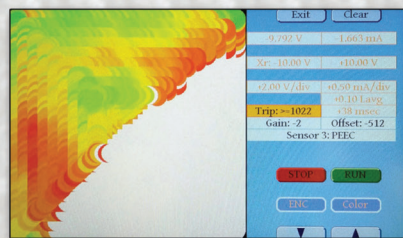
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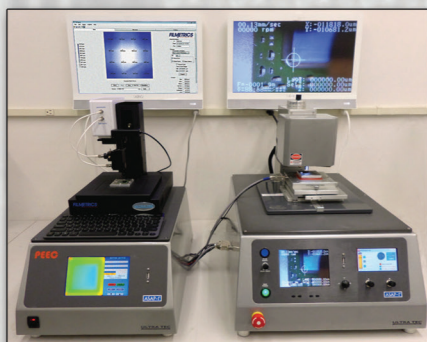


Oscilloscope



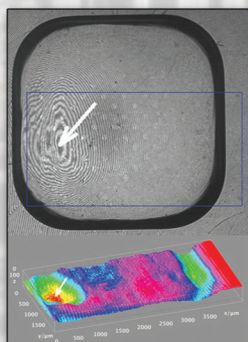
Plot Screen

ULTRATHIN with Confidence

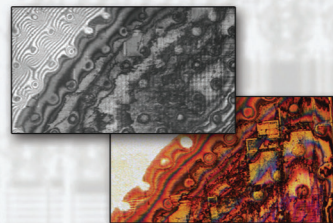


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NIR image top shows the thinnest area on a thinned- deliberately tilted die. Lower image shows a C-SPM scan made on ASAP-1 IPS of the same area showing a consistent point of minimum RST.



NIR and VISIBLE Images show the same position as the Plot screen for silicon breach

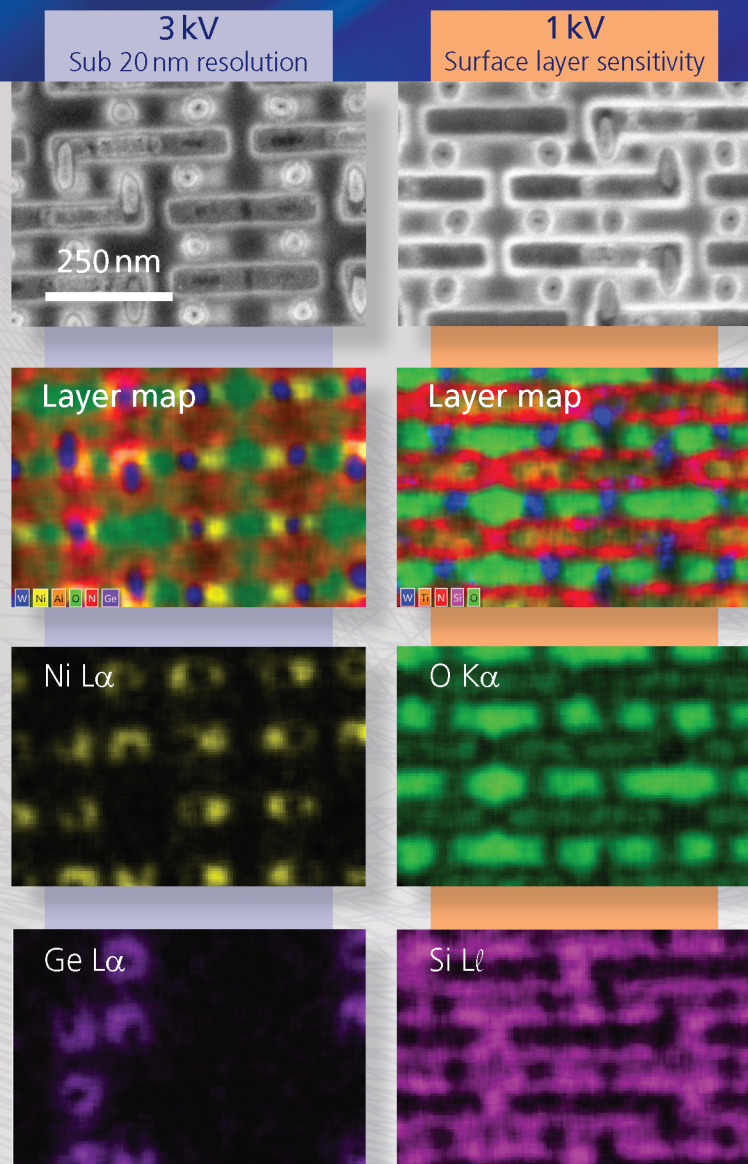


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