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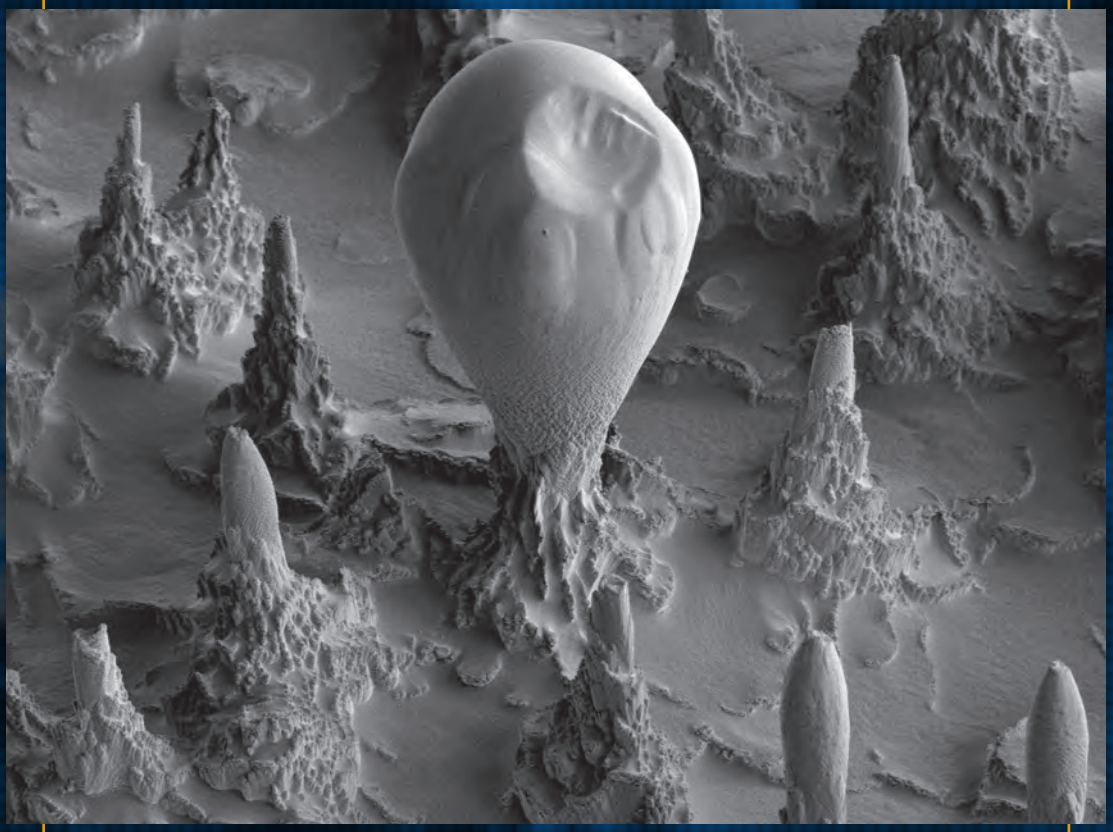

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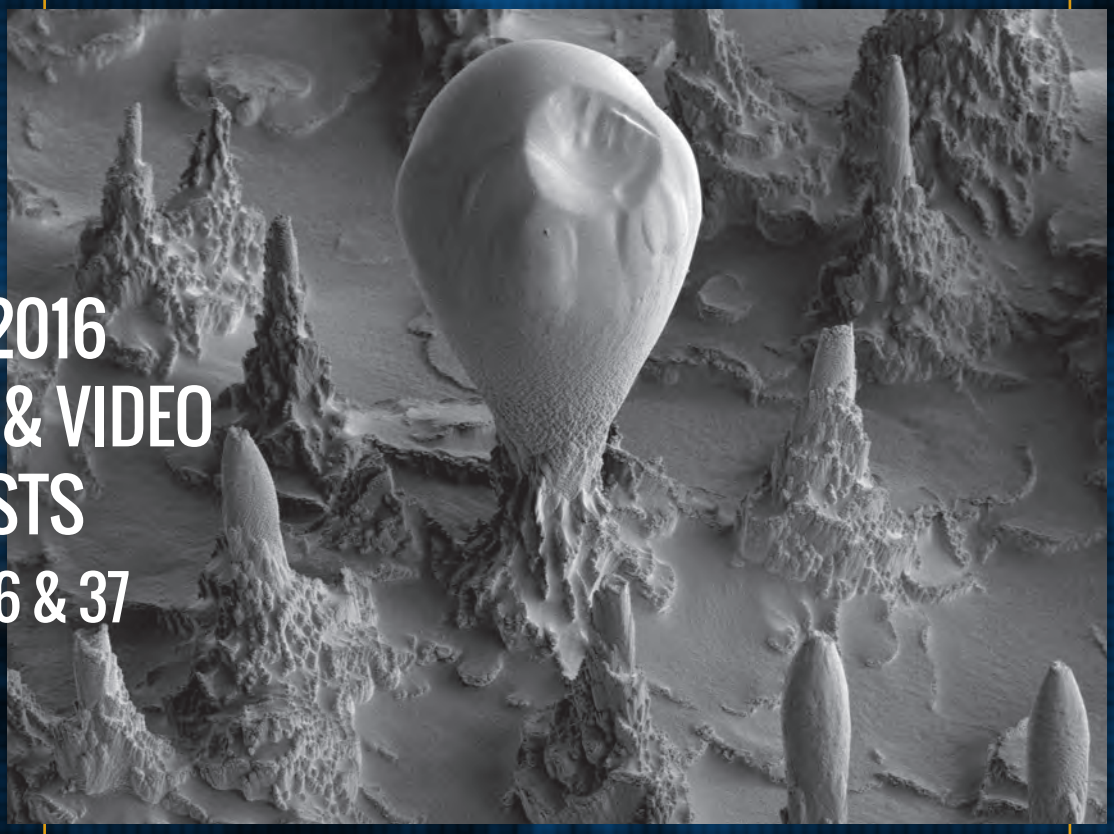

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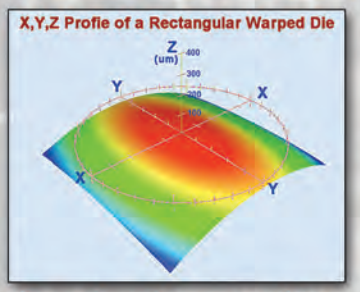

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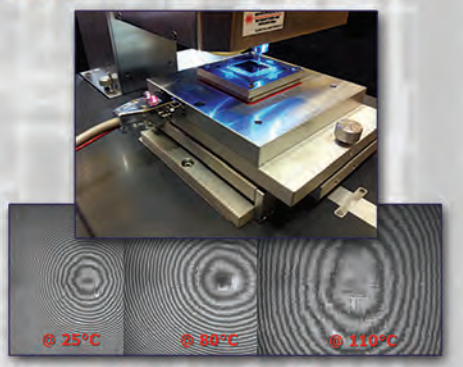

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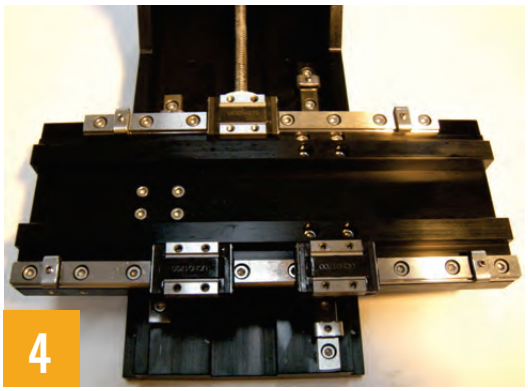
ABOUT THE COVER

Interior of a quartz tube, after repeated exposure to a plasma, revealed spikes and bulbous spires. These formations would break off and contribute to wafer surface defectivity. *Photo by Noel Forrette, IM Flash Technologies, LLC, First Place Winner in Black & White Images, 2015 EDFAS Photo Contest.*



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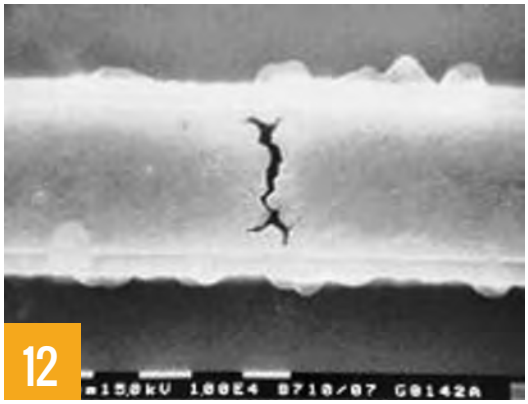

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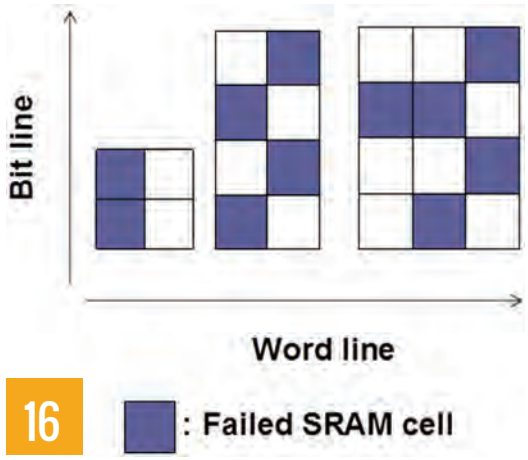

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PURPOSE: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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GUEST EDITORIAL

ARE TODAY'S TOOLS MEETING FA'S NEEDS?

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Technologies are still moving to the nanometer scale, with the technology node already at 14 nm, new materials with high-k dielectric and metal gates, new transistor architecture with FinFETs, complex multicore architectures, and very high-density integration. All the design tools, including design for test, design for manufacturing, and design-in reliability, have been refined and merged to speed up time-to-market and improve yield and reliability, while the latest wafer fabs are already well equipped to manufacture up-to-date and future very-large-scale integration (VLSI). Nevertheless, failure and technological analyses are still mandatory to solve unforeseen issues and to optimize the whole process. This creates incredible challenges for tool manufacturers to fulfill the needed optical resolution for backside analysis, to develop new nanoprobing tools for electrical characterization, and to target ultimate physical and chemical resolution (analytical transmission electron microscopy, atomic probe, etc.). Developing these tools is more and more expensive, while up-to-date wafer fab facilities and the design cost of ultimate VLSI allow fewer and fewer players and factories into the market. One of the results is the high cost of tools, and another result, more linked to device technology, is the need for more and more skilled specialists to manage the analysis and to interpret the analysis results. Fortunately, the mass-market economic impact is so high that integrated circuit (IC) manufacturers are continuing the effort to obtain the necessary tools and to pay the right price for them. Therefore, there is a kind of balance that smooths the trends of fewer customers and more expensive tools on one side versus motivated IC manufacturers on the other. In this ultimate technology field, today's tools are meeting our needs, and we can remain quite confident for the next several years, but not forever, regarding the technical, scientific, and cost challenges that tool manufacturers face in developing new tools. This problem has been clearly identified, and the first Circuit Analysis Tool program has been set up to help develop needed tools and techniques.[1]

However, we cannot reduce failure analysis (FA) to this market. There are other concerns that challenge the tools and techniques we have, primarily the more-than-Moore field, which has both 3-D integration and multiphysics components. If we consider 3-D integration, one of the main challenges faced by FA engineers is the lack of transparency in 3-D devices. So far, only electromagnetic fields, acoustic waves, thermal waves, x-rays, and electrical signaling through conductors can be used. Impressive efforts have been made by tool manufacturers to address shorts and opens. Magnetic microscopy, lock-in thermography, and terahertz reflectometry have been successfully used, but is there any tool and technique capable of localizing soft defects

(continued on page 51)

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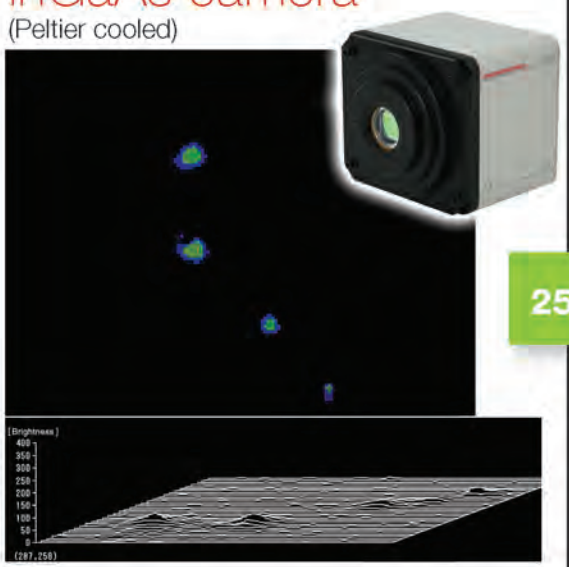

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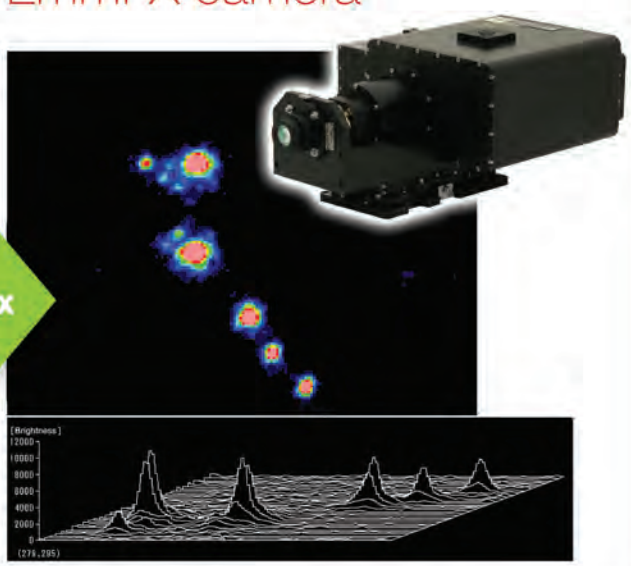

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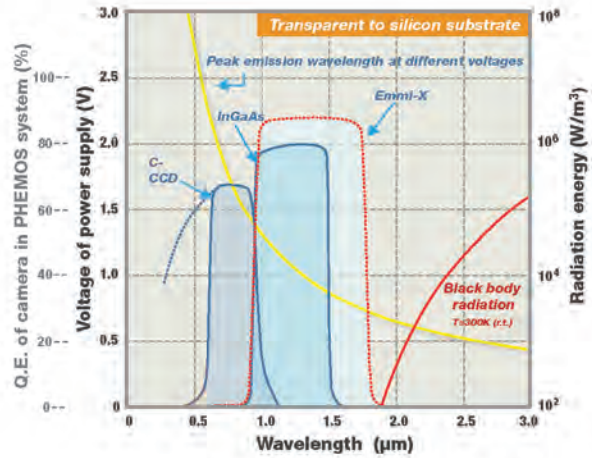

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A DISCUSSION OF THE MECHANICAL LIMITATIONS OF MACHINERY USED FOR SAMPLE-PREPARATION PROCESSES

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INTRODUCTION

Many semiconductor failure analysis sample-preparation procedures require mechanical machining processes. These processes include removing encapsulant, removing heat spreaders, cutting of the sample for cross sectioning, package substrate printed circuit board delayering, die thinning by grinding and polishing, die delayering, and many others. The machines used for mechanical sample preparation have ultimate limitations based on the machine's accuracy, resolution, repeatability, and environmental effects. These limitations can/may affect the results of the sample-preparation process. Limitations to ultimate performance include the intrinsic machine resolution, accuracy, and repeatability of the tool-positioning system as well as tolerance limitations resulting from the tool bits, pads, and other consumable components. Note that a *tool,* as used here, is an end mill, a grinding tool, a saw blade, or other simple functional device. A *machine,* or machine tool, is what utilizes a tool to perform a specific task. A milling machine is a machine. The end mill it uses is a tool.

A BRIEF DISCUSSION OF TERMS

The dictionary definition of *accuracy* is "the extent to which a given measurement agrees with the standard value for that measurement."[1]

The standard used as the "standard value" generally is a National Institute of Standards and Technology (NIST) traceable length standard with an absolute tolerance defined by the reference standard and class. A length reference is normally a gauge block. A gauge block is a piece of metal having flat and parallel opposing gauge surfaces (Fig. 1). A grade 2 NIST 100 mm gauge block matches the NIST reference standard to +0.0003/−0.00015 mm, but only at the standard conditions:[2]

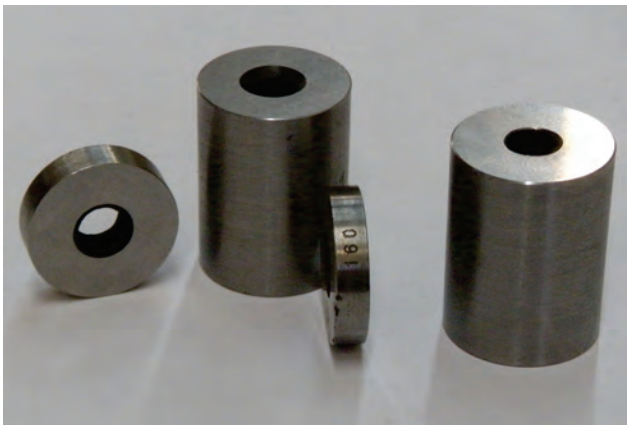

Fig. 1 **Representative cylindrical gauge blocks**

- Temperature = 20 °C (68 °F)
- Barometric pressure = 101,325 Pa (1 atm)
- Water vapor pressure = 1333 Pa (10 mm of mercury)
- CO_2 content of air = 0.03%

The steel of the gauge block expands with increasing temperature at a rate of 11.5 ppm/°C.[2] A 1° increase in temperature of the 100 mm gauge block will result in a dimensional change of 0.00115 mm, or nearly three times its specified accuracy.

The dictionary definition for *resolution* is "the fineness of detail that can be distinguished."[3] When taking any measurements, there is a limiting fineness of the measurement, as determined by the measurement reference. When using a ruler marked with only 1 mm increments, a length can only be determined to the nearest 1 mm. If the ruler's overall length is off by 10%, the measurement can still be taken to a 1 mm resolution. Resolution is not a function of accuracy.

The definition of *repeatability* is "the variation in measurements taken by a single person or instrument on the same item and under the same conditions."[4]

The easiest way to illustrate the difference between accuracy and repeatability is to refer to the rifle target in Fig. 2. A tight grouping is repeatability.

In addition to these terms, the geometric properties of parallelism and orthogonality determine the performance of a mechanical system.

Simple mechanical devices used for sample preparation, such as diamond saws, dimplers, and many others, have easy-to-understand mechanical systems, and as long as they are properly maintained and calibrated, they will perform their designated tasks. With simpler machines, if the quality of the results is lacking, then service and adjustment are required.

A more complex machine is the flat lapper. There are two basic types of lappers: open face, where the sample being lapped is mounted to a fixture that is placed inside or attached to a rotating ring, and lappers with a mast that supports a sample holder and provides sample rotation and movement across the lap surface. Either type can use abrasive lapping films or a slurry feed system. Critical parameters on a lapper include axial runout, lap flatness, and the parallelism of the rotational, scan, and lap spindle axes. The axial runout is the variation in height of the lap surface at the edge as the lap rotates. For controllable results with any lapper, the lap should be flat and not have axial runout. The parallelism of the rotational, scan, and lap spindle axes determines the surface shape of the sample. Axial runout will produce scalloping at the sample edges. Lack of parallelism of the rotational axis will produce a conical surface. Lack of parallelism of the scan axis will produce a spherical surface. Aligning all three axes is difficult to impossible, depending on the machine, but it is necessary if die delayering is to be done. A 1 or 2 μm axial runout on the lap, or the rotational axis not being parallel to the spindle, or the scan axis not being in line will produce a nonplanar result. The geometries of the inaccuracies are easy to calculate. A 0.02 mrad misalignment of the sample holder rotational axis will produce a 10 mm^2 sample with the corners more than 100 nm lower than the center. When delayering, this conical shape can make the results unacceptable. Accuracy depends on set-up adjustments for the machine. Ongoing successful sample preparation depends on maintaining these adjustments. Periodic adjustments may need to be performed by a specially trained technician or engineer.

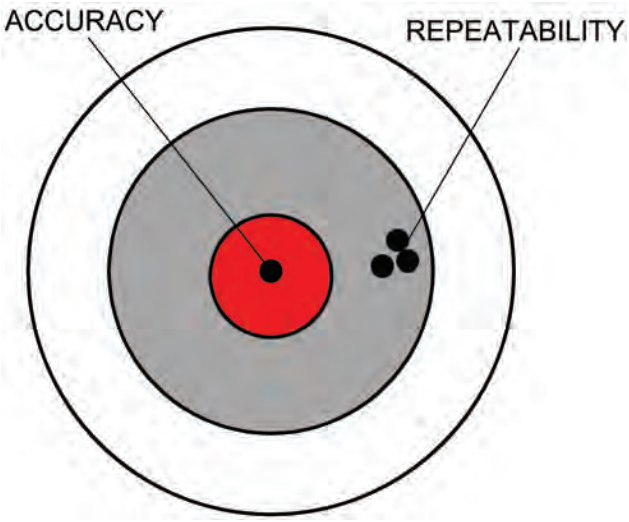

Fig. 2 Accuracy as opposed to repeatability

"IN LINEAR POSITIONING SYSTEMS, SUCH AS USED ON THESE MACHINES, THE LINEAR MOTION IS COMMONLY PRODUCED WITH A LEAD SCREW, AND THE POSITION IS MEASURED BY A LINEAR ENCODER AND SCALE."

THREE-AXIS-MOVEMENT MACHINES

There are machines available for die thinning or delayering that have movement in three axes as well as a rotating spindle that holds the tool. It is with these machines that the concepts of accuracy, resolution, and repeatability are most relevant. These machines move a tool over the die surface by moving the sample in the *X* and *Y* axes and moving the tool in the *Z* axis.

In linear positioning systems, such as used on these machines, the linear motion is commonly produced with a lead screw, and the position is measured by a linear encoder and scale. A computer controls the motor driving the lead screw so that the encoder gives the desired position value. The encoder has specifications for linearity and resolution and, occasionally, zero reference repeatability. In a numerically controlled machine, there is always a reference or zero point that is periodically checked to establish a positional reference. This is almost always at the extreme travel of the machine in *X* or *Y*, while most work is done near the center of the travel. The temperature effects on the linear encoder scale then alter all positional values by a function of the total travel from the zero point. This means that the longer the travel, the greater the zero shift produced by temperature changes. A machine with 200 mm of travel will have twice the thermal zero shift as a machine with 100 mm of travel.

In addition to the temperature effects, there is a tolerance on the zero position. This is a result of the switches used to detect when an axis is at the zero position. These switches may be mechanical, optical, or magnetic. No matter which type of switch is used, it will have some level of uncertainty that results in uncertainty in the zero position.

The resolution of the machine is a function of how well the scale can be measured by the linear encoder. A good encoder can provide positional resolution of 50 nm, but the accuracy is a function of the scale.[5] A typical optical scale will have a nonlinearity of 0.005 mm per meter of travel and a thermal expansion coefficient (T_c) of the material to which it is mounted.[5] Steel has a T_c of 11.5 ppm/°C, and the T_c for aluminum is 23 ppm/°C. A 100-mm-long scale will change 0.0023 mm/°C. All of this is additive. The uncertainty due to scale resolution adds to the nonlinearity, zero position uncertainty, and the thermal variations of the scale. With a typical ±2° variation in temperature and a 100-mm-long scale, zero uncertainty of ±0.5 µm, and the scale nonlinearity, the positional uncertainty is ±5.6 µm. This is 110 times greater than the encoder resolution.

THE CONCEPT OF UNCERTAINTY

Uncertainty is the ultimate tolerance on any positional move. The factors that affect uncertainty are repeatability, accuracy, geometric factors, interaction between the axes of movement, and environmental effects. The repeatability, as shown in Fig. 2, will drift in position resulting from temperature effects, and the pattern center will move as a result of the other factors. Repeatability will always be less than uncertainty.

THE GEOMETRY OF MACHINE PERFORMANCE

All machines involve linear and rotational movement. Most machines involve multiple-axis movements. The geometric relationship of the axes to each other will directly affect the position in the other axes as movement takes place. If the *X* and *Y* axes are at 89° instead of 90°, a move in either axis will produce a positional shift of 1.745% of the move in the other axis. Resolution, accuracy, and repeatability in one axis are meaningless if the axes are not truly orthogonal. If the *Z* axis is not normal to the *X-Y* plane, changes in *Z* position produce changes in the tool tip's position referenced to the *X-Y* plane.

Determining axis uncertainty requires knowing the geometric relationships of all three axes and the rotational axis of the tool. This requires the manufacturer to specify the orthogonality of the axes to each other and the normality of the *Z* axis and spindle to the *X-Y* plane (Fig. 3). Although the geometric variables do not directly affect the repeatability, the interaction in position from geometric inaccuracies makes each axis's real position a function of the other axes' positions.

In addition to the geometric problems, the runout of each axis also must be considered. The linear bearings or linear positioner used in each axis have runout in the perpendicular axes. A typical precision-grade profile linear bearing will have 2 µm runout in the vertical and horizontal axes.[6] That is, as the linear bearing is moved, it can move a small amount vertically and horizontally. Even super-precision bearings have a runout of 1.5 µm. The runout in one axis adds directly to the positional uncertainty of the other two axes. The runout also produces rotation about each axis as a function of the separation between the bearings used. As an example, Fig. 4 shows a single axis using four linear bearings on two profile rails in a square pattern:

- A 2 µm horizontal and vertical runout in *X* will produce ±2 µm movement in the *Y* and *Z* axes.
- The rotation possible is a result of +2 µm on one bearing and −2 µm on another. The pitch is then a function of the bearing spacing. The yaw becomes a function of the rail spacing.
- The pitch and yaw affect true position in all three axes according to the geometric relationships and the distance from the sample to the axis plane.

All of these variables directly add to other sources of positional uncertainty. Vertical runout on the *X* axis bearings adds directly to the uncertainty of the *Z* axis

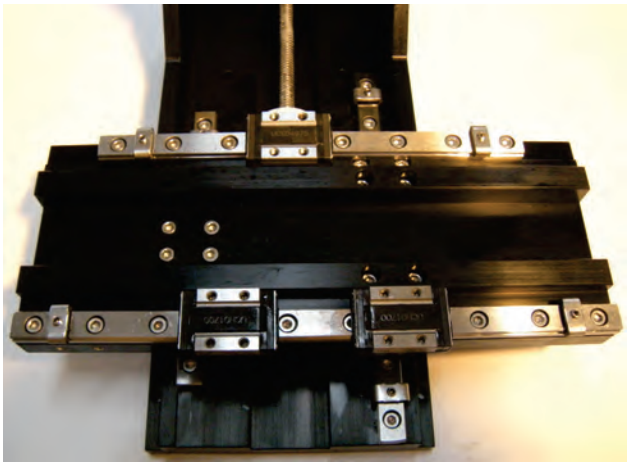

Fig. 3 **Typical *X-Y* movement mechanism with the *X* axis stage removed. There are three bearings instead of four on each axis, although the runout and orthogonality effects are the same as in the text.**

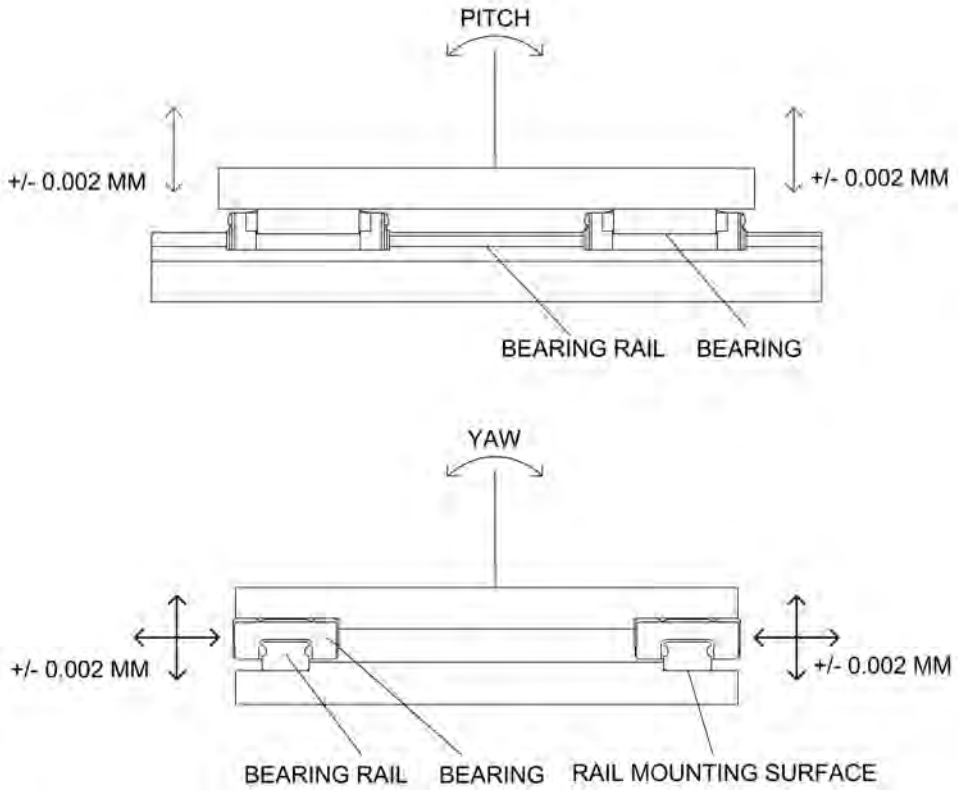

Fig. 4 **Linear bearing arrangement and the effects of runout**

position, and the horizontal runout adds directly to the *Y* axis uncertainty.

PROCESSES FOR BACKSIDE THINNING

Backside thinning of a sample often requires the removal of encapsulant, die-attach pad, and die-attach adhesive. These processes are usually defined by the position of the extreme edge of the cutting tool. As the tool is rotating, the eccentricity of the tool and spindle and the actual tool diameter all determine the location of the extreme cutting edge. A typical end mill will have a diameter tolerance of ±13 µm[7] or more. A very good spindle and collet for securing the end mill to the spindle may have a runout of ±7.6 µm.[8] The runout is a function of the concentricity of the spindle to the collet axes. The end mill may also have runout that results from the cutting edges not being coaxial with the shank. All of this makes the uncertainty of the edges of the machined area ±20 to 25 µm from tool and spindle tolerances alone. A desire to define the machined area to ±1 µm requires that the running tool and spindle inaccuracies be taken into account. This can only be done in situ. That is, an operator must adjust the machined area during machining. Once this is done, the repeatability of the *X-Y* movement only needs to be within the desired positional tolerances to produce an acceptable result.

Adjusting tool position and travel during operation is problematic. Attempts to have video viewing during operation are often obscured by slurry and swarf. Because the video camera cannot view directly down the tool axis, there must be some parallax. The parallax makes any *Z*-positional movement also appear to be a movement in the *X-Y* plane. Moving the sample to a viewing position creates measurement and correlation problems.

When thinning a die to a measured surface contour, *X*- and *Y*-positional uncertainties have an effect on the *Z* position due to the surface profile. The maximum slope of the profile, multiplied by the *X-Y*-positional uncertainty, adds to the *Z* axis positional uncertainty when determining the overall profile reproduction uncertainty. A slope of 20 µm/mm will add to the *Z* axis uncertainty as the *X-Y*-positional uncertainty (in mm) times the 20 µm/mm slope. Therefore, a ±5 µm *X-Y* uncertainty will introduce an additional *Z* axis uncertainty of 0.1 µm.

WHAT IS REQUIRED

The system repeatability must be equal to or slightly less than the desired positional accuracy. If a machined pattern must be maintained at ±1 µm, then the repeatability of *X-Y* positioning must be 1 µm or less. A resolution of less than one-half of the positional uncertainty is

unnecessary and only increases the cost of the system. The *Z* axis uncertainty must be equal to or better than the required profile integrity. If it is desired to reproduce a surface profile to ±1 µm, the *Z* axis repeatability need not be less than 0.5 µm. If *X-Y*-positional repeatability is not constrained directly, it can be defined as the maximum profile slope divided by the *Z* axis maximum uncertainty. Therefore, if a 1 µm *Z* axis limit is required, and the maximum profile slope is 20 µm/mm, the *X-Y* uncertainty needs only to be less than 50 µm. Nowhere is there a requirement for 50 nm resolution in any axis or "submicron" accuracy.

If a machine is required to thin plastic-packaged devices and produce a thinned die with less than ±5 µm in thickness variation, the following specifications are all that are required. Tighter specifications only result in increased purchase and maintenance costs:

- *X* and *Y* axis resolution: 1.0 µm
- *Z* axis resolution: 0.5 µm
- *X, Y* axis independent repeatability: 2.0 µm
- *Z* axis independent repeatability: 1.0 µm
- Spindle runout: 10 µm
- Axis orthogonality: 0.05 mrad, maximum
- Variation from straight line travel: 0.003 mm per 25 mm of travel, including runout
- Axis pitch and yaw: 0.05 mrad, maximum
- Stage deflection: 50 Newtons/µm, maximum

The axis resolution defines the minimum required scale resolution. It should be 50% or less of the repeatability. The spindle runout limits the effective increase in tool diameter caused by "wobble." The axis orthogonality and axis pitch and yaw each limit axis-to-axis interaction to 0.05 µm per millimeter of travel. Because all materials and machines are elastic, the stage deflection specification is required to limit the *Z* axis positional change as a result of the tool forces.

In total, over a 25 mm^2 area, the *X-Y*-positional uncertainty is approximately 15 µm with 2 µm repeatability. The *Z*-positional uncertainty is approximately 11 µm with repeatability of less than 2 µm. Any more than this is unnecessary and costly, and any less does not guarantee performance.

The axis positional uncertainty comes into play if the surface profile is measured by different equipment. If this is done, all of the positional uncertainties of both the measuring system and the processing machine add. Because the positional uncertainty is much greater than repeatability, the integrity of profile reproduction comes into question.

FRONTSIDE DELAYERING REQUIREMENTS

Delayering requirements are much more complex. Delayering on a flat lap requires that the device rotational axis and the scan axis be parallel to the platen rotational axis to a degree of precision that is not normally encountered. Maintaining 10 nm planarity of a 10 mm^2 die sample requires that all axes be within 0.002 mrad. In addition, the vertical runout of the platen must be less than 0.2 µm. Measuring the runout is problematic, as are the alignment measurements, but all are possible with the right measurement equipment and personnel. Delayering on a backside thinning machine is even more problematic because axis alignment is either not available or difficult to adjust to the accuracy required. Delayering requires that the spindle be orthogonal to the *X-Y* plane within 0.0067 mrad for a 3-mm-diameter tool. A larger tool diameter tightens the requirements. Normally, the spindle orthogonality of a backside system is more than 10 times that required to do die delayering. Additionally, 10 nm *Z* axis repeatability is not truly available. This indicates that using a flat lap is difficult and using a backside thinning system is not realistically possible. If one is delayering a 5 µm design-rules die, almost anything can be used. Currently for the latest design rules, only a very carefully set up flat lap can meet the requirements.

CONCLUSIONS

Claiming or stating resolution as accuracy is disingenuous because accuracy is a function of many different parameters. Accuracy, repeatability, and resolution must be matched to the process requirements. Increasing resolution, repeatability, and accuracy beyond what is required will not increase sample quality. The desired process results should determine the equipment specifications. There are some critical parameters that currently are not specified by some equipment suppliers, such as the geometric relationships and straight line movement variations of each of the axes. To ensure that the desired results are obtained, these parameters must be defined. For some processes, there are no readily available, simple, and easy equipment solutions…yet.

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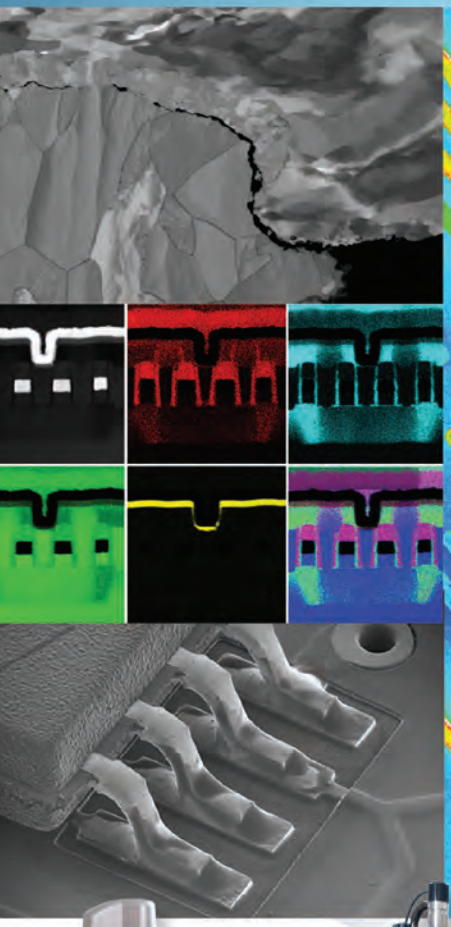
(continued on page 10)

WHEN FA = FAST ANSWERS FOR FAILURE ANALYSIS



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A DISCUSSION OF THE MECHANICAL LIMITATIONS OF MACHINERY *(continued from page 8)*

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Kirk Martin has 40 years of experience in designing and building specialized equipment for all aspects of the semiconductor industry, from crystal growth through final test and failure analysis. In 2005, he became a founder of RKD Engineering, which designs and builds equipment for semiconductor failure analysis and sample preparation. Kirk has patents in the fields of sample preparation, chemical vapor generation, and electrostatic discharge detection and mitigation.

Nancy Weavers has 30 years of experience in applications in the semiconductor and test equipment industries. She started at National Semiconductor in 1982. In 2006, she became the Chief Executive Officer of Left Coast Instruments, a semiconductor test equipment and electron microscope imaging sales and marketing company. She sits on the Board of Advisors for the San Joaquin Delta Electron Microscopy Program. Previously, she was a Vice President at Nisene Technology Group.

NOTEWORTHY NEWS

ANADEF WORKSHOP

The 15th ANADEF Workshop will be held **June 7 to 10, 2016,** at Belambra Business Club, Seignosse-Hossegor (Landes), France. The conference addresses new issues related to the latest technological developments in electronic component failure analysis, presented through tutorials, plenary sessions, micro-workshops, as well as participation by equipment manufacturers and suppliers.

ANADEF, a French nonprofit scientific society established in 2001, meets biennially to bring together industry experts and mechanism scientists concerned with the prevention, detection, and failure analysis of electronic components and assemblies. For more information, visit anadef.org.

NOTEWORTHY NEWS

ESREF 2016

The 27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF '16) will take place **September 19 to 22, 2016**, in Händel-Halle, Halle (Saale), Germany. The conference continues to focus on recent developments and future directions in quality, robustness, and reliability research of materials, components, integrated electronic circuits/systems, and their nano-, micro-, power-, and optoelectronics devices. ESREF provides the leading European forum for developing all aspects of reliability management and failure prevention for present and future electronics. ESREF 2016 will have a specific focus on reliability issues in automotive electronics.

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HOW TO DO FAILURE ANALYSIS FOR STRESS CRACKS

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INTRODUCTION

Failure analysis is all about finding pertinent questions with meaningful answers.

How do you do failure analysis for stress cracks? This is, of course, a dumb question. The obvious simple answer is: you don't. You don't know stress cracks are the cause of a failure before the analysis is done.

The simple answer is correct but not helpful. Dumb questions often point to valid and real questions. In this case, a real question is: "If stress cracks were the cause of a failure, how can that conclusion be discovered and supported?" That is a good question and an important one. Chances are that the correct conclusion will be missed or delayed unless the analyst is familiar with the physics and history of stress voids in integrated circuits (ICs). Without a firm concept of mechanical stress in ICs and IC packaging, many failure mechanisms may not be recognized or appreciated until later ... maybe too much later.

New metallization systems have largely replaced the aluminum and aluminum/silicon conductors that were commonplace in the examples that follow. The stress void mechanism described remains important in today's most advanced metal systems. In fact, stress in metallization may be more critical because of reduced dimensions and multiple metal layers. We're engineering around the problem, but the stress is still there and may be a mechanism that can "bite" us again if we're not vigilant.

BACKGROUND

Stress cracks, or stress voiding, in IC metallization were not a problem until 1980. Electromigration was a major focus. However, metal opens were occurring in high-temperature operating life, after temperature cycle, and after time in room-temperature storage. Opens were found immediately after wafer processing. Clearly, electromigration could not be the cause of failures after unbiased storage.

Stress cracks were found in products from manufacturers worldwide. Attempts to screen out potential failures were not successful. The failure rate due to stress voiding (or "creep") seemed to increase with time. That is, stress voiding was a wearout mechanism that started at time zero.

BASIC CAUSE OF STRESS CRACKS

Aluminum has a coefficient of thermal expansion (CTE) of 26×10^{-6}/°C. The CTEs of SiO_2 and silicon are approximately 0.5×10^{-6}/°C and 3.5×10^{-6}/°C, respectively. Deposited aluminum adheres well to SiO_2. Good adherence to SiO_2 is necessary for IC manufacture, but adherence results in mechanical stress in a deposited aluminum film. Aluminum was deposited at elevated temperatures near 300 °C. When cooled to room temperature, aluminum tended to shrink approximately 50 times more than its SiO_2 substrate. An unavoidable tensile stress is left in the aluminum close to the SiO_2. The oxide stretches the aluminum. The mechanical force tends to pull the aluminum apart. Note that while the aluminum is in tension, the substrate oxide is in compression.

After metal deposition, the metal is patterned and subsequently covered with a passivation layer, with the wafer heated to approximately 400 °C for passivation deposition. As applied, the passivation layer is in compression. Aluminum lines become highly stressed by nitride and oxide that encapsulate and restrict the metal on top, bottom, and both sides. All of this creates more tensile stress in the aluminum.

Although aluminum is a rather soft metal, it is also brittle. Under tensile stress, a brittle material does not stretch and elongate. Deposition variables such as the addition of silicon or nitrogen can make the film more brittle.[1] Stress voiding is made more severe for more brittle metal.

Similarly, passivation films tend to be compressive. Passivation material and deposition details are as important to stress voiding as the metal itself.[2]

OBSERVATION OF ALUMINUM STRESS CRACKS

Very small cracks in aluminum are not detectable by optical or scanning electron microscopy while the passivation is intact. Figures 1 and 2 show typical aluminum lines after passivation removal. Figure 1 is an optical photo showing wedgelike voids at the metal edge. Wedgelike voids do not cause failure, but they are characteristic of stress voiding. Material that was previously in the void has been pulled into the remaining aluminum on either side. Stress in the aluminum is therefore lessened. Figure 2 shows a cracklike void totally across a metal line. Obviously, such cracks cause the line to be electrically open. Cracks may occur most frequently at oxide steps, where stress is enhanced. Cracks may also be where the strength of a line is compromised by a material weakness such as a silicon nodule. Such precipitates effectively reduce the cross section of aluminum, therefore reducing its strength. However, cracks can occur anywhere along a line.[5]

SUMMARY OF STRESS VOID SYMPTOMS

Stress voiding is most prevalent in aluminum lines less than 3 μm wide. Voids may be coincident with silicon nodules or oxide steps. However, voids can occur anywhere without discontinuities that concentrate stress or weaken line strength. Longer lines also tend to be more susceptible to stress voiding, but this is not a necessary condition.

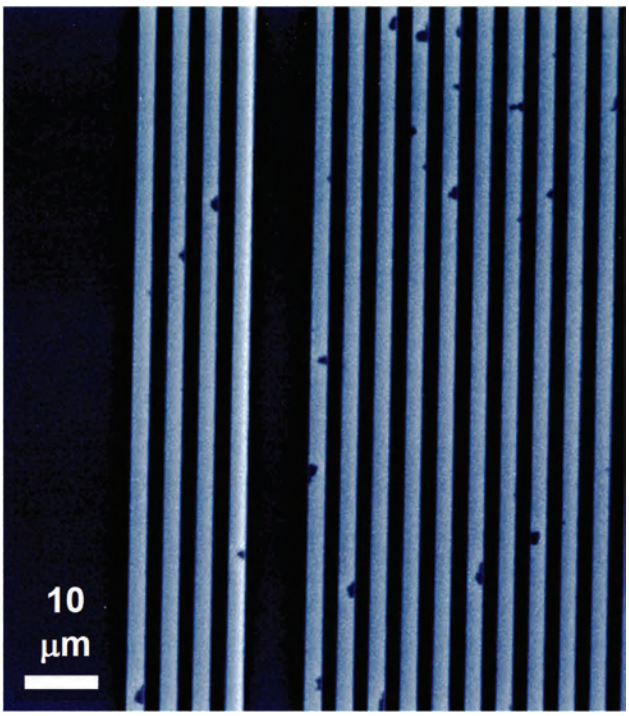

Fig. 1 Wedgelike voids. Source: Ref 3

"SILICON NITRIDE PASSIVATION IS HARDER THAN PHOSPHORUS-DOPED GLASS AND THEREFORE CREATES MORE STRESS IN UNDERLYING ALUMINUM."

Void failures may occur immediately after fabrication and continue to occur with time. Failure rates may increase with moderate temperature increase. However, failure rate decreases for very high temperature, because the driving tensile stress is relieved as metal temperature approaches deposition temperature. Note that this is a countercondition to most other reliability mechanisms where heating is used as an accelerating factor. Failures are also found in high-temperature operating life, but nominal current and voltage conditions are not a factor.

Although aluminum is a soft metal, it is also a brittle metal. Additives to aluminum such as silicon and nitrogen make aluminum films harder and more brittle. Severity of stress voiding is increased for the more brittle, less ductile metal.

Passivation is as important as the metal itself in the stress void mechanism. Greater compressive stress in the passivation increases the severity of stress voiding. Silicon nitride passivation is harder than phosphorus-doped glass and therefore creates more stress in underlying aluminum.

FAILURE ANALYSIS

For the open failures described, defect sites were electrically isolated. Cracks associated with failure became

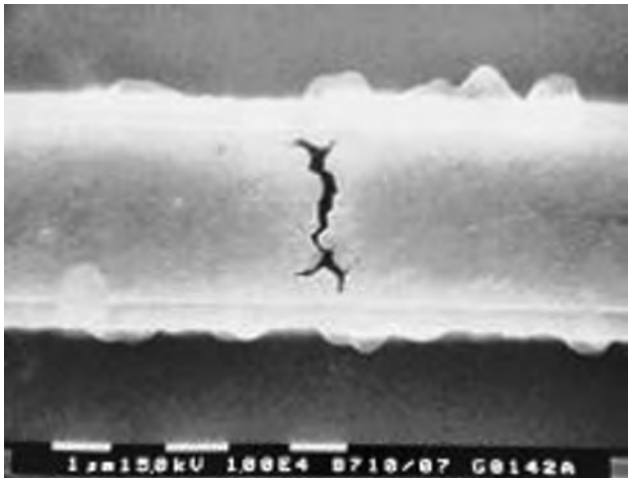

Fig. 2 Cracklike void. Source: Ref 4

visible after passivation removal. Even though the defects were clearly visible, their cause, extent, and implications were unknown. Extensive study over several years was required to understand the physics of stress-induced voiding. Because of quantum mechanical tunneling, lines with stress voiding may operate even at low frequencies. However, the voids become wider very slowly with time and eventually cause low-frequency failure. Heating and cooling can alter the failure signature and make it harder to identify. Removal of the passivation or other encapsulating layers will change stress cracks, usually making them worse. The analyst then must answer the question of whether the identified defects were present before deprocessing or are a result of deprocessing.

Today, it is understood that different CTEs of metal and surrounding oxide produce stress that induces voiding. Stress voids are a fact that must be expected. Barrier metals have been added to provide a redundant path around a void in a long metal strip. A void in a long metal strip no longer causes an electrical failure. Stress void failures are not that easily eliminated. Vias, or connections between layers of conductors, are locations where a stress void can produce an electrical open. For aluminum systems, tungsten plugs can create stress and introduce open possibilities.[6] For copper systems, vias again offer unique possibilities of failure.[7] Redundant vias may be used to avoid IC failure despite possible voiding. However, redundant vias may not always be possible.

In today's ICs, many new diagnostic techniques may be required to electrically define a defect site. If the defect is in the metallization, stress cracks become a consideration. There will not be one dramatic finding that proves stress voiding as the cause. If the defect is a stress void, it will not be the only one; other voids will exist in different or similar places. Metal purity may be an issue. The analyst will be challenged to find and answer good questions that hone in on the cause. When peripheral symptoms are verified and other mechanisms have been eliminated, stress voiding will top the list. It will be up to the analyst or responsible colleagues to finalize the conclusion. The procedure may not be that different from 1980, which may be why failure analysis is still so much fun.

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David Burgess is a failure analyst and reliability engineer. He developed techniques and taught in those areas at Fairchild Semiconductor and Hewlett-Packard. He is the founder of Accelerated Analysis, a manufacturer and distributor of specialty failure analysis tools. David is the co-author of *Wafer Failure Analysis for Yield Enhancement*. A graduate of Rensselaer Polytechnic Institute and San Jose State University, he is a member of EDFAS and has served on various ISTFA committees. David is a Senior Life Member of IEEE and was General Chairman of the 1983 International Reliability Physics Symposium (IRPS).

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SOFT-ERROR SUSCEPTIBILITY OF FinFET SRAMs

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INTRODUCTION

For technology scaling beyond 20 nm, FinFET transistors will replace the conventional planar geometry. The driving force for the introduction of FinFET architecture is the superior immunity to short-channel effects and the reduction of the effects of process variation on device performance exhibited by the FinFET.[1-4] Figure 1 shows a comparison of architectures of the planar FET and the FinFET. One of the major concerns with the introduction of a new transistor architecture is ensuring that the transistor maintains the high level of reliability required for silicon circuits. Fortunately, in terms of reliability, the transition to FinFETs has been smooth; FinFETs do not introduce new reliability issues beyond those with which we are familiar.[4]

One of the most important reliability concerns for silicon circuits is soft errors in SRAM circuits, which involves electrical upsets generated by the interaction of energetic atomic and subatomic particles with the silicon substrate material. SRAMs are particularly sensitive to radiation-induced soft errors due to the relatively low amount of charge at the storage nodes. Errors are generated by the impact of alpha particles emitted from trace amounts of uranium in solder and packaging materials of the circuit, and by neutrons that originate in the cosmic ray shower in the Earth's atmosphere. Alpha particles generate charge in the silicon substrate as they lose energy.[5] Neutrons, because they are electrically neutral, induce errors when they collide with the silicon atoms of the substrate, leading to the generation of charged secondary ions. These ions generate charge as they move through the silicon.[6] There is a second mechanism whereby neutrons induce errors: Cosmic ray neutrons have a wide energy range (unlike alpha particles emitted from package materials), and low-energy (slow) neutrons may be captured by naturally occurring B^{10} atoms close to the surface of the silicon substrate.[7] The decay of the B^{10} resulting from the neutron capture produces an energetic alpha particle together with a lithium ion, both of which can generate charge in the silicon. For the most advanced silicon process technologies, B^{10} is commonly incorporated in the contact regions of transistors due to the use of B_2H_6 as a carrier gas during tungsten contact deposition.[8,9] Soft errors may also be generated by cosmic ray muons, which are actually more abundant in the cosmic background radiation than neutrons. However, the authors' recent work[10] indicates that errors due to muons are negligible compared to alpha particles and neutrons, and so muon-induced errors will not be discussed here.

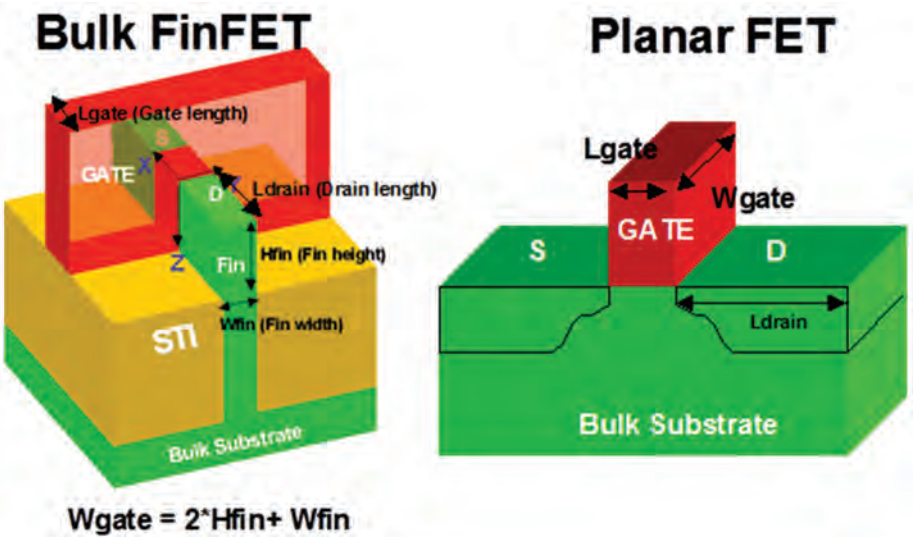


Fig. 1 3-D schematic of a bulk FinFET compared with a planar FET

Soft errors are a dominant reliability concern for advanced silicon process technologies because the associated failure rates are constant with time and therefore can be present over the whole operational life of a circuit. Furthermore, with technology progression, the rate of failure of circuits or systems tends to increase as ever-higher densities of transistors are incorporated to improve performance, cost, and functionality. With the introduction of the FinFET, it is important to understand how soft errors are impacted and what, if any, new soft-error-rate (SER) issues may be introduced by this change. This article reviews recent work aimed at characterizing soft-error effects in SRAM circuits fabricated with bulk silicon FinFET transistors. Experimentally determined error rates are combined with technology computer-aided design (TCAD) simulations to provide a clear understanding of the charge generation and collection processes that occur in both planar and FinFET transistors. As shown, the introduction of the FinFET leads to a significant improvement in SERs because of a large reduction in charge collection resulting from the more limited geometry of the fin compared to the planar structure.

EXPERIMENTAL DETAILS

All accelerated tests were conducted following the JEDEC JESD89 testing standard.[11] SRAM circuits with a range of manufacturing processes and bit-cell sizes were tested. The SRAM devices used the standard 6-transistor (6T) cell design, as shown in Fig. 2. High-energy neutron characterization of 6T-SRAMs was carried out using neutrons with an atmospheric-like energy spectrum, where the energy range is up to 150 MeV.[12] Neutrons were incident normal to the surface of the SRAMs. The fluence (neutron beam flux × exposure time) of each test run was ~1 × 10^9 neutrons/cm^2. Thermal neutron SER tests were conducted at the Laboratoire Léon Brillouin facility in France using a low-energy neutron source with a 25-meV-equivalent neutron spectrum.[13] Alpha SER tests were performed using an Am-241 irradiation source placed on the packaging-decapped SRAM chip. The gap between the irradiation source and the tested chip surface was ~1 mm in all cases. Tests were performed dynamically with a clock cycle of 100 ns. Tests were performed at room temperature using a checkerboard all-0 or all-1 test pattern. Experimental data are presented as the average of all test patterns. Neutron errors were normalized to the neutron flux at the sea level of New York City, that is, 13 counts/cm^2/h for high-energy neutrons and 6.5 counts/cm^2/h for thermal neutrons. Alpha particle errors were normalized to an emission rate of 0.001 count/cm^2/h.

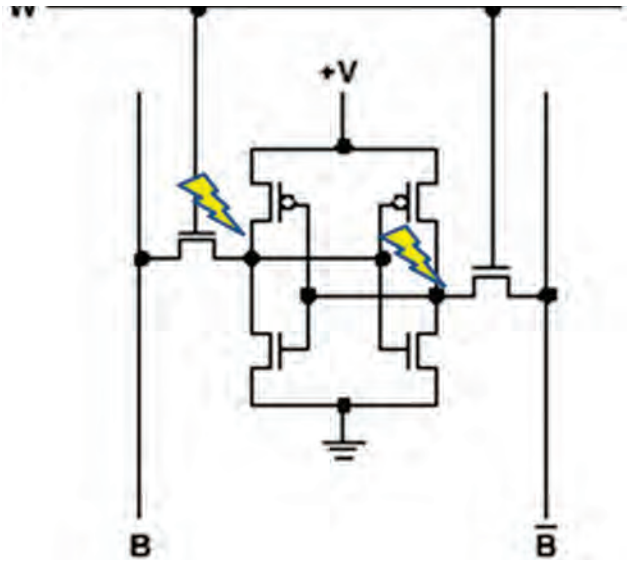


Fig. 2 6T-SRAM cell

SINGLE-BIT ERRORS IN SRAM CIRCUITS

Figure 3 shows the experimentally determined trend of single-bit upsets (SBUs) for SRAM circuits as a function

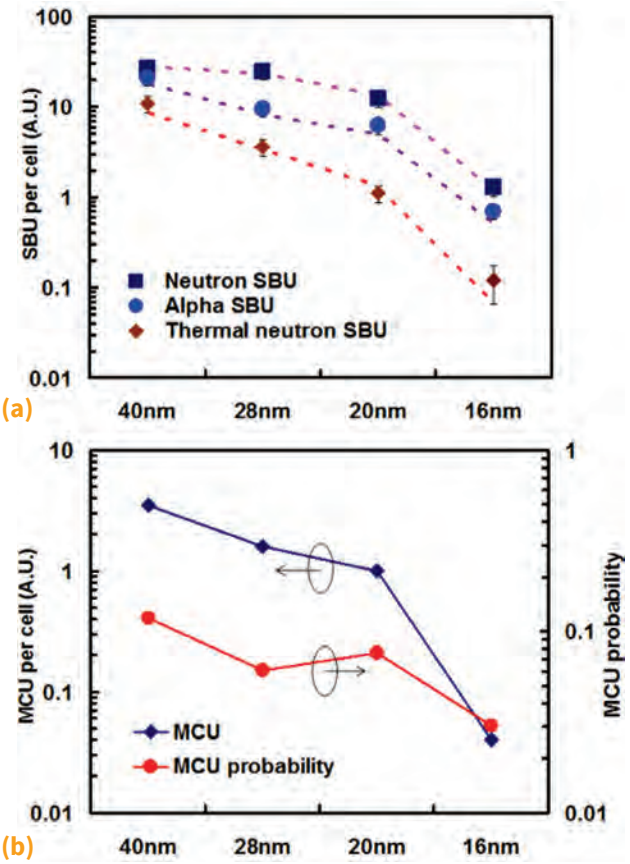


Fig. 3 (a) Measured alpha, thermal neutron, and high-energy neutron SBU events for 40, 28, and 20 nm planar SRAMs as well as a 16 nm FinFET SRAM with nominal voltage. Dashed lines are modeled results using Eq 1 for all irradiation sources. (b) High-energy-neutron-induced multicell upset (MCU) events and MCU probability of SRAMs (MCU per total upsets) as a function of technology

of technology progression for recent silicon technology nodes. Note that the FinFET transistor was introduced at the 16 nm node. The error rate has trended down over this technology range for all the upset mechanisms. However, the introduction of the FinFET has led to a large decrease in the magnitude of errors (approximately a factor of 10) compared to what would be expected from an extrapolation of the data for planar transistors.

The magnitude of errors for planar transistors is readily calculated using the following expression:

$$S = FA_s \exp(-Q_{coll}/Q_{crit}) \quad \text{(Eq 1)}$$

where F is the flux of particles incident on the silicon surface, and A_s is the sensitive area for charge collection. The relation indicates that S decreases with lowering Q_{coll} when Q_{crit} of the device is constant. The exponential function $\exp(-Q_{coll}/Q_{crit})$ is the probability of an error occurring, which depends on the nature of energetic particle involved. The downward trend of S occurs because the sensitive area, A_s, has decreased faster than the decrease in the critical charge with technology scaling. Shown in Fig. 3 are relative failure rates calculated using Eq 1. The large reduction of S with the introduction of the FinFET is beyond what is expected on the basis of changes in A_s alone and implies that the probability of an error is reduced. This must involve modification of the collected charge with the FinFET geometry.

Charge collection resulting from the impact of an energetic particle with the silicon substrate occurs by two mechanisms:

- Charge drift in the drain region when the ion track crosses the drain directly
- Charge diffusion via the *p-n* junction to the drain region when the ion track does not cross the drain

In planar devices, charges associated with the ion tracks penetrating the silicon substrate are deposited in the drain directly and also under the drain region, which then diffuse to the drain. While the fin body of the bulk FinFET is connected to the substrate, the volume of silicon

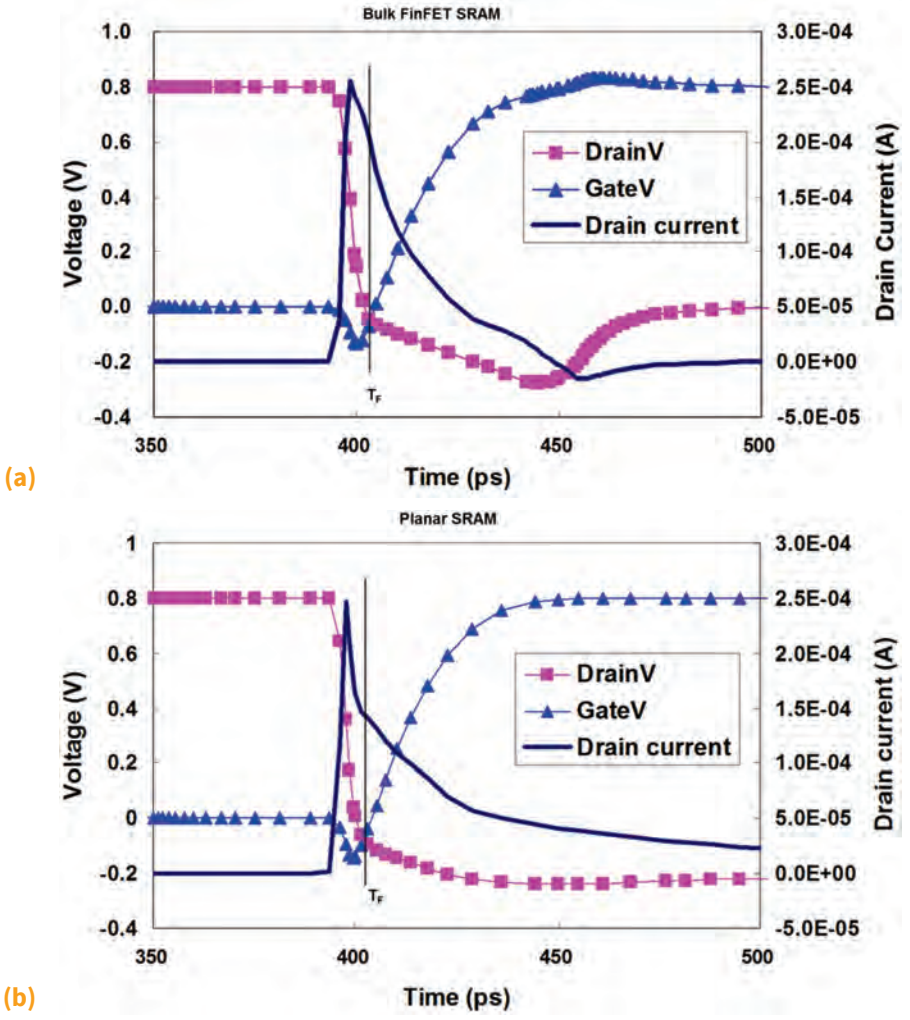


Fig. 4 Gate voltage and drain voltage change as well as drain current variation when a heavy ion crosses the drain horizontally in (a) bulk FinFET SRAM and (b) planar SRAM. Data-flipping time, T_F, is the time where the increasing gate voltage crosses the falling drain voltage.

available for charge collection is smaller than that for planar devices, so a smaller amount of deposited charges can be expected to diffuse to the FinFET drain. Simulations of the transistor response to energetic ion strikes were performed using the Synopsys Sentaurus 3-D tool. Details of the simulation procedure are described in Ref 14.

Two ion-strike conditions are considered in these simulations. The first involves ion strikes to the drain where the ion track either crosses the drain along its length in the center of the drain body or occurs at normal incidence from the top and vertically crosses the drain. In the second condition, the ion strikes the bulk substrate at a distance approximately 0.5 µm under the drain, and the ion track does not cross the drain. The collected charge, Q_{coll}, of the drain node of the *n*-FET is then calculated by integrating the transient current over this time interval. An upset of the data stored in the SRAM cell occurs when the Q_{coll} is collected over a threshold value, Q_{crit}, which results in a flip of the stored data. Figure 4 shows the drain voltage as a function of time for both bulk FinFET and planar SRAMs when the ion track crosses the drain along its length at a time of 400 ps in the simulation. In this instance, an incident ion linear energy transfer (LET) = 30 MeV-cm^2/mg is chosen. In both cases, the drain voltage falls after the ion strikes, while the voltage of the gate increases. Q_{crit} is obtained by integrating the drain transient current that results from a collision of an energetic particle with the silicon substrate over the time at which the falling drain voltage crosses the increasing gate voltage. The simulated Q_{crit} of the FinFET SRAM is 1.53 fC, and that of the planar SRAM is 1.46 fC. The similarity of the Q_{crit} values of FinFET and planar SRAMs is reasonable because the effective W_{gate}, L_{gate}, and T_{ox}, as well as the operation voltage, are identical.

Figure 5(a) shows the comparison of the drain current transients arising from a horizontal ion strike through the *n*-FET drain with an LET of 30 MeV for the bulk FinFET and planar SRAMs. The time-dependent drain current pulses of

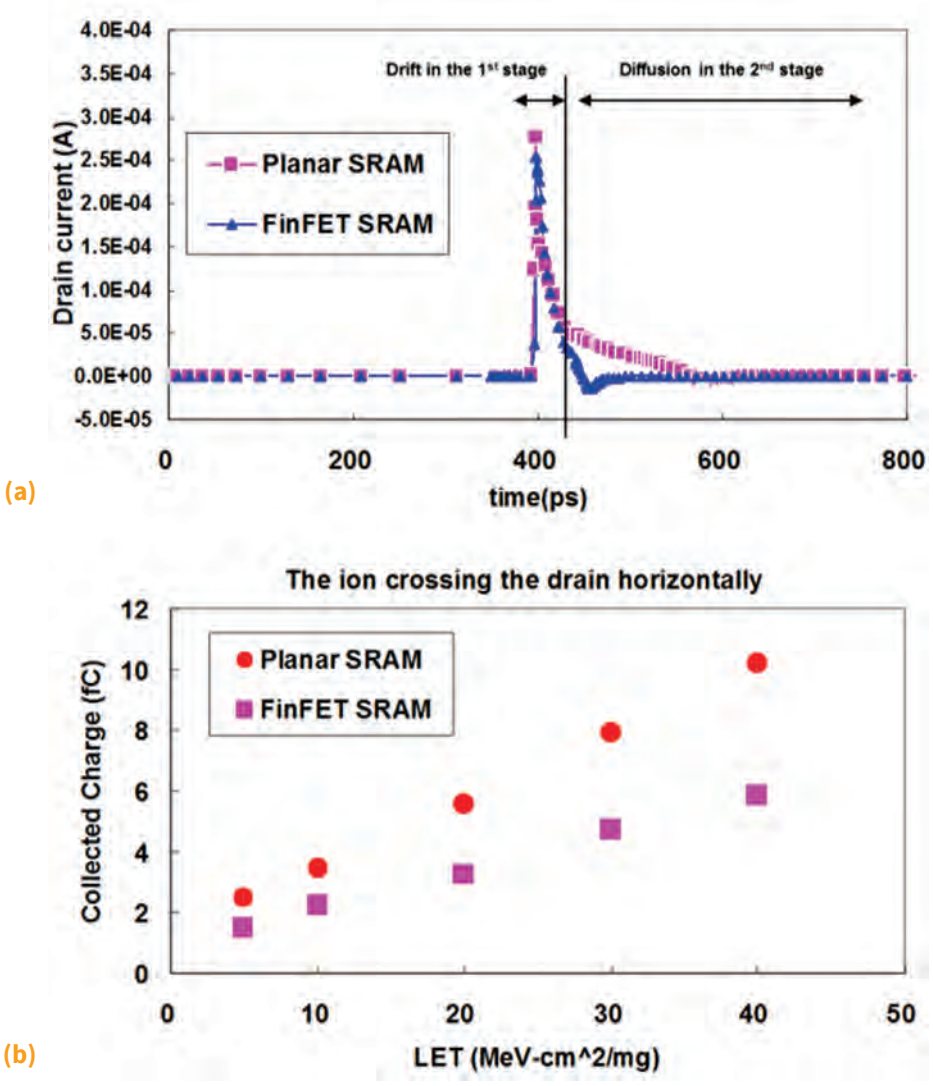


Fig. 5 **(a) Comparison for drain current transients of planar and FinFET SRAMs when an ion of 30 MeV-cm^2/mg strikes horizontally through the drain. (b) Q_{coll} of planar and FinFET SRAMs from the horizontal track crossing the drain with different LETs**

both devices are consistent in the first stage of charge collection, which is dominated by drift. In the second stage, the drain current of the planar SRAM is higher than that of the FinFET SRAM. This is because of additional charge diffusion from the substrate. In contrast, the charge in the FinFET SRAM is collected almost entirely by drift because the ion track only crosses the drain of the fin body. For the planar SRAM, the ion track crosses not only the planar drain but also the substrate. The Q_{coll} is obtained by integrating the current up to 1000 ps, which is 4.71 fC for the FinFET SRAM and 7.92 fC for the planar SRAM. The comparison of Q_{coll} of the FinFET and planar SRAMs with ion strikes with different LETs is shown in Fig. 5(b). On average, when the ion track crosses the drain horizontally along the drain body, Q_{coll} of the FinFET SRAM is ~0.6× smaller than that of the planar SRAM up to an LET of 15 MeV, which is the range of charge deposition of terrestrial neutron-induced ions in silicon.[10] Figure 6 compares the FinFET Q_{coll} and planar SRAMs when the incident ion track crosses the drain vertically from the top. In this case, Q_{coll} of both FinFET and planar SRAMs increases compared to the ion crossing horizontally, because charge diffusion from the substrate increases when the ion track is at normal incidence to both the drain and the substrate under the drain. The averaged Q_{coll} of the FinFET SRAM for LETs up to 15 MeV is close to a factor of 0.6 that of planar SRAM in the normal incidence case.

When the ion track does not cross the drain, deposited charges are collected by diffusion only. The planar SRAM is sensitive to the diffused charges generated by the ion penetrating under the drain because there is a wide sensitive volume of charge collection. Figure 7(a) shows the variation of the drain voltage of the planar SRAM with different LETs. The drain voltage drops with time when the LET of the ion is over 5 MeV. In the bulk FinFET, only the fin body is connected with the substrate. For the same ion strike, the ion must deposit more charge in the substrate to cause the bulk FinFET SRAM to flip compared with the planar SRAM. The increasing LET required to cause a bit flip is shown in Fig. 7(b). The drain voltage of the bulk FinFET SRAM does not flip until the LET is 60 MeV. In the terrestrial environment, the maximum energy of incident neutrons is limited to 1 GeV.[15] The maximum energy deposition (or LET) of a neutron-induced ion in silicon is 15 MeV. Therefore, the planar SRAM flips easily in the 15 MeV range of LET. The bulk FinFET SRAM is immune to an upset in this energy range. That is, Q_{coll} of terrestrial neutron-induced energetic ions from the silicon substrate is ineffective in causing a change in the data stored in the SRAM bit cell.

It has been shown that the maximum probability of neutron-induced ions crossing the drain is 0.25 (i.e., the probability of ions not crossing the drain is 0.75) for a fixed-drain area of a planar device.[15] In the situation studied here, where the overall geometries of the FinFET and the planar SRAMs are the same, when the ion crosses the drain, Q_{coll} of the bulk FinFET SRAM is only 0.6 that of the planar SRAM. Without the ion crossing the drain, the FinFET SRAM is immune to upsets in the terrestrial environment. Therefore, for a wide range of incident ions, Q_{coll} of a FinFET SRAM should be 0.6 × 0.25 = 0.15 compared with a planar SRAM. Using the Q_{crit} determined in the previous section and the top drain area of the FinFET of 0.4 that of the planar device, the relative SER of the bulk FinFET SRAM is estimated to be ~0.06 compared with the planar SRAM; that is, it is anticipated that FinFETs will

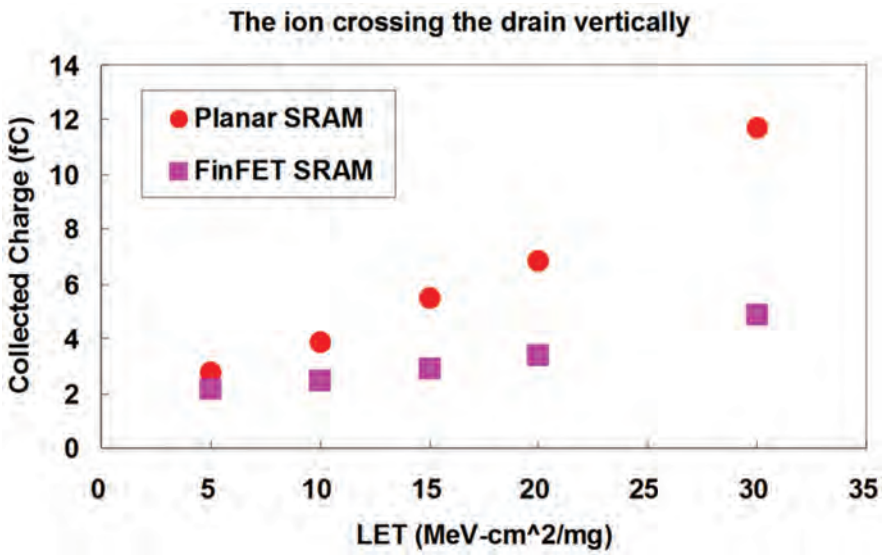


Fig. 6 Q_{coll} **of planar and FinFET SRAMs from the normal incident track crossing the drain with different LETs**

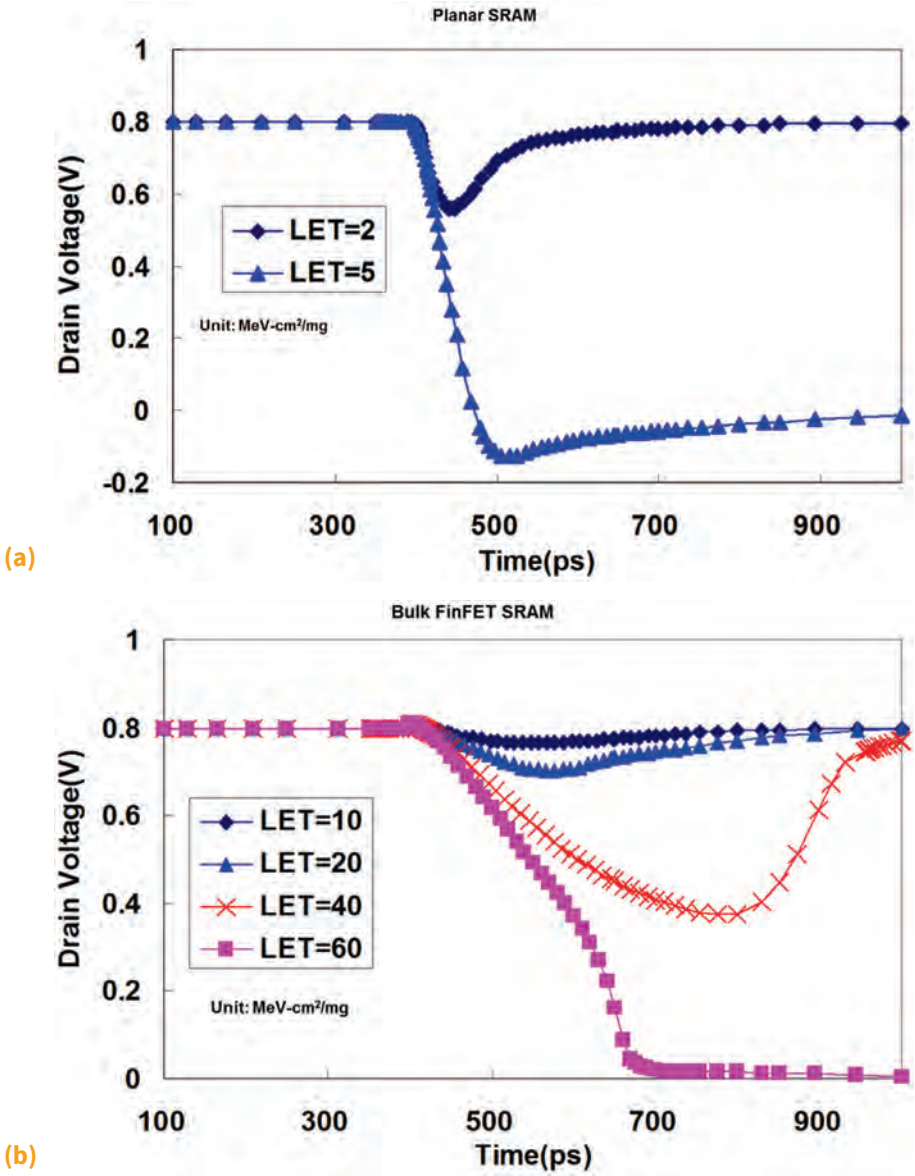


Fig. 7 Drain voltage variation with different LETs for (a) planar and (b) bulk FinFET SRAMs when the ion track does not cross the drain

exhibit approximately an order of magnitude decrease in soft errors compared to planar transistors at the same technology node. This is consistent with the experimentally observed decrease in soft error in Fig. 3.

MULTICELL ERRORS

Thus far, only single-bit errors have been considered for all particle sources. In reality, for high-energy neutrons in particular, the range of errors introduced is larger than this, and it is common to observe multiple bits (multicell upsets, or MCUs) being simultaneously upset by a fast neutron strike. Figure 8 shows examples of the MCU bit map in a SRAM array. As Fig. 3(b) shows, the magnitude of MCU events has decreased in tandem with SBU events as silicon technology has progressed, with FinFETs showing a similarly large reduction compared to planar devices

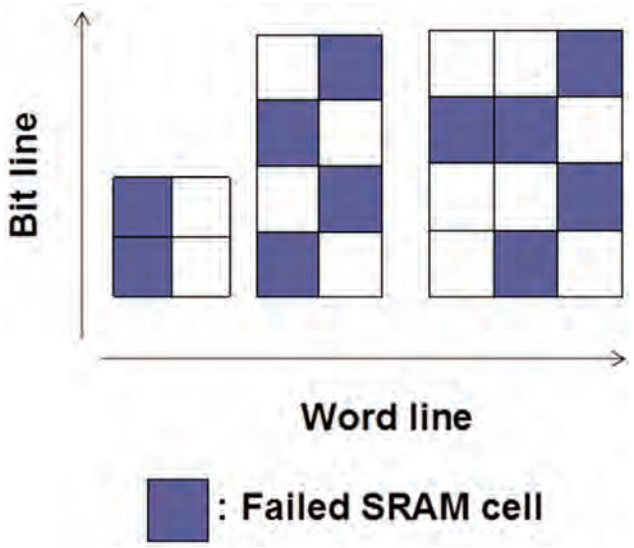


Fig. 8 Examples for MCU bit maps in a memory array

for both types of error. However, the probability of MCU events shows a dependence on the technology node, implying a dependence on the details of the processing sequence because the SRAM design is similar in all cases. While single-bit errors are readily corrected at the system/circuit level using a variety of techniques that are commonly known as error-correction codes, these techniques cannot be used to correct MCU events, and so the latter tend to dominate the soft-error reliability of SRAMs.

The MCU events are caused by two mechanisms, leaving aside the possibility of multicell errors caused by a single direct ion strike. First is bipolar amplification of charge collection caused by the turn-on of the parasitic bipolar transistor formed by the source/bulk/drain of the MOSFET. Positive charge accumulation in the silicon tub region of the transistor is responsible for the turn-on of the parasitic bipolar transistor. A second mechanism that

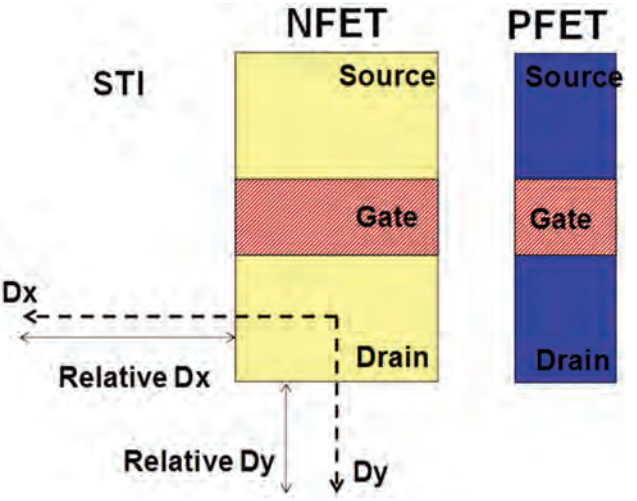
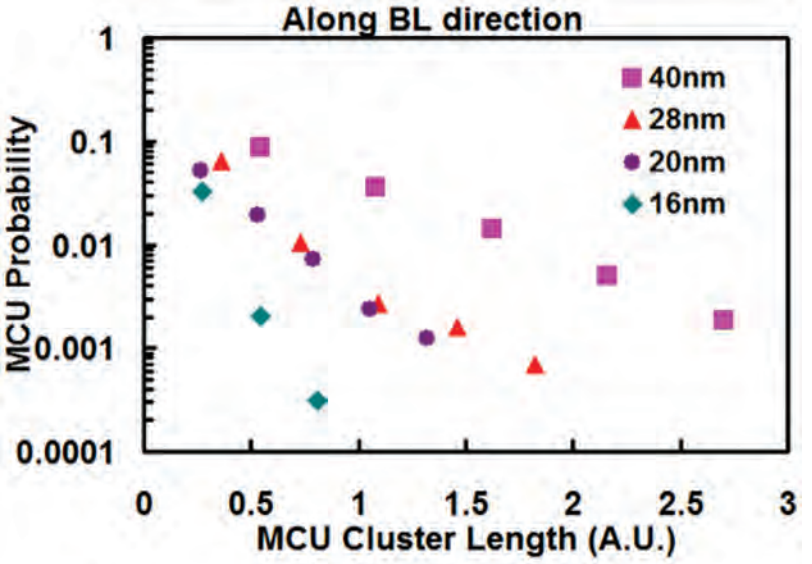
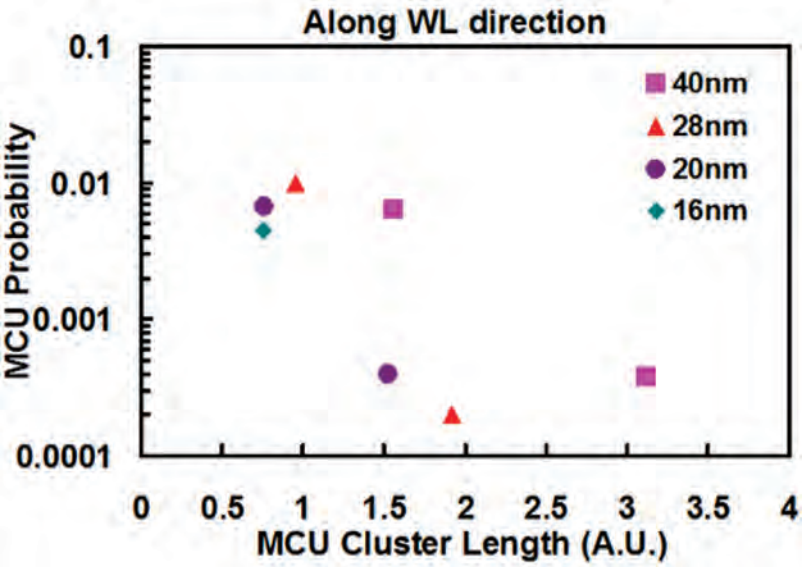


Fig. 9 Schematic 2-D top view for the inverter structure in a SRAM. The ion is normally incident to the silicon surface with a relative distance D_x (or D_y) away from the edge of the drain.



(a)



(b)

Fig. 10 Measured neutron-induced MCU cluster length distributions along the (a) *BL* direction and (b) *WL* direction for 40, 28, and 20 nm planar SRAMs and a 16 nm FinFET SRAM. The unit of the MCU cluster length has been scaled by a constant.

causes error is charge sharing, which results from diffusion of charge to cells that are adjacent to the cell directly involved in the particle strike. The authors recently have shown that the primary mechanism responsible for MCU events in both planar transistors and FinFETs is charge sharing, so bipolar amplification is not considered further in this discussion. A charge-sharing mechanism is primarily characterized by a decrease in the probability of MCU events with increasing physical distance over which the MCU event occurs.

To understand the origin of MCU events in SRAM devices, the authors performed charge-collection simulations using Synopsys' Sentaurus TCAD. Details are given in Ref 16. A heavy ion with LET of 150 fC/μm was normally incident at different locations in the vicinity of the *n*-FET drain, as shown in Fig. 9. The strike location $D_x = 0$ indicates the heavy ion is normally incident to the *n*-FET drain region, whereas the relative $D_x > 0$ means the ion is normally incident to the silicon surface with a relative distance away from the edge of the *n*-FET drain along the D_x direction. The distance unit of all devices is the same as the unit of MCU cluster length shown in Fig. 10.

Figure 11 shows the transient currents of the 40 nm planar *n*-FET and the 16 nm *n*-FinFET as a function of the strike location. The current consists of an initial spike due to the drift component, followed by a tail at larger times from the diffusion component. The drift current is collected when the ion penetrates through the drain depletion layer, whereas the diffusion current is collected from the substrate via the drain *p*-*n* junction. When the strike occurs outside the drain, the drift component disappears, leaving only the diffusion current. The drift currents of the

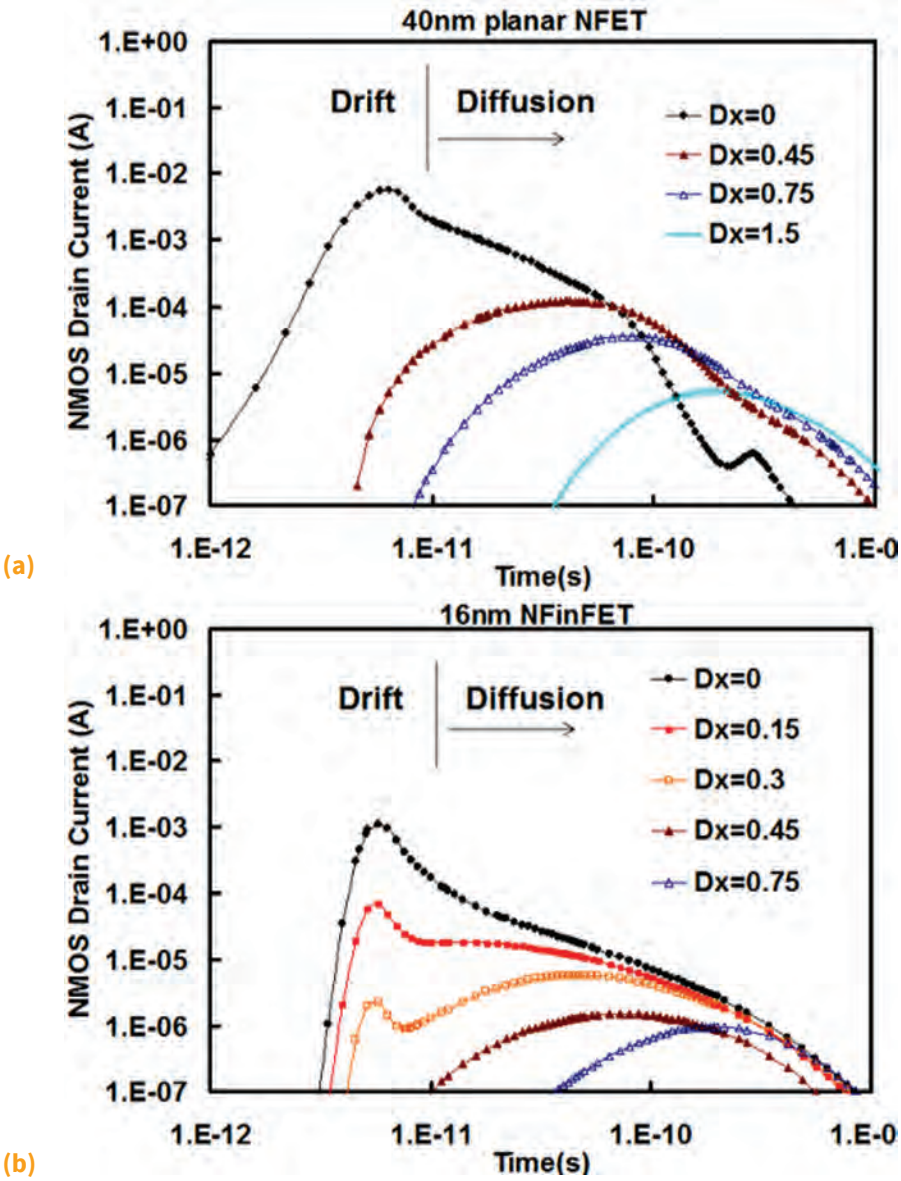


Fig. 11 Drain transient currents of (a) 40 nm planar *n*-FET and (b) 16 nm *n*-FinFET with different strike locations. The ion strike with an LET of 150 fC/μm starts at 4×10^{-12} s.

planar SRAM are higher than those in the FinFET SRAM, as expected because Q_{coll} is suppressed by the geometry of the FinFET.[14] Figure 12 shows Q_{coll} as a function of the relative distance of the strike locations along the D_x direction. Q_{coll} as a function of distance decreases in a similar manner as the measured MCU probability distributions as a function of the MCU cluster length, as expected for a charge-sharing mechanism. Moreover, it is clear that Q_{coll} is a function of the technology node for any given cluster length, implying that the differences observed in MCU probabilities at any given distance are in fact related to variations in Q_{coll} between technologies.

For a charge-sharing mechanism of upset, the absolute rates of SBU and MCU are highly correlated, and so it is assumed that the MCU probability is determined only by the Q_{coll} associated with the particular cluster length. The relative MCU probability that may be anticipated from charge sharing at a distance D_x from the drain can be approximated as:

$$P_{MCU}(Q_{crit}, Q_{coll}, D_x) = \exp\left(-\frac{Q_{crit}}{Q_{coll}(D_x)}\right) \approx 1 - \frac{Q_{crit}}{Q_{coll}(D_x)} \quad \text{(Eq 2)}$$

and the number of MCU events is $N_{MCU} = N_{SBU} \cdot P_{MCU}$. Relative

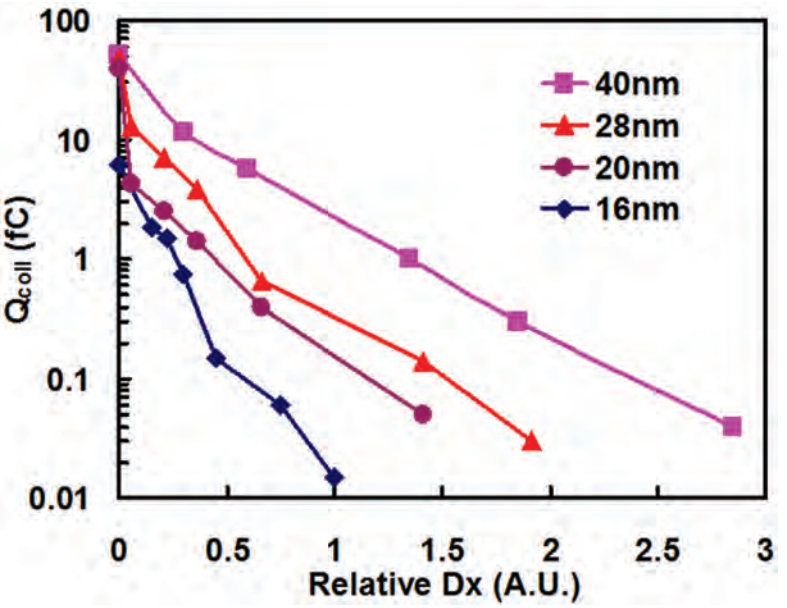


Fig. 12 Q_{coll} **as a function of** D_x

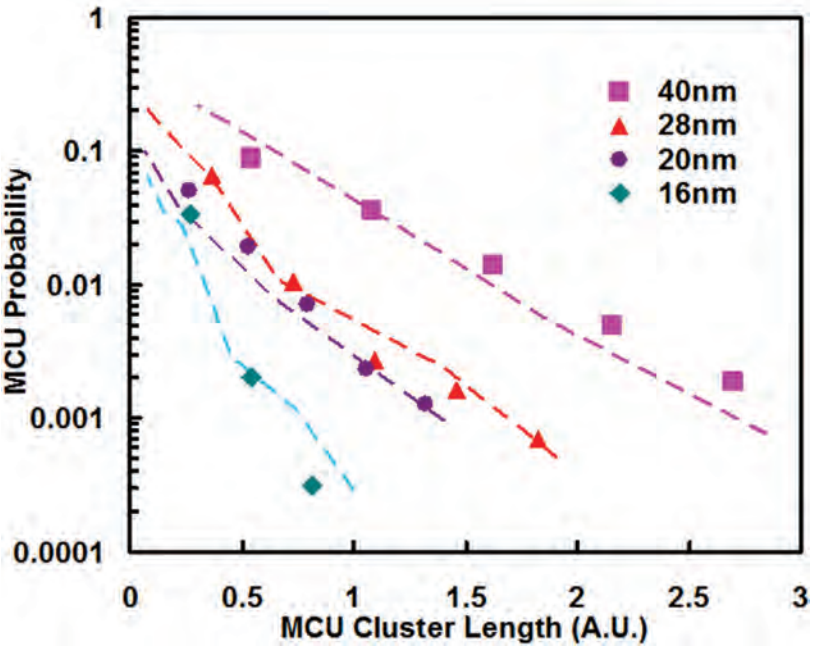


Fig. 13 Modeled MCU probabilities (dashed lines) of SRAMs normalized to Q_{coll} **of 40 nm at** D_x **= 0 compared to experimental data (symbols), which is the average of all test patterns, along the** *BL* **direction**

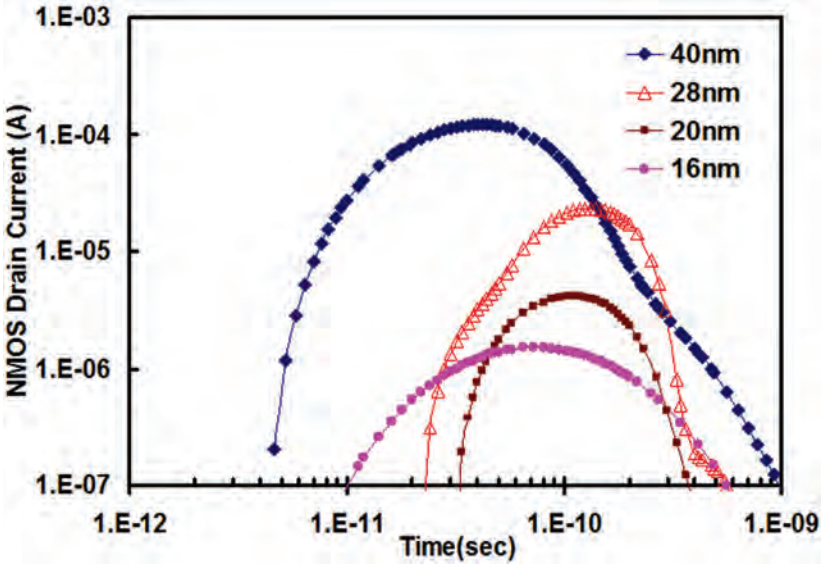


Fig. 14 **Comparison for drain transient currents of 40, 28, and 20 nm planar *n*-FETs as well as a 16 nm *n*-FinFET with an identical relative D_x of 0.45**

MCU probabilities between technology nodes were obtained by assuming all ion strikes incident to the region of the 40 nm *n*-FET drain result in a data error; that is, the probability of upsets at $D_x = 0$ of the 40 nm SRAM is 1. Then all $Q_{coll}(D_x)$ are normalized to $Q_{coll}(0)$ of the 40 nm to give the probability P_{MCU} (Q_{crit}, $Q_{coll,}$ D_x). Figure 13 shows that the calculated relative upset probability compares well to that determined from the measured MCU cluster distributions. It can be clearly observed in Fig. 13 that MCU probability at a given cluster length decreases with technology scaling, as is evident by the increasingly negative slope of the MCU cluster length distribution; this implies that factors in addition to the geometry of the bit cell impact MCU probability. Figure 14 compares simulated transient currents with the identical relative strike location ($D_x = 0.45$) for all devices. For $D_x = 0.45$, all deposited charge is collected by diffusion only. With the identical relative D_x, the diffused current peak decreases with scaling. The authors suggest this suppression occurs due to the reduction of charge mobility caused by increasing doping levels of the substrate beneath the transistor, because this is the primary region where diffusion of the charge occurs.[17,18]

The transport of charge in semiconductors is dominated by scattering by the ionized impurities in doped silicon. In TCAD simulations, the charge mobility dependence on substrate doping is accounted for by using the Masetti model,[19] which models charge mobility in arsenic-, phosphorus-, and boron-doped silicon over a wide range of carrier concentrations (10^{13} to 10^{21} cm^{-3}). Higher doping concentration in the silicon leads to lower charge mobility due to ionized impurity scattering. To determine the substrate doping impact on Q_{coll}, the authors re-ran the TCAD simulations but intentionally turned off the doping-dependent mobility degradation model. Figure 15 shows the comparison for transient diffusion currents only of the 20 nm planar FET and the 16 nm FinFET with

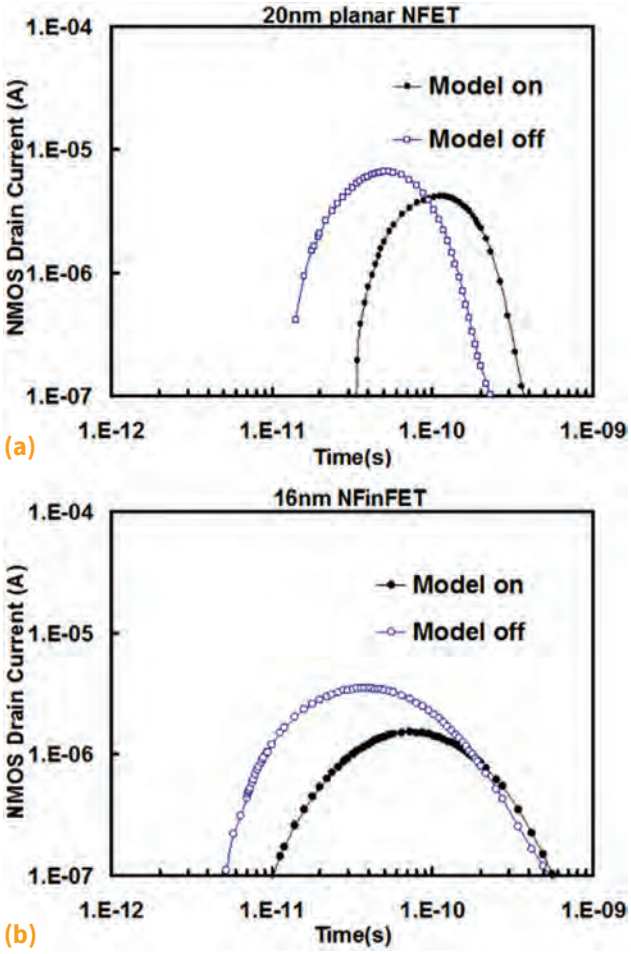


Fig. 15 **Comparison for transient currents of (a) 20 nm *n*-FET and (b) 16 nm *n*-FinFET with strike locations at the relative D_x = 0.45 before and after turning off the doping-dependent charge mobility model**

the identical D_x before and after turning off the doping-dependent mobility degradation. The diffusion current peaks of both devices shift to shorter times, and the peak heights of both increase. Moreover, the current peak height of the 16 nm device increases greater than that of the 20 nm device, suggesting the mobility degradation is larger for the 16 nm device. Figure 16 compares Q_{coll} as a function of the relative D_x before and after turning off the mobility degradation for each SRAM device. The Q_{coll} with D_x ~ 0 (including drift and diffusion currents) does not change after turning off the model, because charge mobility is dominated by the high electric field in the drain region. The Q_{coll} with larger D_x (diffusion current only) for all nodes increases after turning off the mobility degradation. Clearly, doping profiles significantly impact the diffusion component, having an increasingly large role in decreasing charge collection with scaling. Finally, after normalizing for the changes in the drain area, as shown in Fig. 17, it is found that the distributions of cluster length of all nodes are similar.

SUMMARY AND CONCLUSIONS

The introduction of the FinFET transistor architecture has resulted in a significant reduction in the rate of radiation-induced soft errors in SRAMs for all known particle-strike mechanisms. Both single-bit and multicell

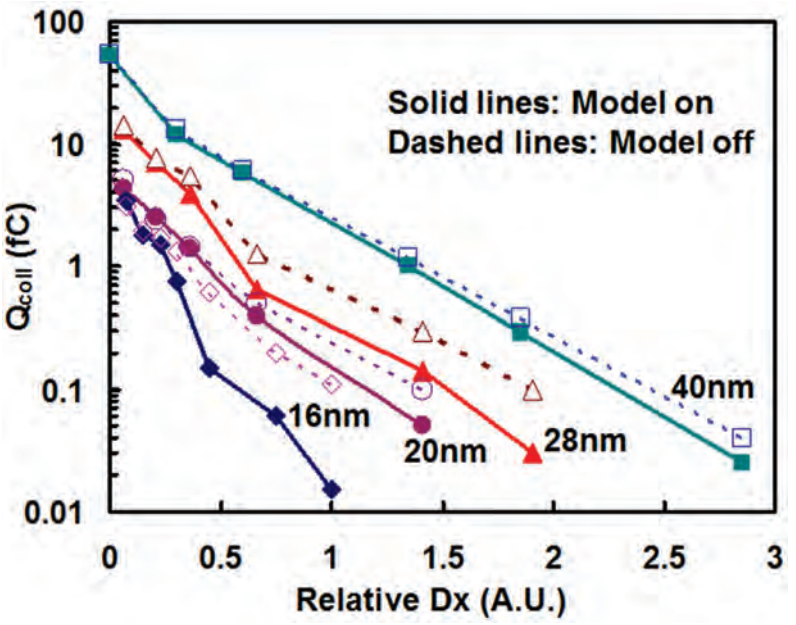


Fig. 16 Comparison for $Q_{coll}(D_x)$ before and after turning off the doping-dependent charge mobility model

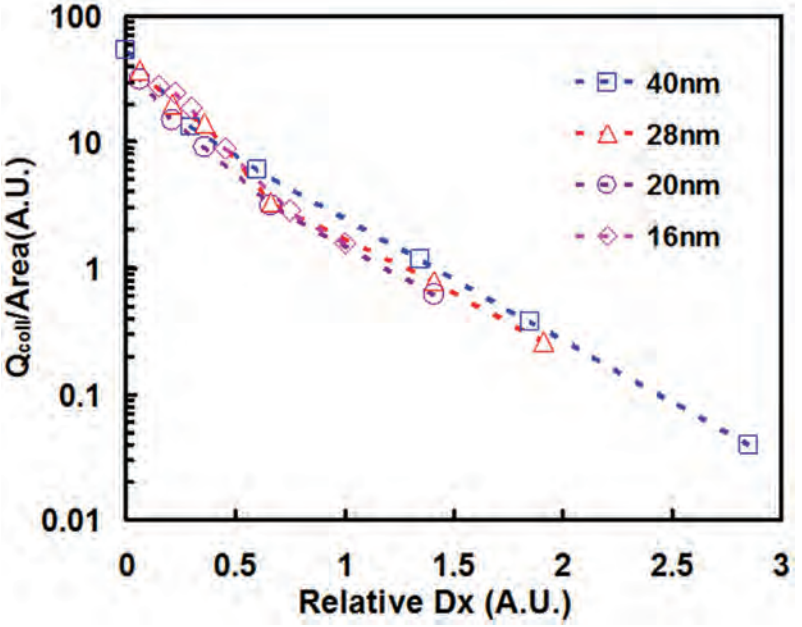


Fig. 17 $Q_{coll}(D_x)$ distributions with the model off normalized for identical drain area

failure mechanisms exhibit improved SERs with similar magnitudes. The authors have shown that these reduced error rates result from a reduction in charge collection due to the limited silicon geometry of the fin structure. Multicell errors are determined by charge sharing between physically adjacent SRAM bit cells. Importantly, it was found that MCU probabilities at a given cluster length of bit cells decrease significantly with technology progression, and this is also primarily a result of the decrease in charge collection inherent in the FinFET.

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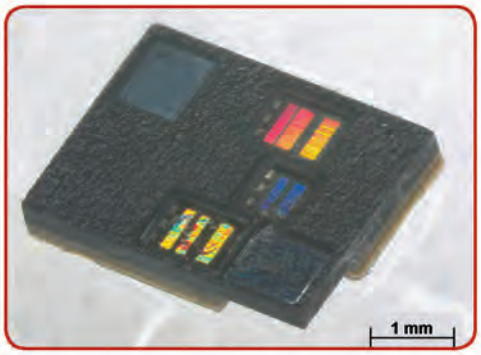
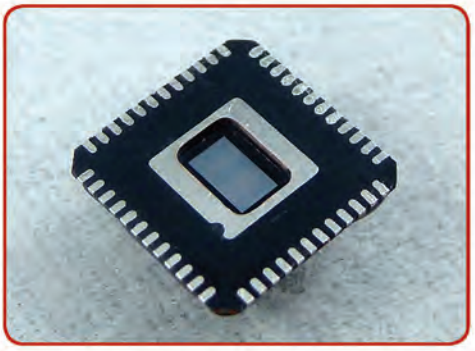
ABOUT THE AUTHORS

Anthony S. Oates received a Ph.D. degree in physics from the University of Reading, Reading, U.K., in 1985. He was then with AT&T Bell Laboratories, where his research centered on studies of failure mechanisms in CMOS technologies. During this time, he was appointed as a Distinguished Member of the Technical Staff, and he assumed responsibility for reliability physics development and CMOS technology process qualification. Since 2002, Dr. Oates has been with Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan, where he is responsible for technology reliability physics research and holds the position of Fellow of the TSMC academy. He has published more than 100 papers in the field of microelectronics reliability, and he is the co-holder of seven patents. Dr. Oates is a Fellow of the IEEE. He is currently the Editor-in-Chief for *IEEE Transactions of Device and Materials Reliability*. He served as the General Chair of the International Reliability Physics Symposium in 2001 and was the chair of the IEEE Electron Devices Society Device Reliability Advisory Committee from 2006 to 2011.

Yi-Pin Fang received M.S. and Ph.D. degrees in physics from National Tsing Hua University, Hsinchu, Taiwan, in 2000 and 2005, respectively. In 2005, he joined TSMC Hsinchu as a principal engineer; he is currently a technical manager in the Technology Reliability Physics Department. Dr. Fang is responsible for the analyses of soft-error-rate reliability issues. His research interests include cell-level soft-error-rate model setup and TCAD simulations of ion-induced charge collection on devices.

Small Device Preparation

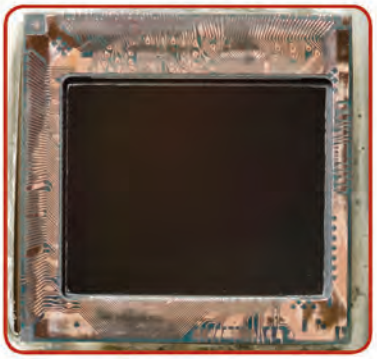




- Open areas as small as 100 x 100 µm

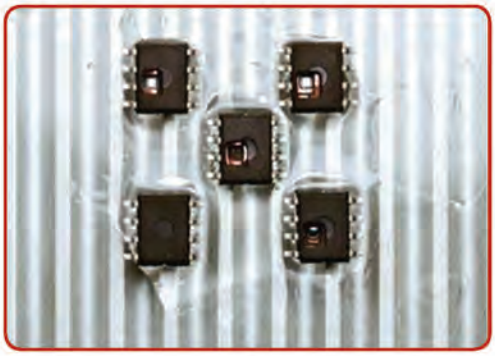
Complex Device & Stacked Die Deprocessing

- TSV exposure



- Targeted stacked die exposure

HD Camera System



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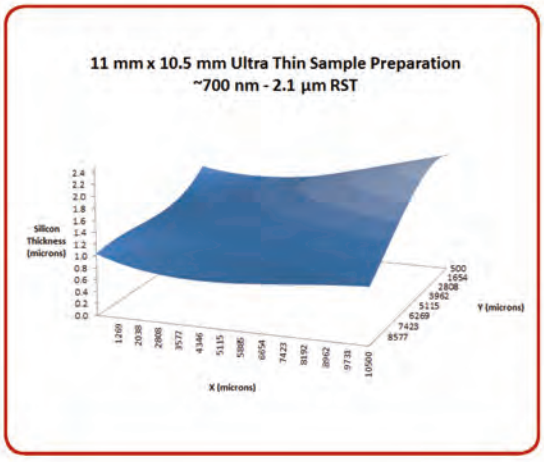

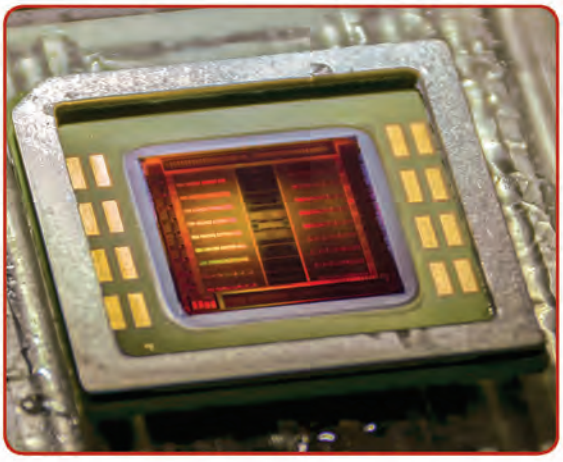

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BOARD CANDIDATE PROFILES

PROFILES OF CANDIDATES FOR THE EDFAS BOARD OF DIRECTORS

Jeremy Walraven, Chair, EDFAS Nominating Committee
jawalra@sandia.gov

The EDFAS Board of Directors (BOD) elections for 2016 are coming up this summer. Nominations closed on March 4, and we have five excellent candidates for the two open positions for the 2016-2020 term. Four new candidates accepted nominations, and one incumbent accepted a nomination for re-election. Each candidate's photo, biographical statement, and vision for EDFAS are provided below. The candidates for the 2016-2020 term are:

- Nicholas Antoniou (incumbent)
- Becky Holdford
- Peter Jacob
- Ted Lundquist
- Ryan Ross

As stated in the EDFAS Charter and BOD Operating Procedures, the election will take place in June 2016 and will be conducted by electronic balloting. New BOD members will assume their duties on September 1, 2016, and serve through August 31, 2020. This is one of your opportunities to influence the direction of EDFAS, so please take this opportunity to vote and be an active participant in EDFAS.

Nicholas Antoniou (incumbent) received his B.S. and M.S. degrees in electrical engineering from Texas A&M University. He spent his early career in the design, test, debug, and manufacture of microprocessors at Motorola and Ross Technology. Nicholas joined FEI Company as FIB Product Manager and later was Director of Marketing. In 2009, he was Principal FIB Engineer at the Center for Nanoscale Systems at Harvard University. In 2014, he became Product Manager at ReVera (maker of metrology equipment for semiconductor manufacturing). He owns a private concern that develops intellectual property, with one patent issued and more pending. He was published in *Science* in April 2013 and has contributed to *EDFA* magazine and the *Microelectronics Failure Analysis Desk Reference,* 5th edition.

Nicholas has held various positions on the ISTFA Organizing Committee, including General Chair (2009). In addition to ASM International and EDFAS, he is an active member of the Microscopy Society of America and IEEE.

VISION STATEMENT

"As a Board member of EDFAS for the last four years, I appreciate the challenges we face and better understand how to address them. I wish to serve this Society for another term so I can focus on ensuring the Society continues to be of great value to its members. I share the current Board's emphasis on education and believe we can improve in this area, but I also want to provide insight into the direction and composition of the electronic device FA market.

Our industry is maturing and, as a result, there is a lot of consolidation. A related trend is to outsource manufacturing, which has created gaps in where and how FA will be handled. Gaps need to be filled, providing a challenge and an opportunity. I want to identify these gaps and provide ideas on bridging them. The fabless model is pervasive, as foundry capacity is now accessible to many companies. In this model, who owns FA? What about intellectual property concerns? Is the value of FA realized upfront or only in an emergency? These are some of the questions that, as a Society, we can help answer. I would like to provide

(continued on page 32)

SAVE THE DATE!

THE NEXT GENERATION FA ENGINEER

Failure analysis engineers are constantly challenged by next generation technology, materials, and equipment. Learn from experts, network with people who can support your work, explore the latest apps and tools for the lab, and keep up with the industry at ISTFA 2016. The expo floor at ISTFA, the largest FA equipment exposition in the country, is also a big draw because all the top companies are represented. Mark your calendar to attend ISTFA and see where the industry is headed for the next generation FA engineer.

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CANDIDATE PROFILES

CONTINUED FROM PAGE 30

our members with an FA roadmap and other information to help them in their work.

The value of EDFAS is directly tied to the perceived value of FA in our industry, and as a Society, we can help promote the importance of FA."

Becky Holdford worked as a failure analyst in the Semiconductor Packaging FA Team at Texas Instruments (TI) in Dallas, Texas, before retiring in 2015. The team was responsible for failure analysis development of the company's new packaging technology. She joined TI in 1978 after graduating with honors from Southern Arkansas University Technical Branch. She spent most of her TI career—31+ years—in wafer fab and product/packaging failure analysis. She has broad and deep experience in physical failure analysis techniques and was the group's cross-sectioning and SEM/EDX/FIB expert. Becky also taught these techniques to new hires and colleagues. A charter member of EDFAS, webmaster of the Lone Star (Texas) Chapter of EDFAS, and long-time member of the Microscopy Society of America, Becky is also a member of the Surface Mount Technology Association and IEEE.

Becky helped start the Lone Star Chapter of EDFAS and continues to be involved with that chapter, having served as vice-chair, chair, and now as webmaster. Her involvement with ISTFA began around 2000. Since then she has served in various capacities, such as reviewer, Session Chair, tutorial presenter, Tutorial Chair, and, in 2015, Audio/Visual Chair. Currently Becky is the Local Arrangements Chair for ISTFA 2016, to be held in Fort Worth, Texas.

VISION STATEMENT

"I want to keep EDFAS in the forefront of the failure analysis world. I want to extend its reach and relevance to all device and system failure analysts, no matter their experience or education level. EDFAS should be the first thing one thinks of when thinking about electronic FA training and information. We need to broaden the exposure of EDFAS to the world and increase the relevance of ISTFA in the industry. We can only do that by having valuable content and classes that are relevant. I think we, as a Society, should do more virtual seminars and tutorials, leveraging the advantages the internet has to offer to an industry that is spread all over the world. We should showcase EDFAS all year long, instead of just the once-a-year exposure of ISTFA."

Peter Jacob, Prof. Dipl. Ing., studied technical physics in Munich, Germany, with additional engineering training in the accelerator laboratories of Munich University. He started his professional career at IBM Germany, where he developed process failure analysis at the IBM semiconductor plant in Boeblingen/Sindelfingen. He later joined Hitachi Scientific Instruments in electron microscopy customer support and training and gave lectures in scanning electron microscopy for biologists at the Technical University Munich.

In 1993, Peter accepted a senior research position at ETH Zurich, where he developed an industry pool for failure analysis and reliability research and services. While there, his group earned the Lillehammer Award in 2002. In 1995, Peter joined EM Microelectronic Marin SA, the Swatch Group low-power CMOS fab near Neuchâtel, as the engineer responsible for failure analysis on both wafer-level and packaged devices. In that same year, his ETH working group moved to Empa (Swiss Federal Laboratories for Materials Testing and Research), joining the laboratory for reliability, electronics, and metrology.

In the past 25 years, Peter has published approximately 100 papers on various failure analysis topics, many of them at international conferences such as ISTFA, ESREF, and IPFA; these include three Best Papers and one Best Poster. He also organized or developed many seminars and tutorials on FA topics. In recognition for his SEM lectures, he was appointed in 2007 as Honorary Professor at Technical University Munich, and in 2010 he received the International Dresden Barkhausen Award for his activities in electrostatic discharge risk evaluation. Peter volunteers in the EUFANET organization.

(continued on page 34)

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CANDIDATE PROFILES

CONTINUED FROM PAGE 32

VISION STATEMENT

"EDFAS needs to be more involved in the further development of industrial procedures related to failure analysis, for example, 8D reports. My personal goal is to push EDFAS to develop toward "EDSFAS—Electron Device and System Failure Analysis Society." The failure analysis community of the future needs to extend its scope to a system-level view. The more complex the supply chains become, the more root cause becomes involved and must be considered. Besides the classic device failure analysis, which will always be limited by the actual available state-of-the-art analysis technologies, failure anamnesis and application characterization shall become more and more important to achieve the goal of root-cause discovery and making electronics more reliable."

Ted Lundquist, consultant, previously served as Chief Technology Officer, Director of Technology, and Applications Manager at DCG Systems Inc. in Fremont, Calif. (2008-2015). Prior to that, he was Applications Manager at Credence Systems Corp., Sunnyvale, Calif., and also at NPTest, Inc. of San Jose. Ted worked at Schlumberger ATE from 1994 to 2003 as an Applications Manager and Engineer. He received a Ph.D. in physics from the University of Maryland and has three FA patents.

Ted has been a member of EDFAS since 1997 and was a guest speaker at the first EDFAS-Taiwan Chapter meeting. He has been a reviewer of FA-related journals, led teams to win IARPA Circuit Analysis Tools contract awards, and has been a guest speaker at TSMC's Failure Analysis Workshop (2014) and the LSI Testing Symposium in Osaka, Japan (2010). He served as Circuit Edit Session Chair at ISTFA 2008-2011, was a panel expert for ISTFA 2011's "Finding the Invisible Defect," and is a profile author of ISTFA papers.

VISION STATEMENT

"The goal of EDFAS needs to be in maximizing the value delivered to our members. EDFAS recently established affiliations with other Societies interested in the failure analysis of electronic devices, such as IEEE-IPFA, IEEE-ESREF, and EUFANET. Could ISTFA sponsor FA sessions at other conferences, such as IEEE-IRPS, IEEE-ITC, IEEE-DATE, and so on, or work together with them? We could be delivering value to our members at other venues.

A challenge for many members is overcoming objections by their management when requesting to attend ISTFA. The Board of Directors needs to make it easier for upper management to approve attendance. Recently, failure analysis tools have been migrating to the fab lab, where they are being used for yield learning. A yield learning session might attract financial analysts and then catch the attention of upper management. Many companies have held small seminars on advanced topics in various IC-centric locations. These are typically well attended and are quite dynamic because they are small. Perhaps seminars can be sponsored and organized locally by EDFAS chapters but supported by the Society, with talent recruited by EDFAS."

Ryan Ross manages the Analysis and Test Laboratory at NASA's Jet Propulsion Laboratory (JPL), Pasadena, Calif., where he leads a team providing technical services to the JPL campus, enabling root-cause failure analysis, destructive physical analysis, extreme-temperature environmental testing emulating Martian conditions, electronic parts screening, and standard analytical services.

Prior to joining JPL in 2015, Ryan was one of the initial employees at Globalfoundries' greenfield startup Fab 8 foundry in New York, where he created a state-of-the-art Product Failure Analysis team. Ryan served as Globalfoundries' corporate representative on the SEMATECH Integrated Circuit Failure Analysis Council as member-at-large, Vice-Chair (2013), and Chair (2014), and served on the SEMATECH Package and Interconnect Failure Analysis Council.

Ryan worked for more than 10 years at Motorola Semiconductor, which later became Freescale Semiconductor (and now is part of NXP). In 2003, he accepted an assignment at the Crolles2 Alliance in France. In 2006, he joined the Tempe Technology Design Debug Lab and

(continued on page 56)

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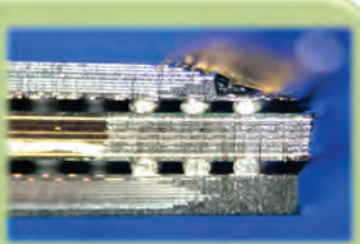

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EDFAS 2016 PHOTO CONTEST

OPEN TO ALL MEMBERS OF THE FAILURE ANALYSIS COMMUNITY!

SHARE YOUR BEST IMAGES WITH THE FAILURE ANALYSIS COMMUNITY AND BE RECOGNIZED FOR CREATING THEM!

SPONSORED BY THE MEMBERSHIP COMMITTEE OF THE ELECTRONIC DEVICE FAILURE ANALYSIS SOCIETY

Where: Selected entries will be displayed and prizes awarded November 6-10, 2016, at the 42nd International Symposium for Testing and Failure Analysis (ISTFA) Conference and Exposition in Fort Worth, Texas.

Categories: No more than one image per person allowed in each category

I. *Color Images Only* (*Optical Microscopy*)

II. *Black & White Images Only* (*Optical Microscopy/SEM/TEM/X-Ray/UV Micrographs/Other*)

III. *False Color Images Only* (*SPM/SAM/Photon Emission/Other*)

Images will be judged on failure analysis relevance (35%), aesthetics (35%), and novelty of the technique or mechanism (30%).

Deadline: Entries must be submitted by September 2, 2016.

Entries: Submit by e-mail to **photocontest@edfas.org** (subject line: EDFAS Photo Contest).

Format: Submissions should be made through e-mail only, with one picture attached. Each submission must be in a standard format (PNG, JPEG, TIFF, BMP, etc.). Please provide your highest-resolution image. The preferred submission is a .jpg or .tif, five inches wide at 300 dpi resolution.

Along with the picture, the e-mail should include the name of the submitter, category of submission, mailing address, phone, fax, e-mail address, and a description of the micrograph (not exceeding 50 words). The picture should not have any contact information embedded.

Copyright & Permissions: Entrants are responsible for obtaining any releases or any other permission or license necessary for the submission of their work for this contest and future publication. EDFAS and ASM International will have the right to exhibit, reproduce, and distribute in any manner any or all of the entries. The entries will not be returned to the submitters.

Prizes: **1st place** in each category receives a wall plaque and one-year complimentary EDFAS membership.

2nd and 3rd places in each category receive award certificates and one-year complimentary EDFAS memberships.

The top 10 entries in each category will be displayed at ISTFA 2016 in Forth Worth, Texas.

edfas.org

EDFAS 2016 VIDEO CONTEST

ARE YOU THE NEXT SCORSESE OF FAILURE ANALYSIS? WE HOPE SO!

Submit your 3 minute (or less) video about an exciting result or a scintillating artifact—anything goes as long as it relates to failure analysis! Your FA community will judge them and recognize winners at this year's ISTFA. Show off your filmmaking skills and FA prowess. **Upload your video today!**

Format: MPEG or AVI format with a maximum size of 50 MB. The video should be 3 minutes or less. Audio and subtitles are allowed. A short description should also be submitted along with all of your complete contact information.

Categories: **Failure Analysts:** Anyone working in the failure analysis field

Students: Students currently studying in fields related to failure analysis (physics/electrical engineering/chemistry/materials science, etc.)

Exhibitors

Deadline: September 30, 2016

Entries: Go to https://asm.confex.com/asm/istfa16/cfp.cgi

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Prizes: **1st place** receives a complimentary registration to a future ISTFA conference and a 1st place winner plaque.

2nd place receives a $25 gift card and award certificate.

3rd place receives an award certificate.

(Note: 2nd place will be awarded if total submissions are more than 10; 3rd place will be awarded if total submissions are more than 15.)

The top 10 entries in each category will be displayed at ISTFA 2016 in Fort Worth, Texas.

WIN ESTEEM AND RESPECT FOR YOURSELF AND YOUR COMPANY BY SUBMITTING THE WINNING VIDEO. LIGHTS, CAMERA...ANALYSIS!

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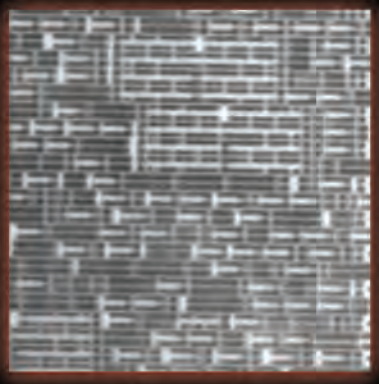
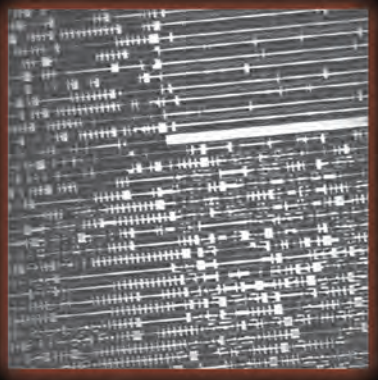
Visible Laser Probing

Debug Technologies from 10 nm to 5 nm

Checkpoint Technologies develops and manufactures optical failure analysis tools that are used by semiconductor manufacturers to improve the speed and reliability of integrated circuits. Checkpoint's role is to help integrated circuit manufacturers produce more reliable and better functioning electronic devices.



Vis SIL image of 16 nm technology
Magnification ~3200X



NIR 2.6 NA SIL image of 45 nm technology
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New Vis-SIL
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PRODUCT NEWS

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Larry Wagner, LWSN Consulting Inc.
lwagner10@verizon.net

SENSOFAR RELEASES NEW SURFACE PROFILER

Sensofar Metrology (Terrassa, Spain) has released a new high-resolution noncontact 3-D surface profiler in a more compact format, the S lynx. The new system draws from more than 14 years of experience in designing optical metrology systems for research and development as well as industry, enabling Sensofar to pack all the performance of Sensofar's S line of high-end 3-D surface profilers into a smaller platform.

Sensofar Metrology's S lynx

Despite the compact format, the S lynx still uses Sensofar's key three-in-one technology approach, namely the integration of confocal, interferometry, and focus-variation techniques into the same sensor head. This approach translates into unparalleled surface-measurement versatility over differing textures, structures, roughness, and waviness, all across varying surface scales. The S lynx now provides this same class-leading performance capability in a smaller footprint.

The S lynx comes equipped with a white-light-emitting diode light source, a high-resolution camera, and an encoded nosepiece for interchangeable objectives. There are no moving parts in the sensor head, improving stability, repeatability, and providing a very long lifetime with no maintenance.

The newly updated software interface, SensoSCAN 6, offers an even more intuitive interface and includes customizable tools as well as new and powerful analysis algorithms that have been especially designed for compatibility with current surface-measurement benchmarks (such as ISO standards).

The S lynx's versatility makes it appropriate for a broad range of high-end surface-measurement applications. Typical applications include automotives, consumer electronics, energy, liquid crystal display, materials science, microelectronics, micromanufacturing (electrical discharge machining, milling, or laser), micropaleontology, semiconductors, tooling, and watch manufacturing.

For more information: web: sensofar.com.

KEYSIGHT ANNOUNCES X-SERIES SIGNAL ANALYZERS

Keysight Technologies, Inc. (Santa Rosa, Calif.) announced new X-Series signal analyzers that provide significantly enhanced capabilities for developers creating next-generation devices. Most notable is a multitouch user interface (UI) that streamlines measurement setup and creates a solid foundation for new solutions. Performance improvements and feature enhancements address emerging needs in aerospace, defense, and wireless communications.

The UI enables optimization of measurement parameters in no more than two touches. Support for gesture-driven controls, such as pinching, dragging, and swiping, makes analysis more immediate and intuitive. With consistent operation across the UXA, PXA, MXA, EXA, and CXA, learning one means knowing them all.

To help developers create next-generation devices, the flagship UXA now offers frequency coverage to 44 or 50 GHz and integrated 1 GHz analysis bandwidth, an industry first. The PXA now offers benchmark phase-noise performance of −136 dBc/Hz at 1 GHz, 10 kHz offset, and real-time bandwidth of 510 MHz with a spurious-free dynamic range greater than 75 dBc over the full span.

"These advances in usability and performance show that Keysight is once again affirming its leadership in

(continued on page 42)

QuantumScope™
Failure Analysis Microscopes

FA engineers need proper tools in order to locate IC defects:

- ohmic shorts
- impedance issues
- leakage currents
- leaky capacitors
- oxide defects
- damaged junctions
- resistive vias
- CMOS latch up
- ESD damage
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QFI suggests maximizing your defect capture rate... NOT your capital expenditure rate.

QuantumScope™ integrates XIVA™ LSIM, Thermal-HS hot spot detection, and emmi™ photoemission into a single, high-performance, microscope platform. Semiconductor FA is more efficient and more accurate when the DUT remains mounted in a single diagnostic tool during all three of these FA microscope techniques. QuantumScope™ eliminates the need for multiple separate systems, freeing capital for other requirements. QFI systems are modular in design and generally compatible with field upgrade.

QFI Quantum Focus Instruments Corporation

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Fax: +1 (760) 599-1242
e-mail: sales@quantumfocus.com
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PRODUCT NEWS

CONTINUED FROM PAGE 40

signal analysis," said Mario Narduzzi, marketing manager of Keysight's Communications Solutions Group. "When engineers choose the X-Series, they get accessible performance that puts them closer to the answers they need to achieve their own breakthroughs at radio, microwave, and millimeter-wave frequencies."

Keysight's N9040B UXA X-Series signal analyzer

To characterize signal interactions in dense radar environments, the UXA and PXA support real-time data streaming at up to 255 MHz bandwidth with 16-bit resolution at 300 MSa/s. When coupled with a data recorder from solution-partner X-COM Systems, the analyzers support real-time acquisition with up to 15 TB (>3 h) of capture memory.

X-Series applications with multitouch simplify complex operations with proven, ready-to-use measurements for pulse analysis, analog demodulation, noise figure, phase noise, LTE/LTE-Advanced, and wideband code-division multiple access. The new pulse application accelerates the development and verification of chirped wideband signals, such as those used in advanced radars. Updates to the LTE/LTE-A application simplify characterization of systems that use carrier aggregation by supporting 256 quadrature amplitude modulation and providing visible configuration of all component carriers.

Using the strengths of the X-Series, the new N896xB noise-figure analyzer X-Series include a larger display, multitouch UI, and improved performance compared to their predecessors. These capabilities enhance a user's ability to make fast, accurate, and repeatable noise-figure measurements up to 40 GHz with a dedicated solution.

For more information: web: keysight.com/find/X-Series; tel: 970.679.5397; e-mail: janet_smith@keysight.com.

NANOPOSITIONING CONTROLLER AVAILABLE FROM nPOINT

LC.300 digital controllers from nPoint (Middleton, WI) are designed to operate closed-loop, flexure-guided nanopositioners with smooth linear motion and nanometer precision. nPControl Basic Software offers the capability to easily change proportional integral-derivative control parameters and apply notch filters via Windows-based graphical user interface. Controllers are compatible with capacitive or strain-gauge sensing technology for closed-loop operation. The LC.300 was designed with a small footprint for simple integration into original equipment manufacturer (OEM) environments. When combined with nPoint's line of nanopositioning stages, the LC.300's 20-bit resolution provides subnanometer positioning capabilities. As the latest addition to nPoint's nanopositioning electronics, the LC.300 series can be used in a variety of industries as an OEM system component.

Application examples include life science, microscopy, semiconductors, data storage, optics, materials science, and photonics packaging.

For more information: web: npoint.com; e-mail: justin.brink@npoint.com.

RBD INSTRUMENTS OFFERS AES ANALYZER

RBD Instruments, Inc. (Bend, Ore.) announced the release of the microCMA, its latest instrument for analyzing the top-most atomic layers of materials. "We are very excited to bring this new product to the surface analysis market. It will be an invaluable tool for researchers and scientists at universities and research facilities worldwide," said Randy Dellwo, President of RBD.

The microCMA is a compact cylindrical mirror analyzer (CMA) that measures the kinetic energies of electrons emitted from materials in a vacuum chamber. This type of analyzer is used in the Auger electron spectroscopy (AES) surface analysis technique, which is named after the French physicist Pierre Auger, who co-discovered the effect in the 1920s.

In use since the 1950s, AES has become a practical characterization technique in research areas such as surface chemistry and thin films. The first commercial

(continued on page 44)

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Extended Wavelength

IREM-IV Photon Emission Microscope

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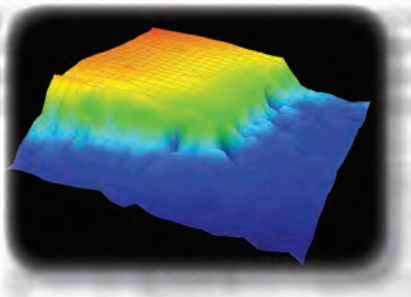
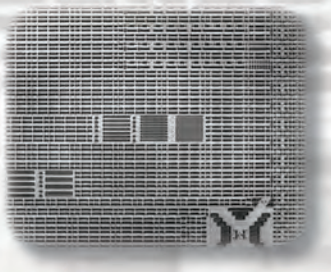
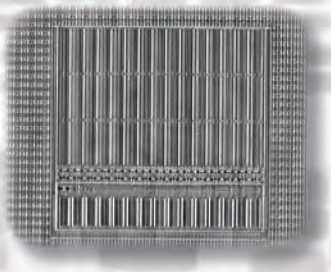


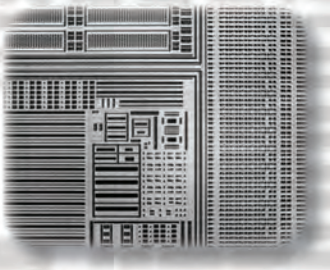
HIGHEST RESOLUTION
3.3 NA SIL Objective



MOST SENSITIVE
22nm Tri-Gate Device



LARGEST FIELD OF VIEW
Custom Optics



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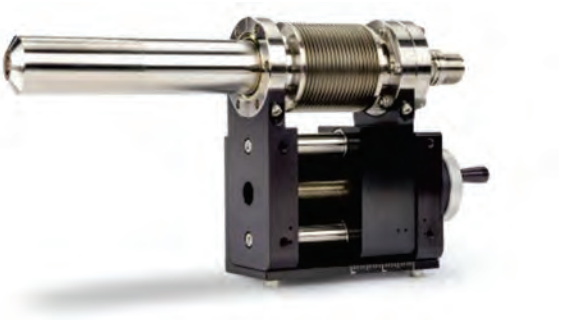
PRODUCT NEWS

CONTINUED FROM PAGE 42

Auger electron spectrometers were introduced in the early 1960s, and since that time, they have improved in performance, increased in size, and today can cost well over $1 million. RBD's microCMA provides high performance in a small form factor for a tiny fraction of what larger CMAs cost.



RBD Instruments' microCMA

"Our microCMA is a real game-changer in the world of thin-film surface analysis," Dellwo explained. Many analytical vacuum chambers have a small open port where the microCMA could be added. Installing a microCMA onto such an existing vacuum chamber can be an ideal way to add the AES surface analysis technique while eliminating the need for additional vacuum hardware.

By making the CMA smaller, the vacuum chamber and pumping requirements are also reduced, which help make AES much more affordable to researchers. Smaller vacuum chambers and pumps reduce the overall cost of a vacuum system by a significant amount.

The small size of the microCMA also makes AES practical as an analytical technique for small vacuum chambers used in research areas such as thermal desorbed spectroscopy and atomic layer deposition.

For more information: web: rbdinstruments.com; tel: 541.550.5016.

EM RESOLUTIONS INTRODUCES MAGNIFICATION STANDARDS

EM Resolutions (Essex, U.K.) has extended its range of resolution and magnification standards for scanning electron microscopy (SEM) with the introduction of the EM-Tec MCS and M series of magnification calibration standards. These fully featured practical calibration standards have been specially developed for magnification calibration or critical dimension measurements in tabletop SEM, standard SEM, field emission gun SEM (FEGSEM), focused ion beam (FIB), Auger, secondary ion mass spectrometry, and reflected-light microscope systems.

The EM-Tec MCS series is made using the latest MEMS manufacturing techniques with high-contrast chromium deposited lines for the larger features and gold-over-chromium for the smaller features below 2.5 µm. This ensures optimum signal-to-noise ratio for calibration purposes. The MCS-1 has a scale ranging from 2.5 mm to 1 µm and is ideal for tabletop and compact SEMs covering 10 to 20,000× magnifications. The MCS-0.1 scale covers a wider range, from 2.5 mm down to 100 nm, which is especially useful for 10 to 200,000× in SEM, FEGSEM, and FIB systems.

The M-10 calibration standard has a grid pattern etched in the surface of an ultraflat silicon substrate and provides a simple yet practical tool for magnification calibration and image-distortion assessments. The M-10, with a 10-µm-pitch grid pattern, is intended for 100 to 1000× magnification.

Both the MCS and M calibration standards are supplied with certificates of traceability. The MCS series has the option of an individual certificate of calibration. The MCS-0.1 calibration standard is an excellent replacement for the discontinued SIRA calibration standard, with added advantages.

These standards can also be supplied as part of the multistandard range. The commonly used "Gold on Carbon" and "Tin on Carbon" resolution standards can be combined on a stub of your choice with MCS or M series standards for quick and easy coverage of all the commonly used SEM calibrations.

For more information: web: emresolutions.com.

KEYSIGHT OFFERS ROBUST HANDHELD DMMs

Keysight Technologies, Inc. (Santa Rosa, Calif.) announced two new series of handheld digital multimeters (DMMs). In addition to offering the capabilities and measurement functions needed for the electronics and industrial test segments, the U1280 Series and U1240C Series handheld DMMs are extremely rugged and come with extended battery life to allow users to test and log data over a longer period of time.

With 60,000-count display resolution and 0.025% accuracy, the U1280 Series is Keysight's highest-performance handheld DMM. These 4.5-digit handheld DMMs offer the precision, accuracy, and repeatability engineers

Keysight's U1280 and U1240C Series handheld DMMs

need to meet the toughest requirements for electronics manufacturing, installation, and maintenance work in the electronics test industry.

The U1240C Series 4-digit handheld DMMs come with 10,000-count display resolution and 0.09% accuracy and provide a broad range of measurement functions for installation and maintenance work in industrial facilities. The U1240C Series also comes with unique features such as Z_{LOW} and harmonic ratio. Z_{LOW} provides low impedance mode to eliminate stray voltages. The harmonic ratio function gives an indication of the presence of harmonics.

"With extended battery life and IP 67 certification, the U1280 Series and U1240C Series are designed to be reliable, durable, and robust," said Ee Huei Sin, Vice President of Keysight's General-Purpose Electronic Measurement Division. "With these new handheld DMMs, engineers can confidently perform tests and troubleshoot over a longer period of time, even in tough electronics or industrial settings."

The U1280 Series and U1240C Series are very robust and are suited for operation in the field. These handheld DMMs are certified to IP 67 for complete protection against dust and immersion in water up to 1 m and are capable of withstanding up to a 3 m (10 ft) drop. Additionally, the U1240C Series is CAT IV 600 V and CAT III 1000 V compliant to improve user safety in electrical testing and measurement. Both series of handheld DMMs come with extended battery life—800 h for the U1280 Series and 400 h for the U1240C Series—so users can continue testing for longer periods of time. This is especially important for industrial test engineers whose ultimate goal is to keep the production line running seamlessly to prevent unplanned shutdowns.

For more information: web: keysight.com.

KEYSIGHT AFM SYSTEM DELIVERS ULTRAFAST SCAN RATES

Keysight Technologies, Inc. (Santa Rosa, Calif.) announced the availability of the ultrafast-scanning 9500 atomic force microscope (AFM). The Keysight 9500 AFM system seamlessly integrates new software, a new high-bandwidth digital controller, and a state-of-the-art mechanical design to provide unrivaled scan rates of up to 2 s/frame (256 × 256 pixels). Engineered with scientific and industrial research and development users in mind, the 9500 is the ideal system for an expansive range of advanced AFM applications associated with materials science, life science, polymer science, and electrical characterization.

The ultrafast scan rates of the 9500 AFM are made possible by Keysight's new Quick Scan technology. Available as a system option, Quick Scan is controlled through NanoNavigator, a powerful new imaging and analysis software package from Keysight. In addition to supporting Quick Scan functionality, NanoNavigator software allows researchers to save time by using a new autodrive feature that automatically and optimally sets all parameters for the 9500.

Novices and experts alike can appreciate NanoNavigator's efficient workflow-based graphical user interface as it guides users step-by-step through system setup and operation via intuitive, eye-catching visuals. For ultimate convenience, the NanoNavigator mobile app for smart phones and tablets allows remote monitoring of AFM experiments while they are being performed by the 9500.

The Keysight 9500 system offers a large (90 µm) closed-loop AFM scanner with atomic resolution, industry-leading environmental control, ultrahigh-precision temperature control, and much more. The 9500 delivers superior imaging in fluids, gases, and ambient conditions. Researchers also can use the 9500 to perform single-pass nanoscale electrical characterization. A new high-bandwidth, field-programmable gate-array-based digital controller ensures high-speed operating precision and eliminates the requirement for additional external control boxes.

The compact mechanical design of the 9500 affords researchers quick and convenient access to their samples. More than a half-dozen of the most commonly used AFM imaging modes (including Keysight's patented MAC Mode) are supported by the system's standard nose cone, which can easily be interchanged with specialized nose cones as needed, extending the 9500's capabilities effortlessly. Keysight also offers a scanning tunneling microscope scanner for studies of conducting materials and an inverted light microscope system for simultaneous AFM/optical imaging.

For more information: web: keysight.com.

TRAINING CALENDAR

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SEMICONDUCTOR ONLINE TRAINING

EDFAS offers online training specialized for semiconductor, microsystems, and nanotechnology suppliers and users. These online training courses are designed to help engineers, technicians, scientists, and managers understand each of these dynamic fields. This one-year subscription provides access to several courses covering semiconductor failure analysis, design, packaging, processing, technology, and testing. Find out more by visiting edfas.org and clicking on Education.

May 2016

EVENT	DATE	LOCATION
Metallography for Failure Analysis	5/2-5	Novelty, OH
Contact: ASM International		
27th Annual SEMI Advanced Semiconductor Manufacturing Conference	5/16-19	Saratoga Springs, NY
Contact: ASMC 2016		
Failure and Yield Analysis	5/17-20	Munich, Germany
EOS, ESD and How to Differentiate	5/23-24	Munich, Germany
Semiconductor Reliability and Qualification	5/30-6/2	Munich, Germany
Contact: Semitracks, Inc.		
IMEC Technology Forum 2016 Brussels	5/24-25	Brussels, Belgium
Contact: IMEC		

June 2016

EVENT	DATE	LOCATION
Introduction to SEM and EDS for the New Operator	6/5	Bethlehem, PA
Scanning Electron Microscopy and X-Ray Microanalysis	6/6-10	Bethlehem, PA
Focused Ion Beam: Instrumentation and Applications	6/6-10	Bethlehem, PA
Problem Solving: Interpretation and Analysis of SEM/EDS/EBSD Data	6/6-10	Bethlehem, PA
Quantitative X-Ray Microanalysis: Problem Solving Using EDS and WDS Techniques	6/6-10	Bethlehem, PA

June 2016 (cont'd)

EVENT	DATE	LOCATION
Scanning Transmission Electron Microscopy: From Fundamentals to Advanced Applications	6/6-10	Bethlehem, PA
Contact: Lehigh Microscopy School		
Advanced Imaging Techniques for Scanning Electron Microscopy	6/6-7	Westmont IL
Advanced X-Ray Microanalysis by EDS	6/8-10	Westmont IL
Polarized Light Microscopy	6/13-17	Westmont IL
Microscopy Workshop for Middle and High School Science Teachers	6/20-24	Westmont IL
Contact: McCrone Group		
Advanced Thermal Management and Packaging Materials	6/7-8	Albuquerque, NM
Contact: Semitracks, Inc.		
ANADEF Workshop 2016	6/7-10	Seignosse-Hossegor (Landes), France
Contact: ANADEF 2016		
Scanning Electron Microscopy	6/13-16	Lansing, NY
Introduction to Metallurgical Lab Practices	6/20-22	Novelty, OH
Contact: ASM International		

July 2016

EVENT	DATE	LOCATION
IMEC Technology Forum 2016 USA	7/11	San Francisco, CA
Contact: IMEC		
Semiconductor Reliability	7/11-13	Singapore, Singapore
Contact: Semitracks, Inc.		

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NOTEWORTHY NEWS

IPFA 2016

The 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2016) will be held **July 18 to 21, 2016**, at Marina Bay Sands, Singapore. The event will be devoted to the fundamental understanding of the physical mechanisms of semiconductor device failures as well as issues related to semiconductor device reliability and yield, especially those related to advanced process technologies.

IPFA 2016 is organized by the IEEE Reliability/CPMT/ED Singapore Chapter. The Symposium is technically co-sponsored by the IEEE Electron Device Society and IEEE Reliability Society.

For more information, visit the IPFA website at ieee-ipfa.org/2016/.

NOTEWORTHY NEWS

MICROSCOPY & MICROANALYSIS 2016 MEETING

The Microscopy & Microanalysis (M&M) 2016 meeting will be held **July 24 to 28, 2016**, at the Columbus Convention Center in Columbus, Ohio. The Scientific Program features the latest advances in the biological and physical sciences as well as techniques and instrumentation. Complementing the program is one of the largest exhibitions of microscopy and microanalysis instrumentation and resources in the world. Educational opportunities include a variety of Sunday short courses, tutorials, evening vendor tutorials, pre-meeting workshops, and in-week intensive workshops. The opening reception offers an opportunity to meet new people in the field and renew old acquaintances, and the Monday morning Plenary Session features showcase talks from outstanding researchers as well as recognition of the major Society and Meeting award winners. There will be other important awards conferred during the meeting, including daily poster awards to highlight the best student posters in instrumentation and techniques as well as biological and physical applications of microscopy and microanalysis.

M&M is sponsored by the Microscopy Society of America and the Microanalysis Society. For more information, visit microscopy.org or microbeamanalysis.org.

MASTER FA TECHNIQUE

SEALANT/CAULK MATERIAL AIDS DECAPSULATION OF ELECTRONIC COMPONENTS

Contributed by Bill Ross, Pelseal Technologies, LLC
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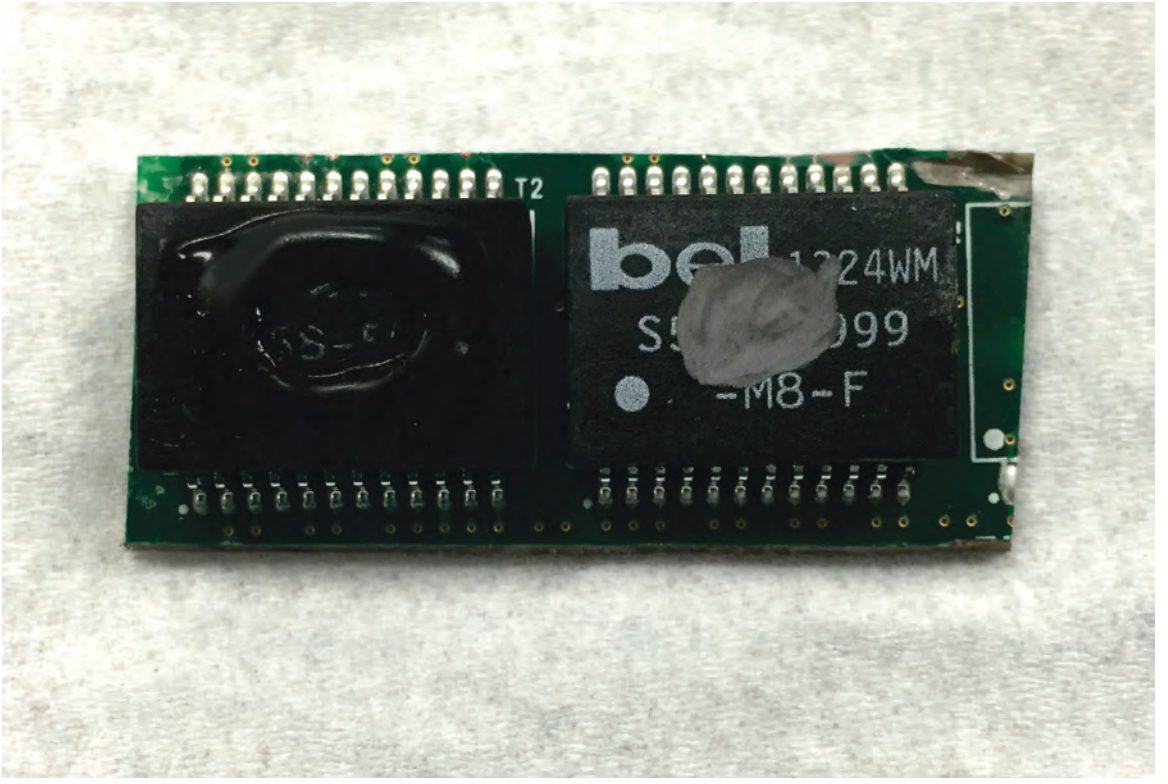
Most failure analysis labs are challenged by new problems and existing equipment. Old techniques must be modified to be effective on new technology. *EDFA* readers are encouraged to submit examples of master FA techniques for future publication.



Two identical (side-by-side) components with caulk well on the left and carved well on the right. Photo courtesy of ACI Technologies

Engineering research company ACI Technologies is tasked with decapsulation of electronics components for testing and investigative purposes. In the normal method of decapsulation, an analyst uses a rotary tool to drill a small indentation in the hermetic sealant material and then applies nitric acid to eat through the polymeric encapsulant.

The company performs this decapsulation for a number of purposes, including wire bond inspection, operational testing, and counterfeit investigation. This testing method allows the operator to explore a silicon die while it is still on a functioning board. Typical pieces being tested are 5 × 5 mm in size.

THE PROBLEM

In the traditional method of decapsulation, the operator makes a small well above the location of the die and places the component in a tin tray on top of a 140 °C hot plate. The operator adds nitric acid in a dropwise fashion into the well to allow digestion of the packaging material.

MASTER FA TECHNIQUE

After 10 to 30 s, the acid is rinsed with acetone for neutralization. The process is repeated until the die and wire bonds of the package are exposed.

While the rotary-tool method is the standard practice, it does have some drawbacks:

- The drilling process introduces an outside source of disruption to the device.
- The drilled well still allows the nitric acid to flow from the surface of the encapsulant.
- It is difficult to direct where the acid is working on the encapsulant.

THE SOLUTION

Faced with the shortcomings of the current process, the company set out to find a better solution. They discovered that Texas Instruments had successfully used a 2078 Viton Caulk from Pelseal Technologies to assist with decapsulation. This caulk exhibits strong chemical properties and remains flexible in service. The company decided to adopt this approach by using the caulk to build up a well to contain the nitric acid, rather than drilling into the component.[1]

To form the well, ACI built up approximately 2 to 4 g of caulk above the die location (in place of carving out a small well) and placed the component on the hot plate. When the component reached the correct temperature, the operator dropped nitric acid into the fabricated well to allow digestion of the packaging material. This was then rinsed with acetone, and the process was repeated until the die was exposed.

After using the caulk-constructed well method of decapsulation, the company found:

- By not drilling directly into the surface of the die, no additional mechanical damage was introduced.
- Electrostatic discharge/electrical overstress was removed from the equation, thus increasing the confidence in the results.
- The caulk adheres easily to a wide range of component materials.
- The caulk was easily removed after decapsulation by simply tugging on it with a pair of tweezers. (The caulk stood up to repeated acetone rinse steps.)
- The deposition of the caulk permits outlining of various geometries, making it possible to use it with a wide range of die sizes and shapes.
- Safety is increased by creating a well on the surface of the die that stands above the original topography, eliminating any splashing or accidental misuse of concentrated acids.
- A larger quantity of acid could be used in the caulk-constructed well, resulting in less time needed for the decapsulation process.

After determining that the use of a caulk well made the decapsulation process easier and more effective, the engineering research company decided to continue using the caulk, and they plan to integrate it into their standard decapsulation procedures.

REFERENCE

1. K.D. Staller: "Safe Decapsulation Techniques Using Viton Caulk," *Proc. 40th Int. Symp. Test. Fail. Anal. (ISTFA 2014),* Nov. 9–13, 2014 (Houston, Texas).

LITERATURE REVIEW

Peer-Reviewed Literature of Interest to Failure Analysis: Optics, Optical Techniques, and a Ripple in the Universe

Michael R. Bruce, Consultant
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The current column covers peer-reviewed articles published since 2014 on optical microscopy, optical fault isolation techniques, photon detectors, and one giant wave. Optical methods and techniques are fundamental to nondestructive analysis of modern integrated circuits. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

- B.P. Abbott et al.: **"[Nondestructive] Observation of Gravitational Waves [Using Laser Interferometry] from a Binary Black Hole Merger,"** *Phys. Rev. Lett.,* 2016, *116,* p. 061102. Also see **"Viewpoint: The First Sounds of Merging Black Holes,"** *Physics,* Feb. 11, 2016, *9*(17), physics.aps.org/articles/v9/17. (Editor's note: No black holes were destroyed by this measurement.)
- K. Agarwal, R. Chen, L.S. Koh, et al.: **"Crossing the Resolution Limit in Near-Infrared Imaging of Silicon Chips: Targeting 10-nm Node Technology,"** *Phys. Rev. X,* 2015, *5,* p. 021014. See also **"Synopsis: Zooming in on Failures,"** *Physics,* May 6, 2015, physics.aps.org/synopsis-for/10.1103/PhysRevX.5.021014.
- R. Attota, and R.G. Dixson: **"Resolving Three-Dimensional Shape of Sub-50 nm Wide Lines with Nanometer-Scale Sensitivity Using Conventional Optical Microscopes,"** *Appl. Phys. Lett.,* 2014, *105,* p. 043101.
- L. Bidani, O. Baharav, M. Sinvani, and Z. Zalevsky: **"Usage of Laser Timing Probe for Sensing of Programmed Charges in EEPROM Devices,"** *Dev. Mater. Reliab., IEEE Trans.,* 2014, *14,* p. 304.
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- T.B. Cilingiroglu, A. Uyar, A. Tuysuzoglu, et al.: **"Dictionary-Based Image Reconstruction for Superresolution in Integrated Circuit Imaging,"** *Opt. Express,* 2015, *23,* p. 15072.
- I. De Wolf, **"Relation between Raman Frequency and Triaxial Stress in Si for Surface and Cross-Sectional Experiments in Microelectronics Components,"** *J. Appl. Phys.,* 2015, *118,* p. 053101.
- R. Horstmeyer, R. Heintzmann, G. Popescu, et al.: **"Standardizing the Resolution Claims for Coherent Microscopy,"** *Nat. Photon.,* 2016, *10,* p. 68.
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- W. Lei, J. Antoszewski, F. Jarek, et al.: **"Progress, Challenges, and Opportunities for HgCdTe Infrared Materials and [MCT] Detectors,"** *Appl. Phys. Rev.,* 2015, *2,* p. 041303.
- U. Leonhardt and S. Sahebdivan: **"[Using Far-Field Optics for Near-Field Sub-Wavelength Imaging:] Theory of Maxwell's Fish Eye with Mutually Interacting Sources and Drains,"** *Phys. Rev. A,* 2015, *92,* p. 053848.
- M.A. Miller, P. Tangyunyong, and E.I. Cole, Jr.: **"Characterization of Electrically-Active Defects in Ultraviolet Light-Emitting Diodes with Laser-Based Failure Analysis Techniques,"** *J. Appl. Phys.,* 2016, *119,* p. 024505.
- N. Naka, S. Kashiwagi, Y. Nagai et al.: **"Micro-Raman Spectroscopic Analysis of Single Crystal Silicon Microstructures for Surface Stress,"** *Jpn. J. Appl. Phys.,* 2015, *54,* p. 106601.
- C. Park, J.-H. Park, C. Rodriguez, et al.: **"Full-Field Subwavelength Imaging Using a Scattering Superlens,"** *Phys. Rev. Lett.,* 2014, *113,* p. 113901.

- Z. Qui, R.S. Wilson, Y. Liu, et al.: **"Translation Microscopy (TRAM) for Super-Resolution Imaging,"** *Sci. Rep.,* 2016, *6,* p. 19993.
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GUEST EDITORIAL

(CONTINUED FROM PAGE 2)

or a purely functional fault inside a system-in-package? The right tool has not yet been built. Acoustic and x-ray tomography are still evolving to provide incredible and accurate resolution, but it may not be enough when the defect must first be localized to reduce the area to investigate with other tools.

We are facing analyses on complex, small systems that have embedded wireless, self-power, various sensors, and actuators. There is not yet a combination of multiphysics tools to locate where the defect is, because the system is often built in a sequential manner: sensor, processing, wireless transmission/actuator. Built-in self-test could help a lot if it integrates the multiphysics—not only electrical—aspects of these devices, but it won't fully replace FA tools and techniques. It will be even worse with the expected development of the Internet of Things.

Last, but not least, nanoelectronics are everywhere. They are a big success story with some side effects for FA. Small- and medium-sized companies are developing new products with an incredible diversity in the technologies used. Remote health monitors, mobile applications, wearable electronics, organic electronics, and plenty of other new fields are included. Unfortunately, each market is too small and not necessarily well identified to encourage tool manufacturers to develop adapted tools for these markets.

It is the right time for the electronics industry to understand that the FA supply chain is fragile and needs common efforts to develop the right tools and techniques.

It is the right time for tool manufacturers to address these new needs and to adapt and customize their tools or develop new ones.

It is the right time for experienced failure analysts to actively participate in the FA tool paradigm shift. EDFAS will play a key role in cross fertilizing the global efforts of all interested FA engineers.

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DIRECTORY OF INDEPENDENT FA PROVIDERS

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Electronic companies of all types and sizes require failure analysis (FA) services. Our goal is to supply a resource of FA service providers for your reference files. The directory lists independent providers and their contact information, expertise, and types of technical services offered.

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NOTEWORTHY NEWS

ITC 2016

The International Test Conference (ITC) will be held **November 15 to 17, 2016**, at the Fort Worth Convention Center in Fort Worth, Texas. ITC is the world's premier conference dedicated to the electronic test of devices, boards, and systems and covers the complete cycle from design verification and validation, test, diagnosis, failure analysis, and back to process, yield, reliability, and design improvement. At ITC, test and design professionals can confront the challenges the industry faces and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

ITC, the cornerstone of TestWeek events, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including formal paper sessions, tutorials, panel sessions, case studies, a lecture series, commercial exhibits and presentations, and a host of ancillary professional meetings.

ITC is sponsored by the IEEE. For more information, visit itctestweek.org.

GUEST COLUMNIST

THE PROCESS OF INVENTING A PATENTABLE ITEM

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Today's professionals are continually pushed to deliver innovation to ensure that a company can remain competitive and, more importantly, profitable in the global market. There are many ways to show innovation, whether it's through internal continuous-improvement projects, the formation of trade secrets, or the strongest method, obtaining patents. Patents are essentially the backbone of industry. A patent provides protection that an innovation will not be used by others for their financial gain. How important are patents to a company? Ask Samsung—they fought a fierce battle with Apple for several years over phone patents covering 40 or more infringements. In 2012, Apple was awarded 1 billion dollars in damages.[1] For many companies, this could be an unrecoverable judgment. It is a considerable amount of money for an idea that was turned into a reality by two separate companies, but only one of them held the patent.

Major changes to the way patents are awarded occurred in 2013 with the implementation of phase III of the America Invents Act.[2] The most important change was the conversion from a first-to-invent system to a first-inventor-to-file system.[3] This places at serious risk all in-progress inventions that are being tinkered with to attain the perfect product before a patent application is filed. If it has not been filed with the U.S. Patent and Trademark Office, it is not protected.

Another significant change is that U.S. patents and U.S. patent application publications as "prior art" are now treated according to their earliest effective filing date, regardless if that date is based on an application filed in the United States or in another country. Also eliminated was the requirement that a prior public use or sale be "in this country" to qualify it for prior-art activity.

What does all this boil down to? If you have an idea, sketch it out on paper, describe it in as much detail as possible, and file it, even if there isn't a final product or the beginning of one. Ideas can be patented; they don't have to physically exist.

Every year there's a drive to obtain new patents. I'm frequently asked, "When can failure analysis provide a new patent idea, and what would it be about?" Because failure analysis does not deal in the direct manufacturing of devices nor with the equipment used, it can be challenging to come up with an invention, especially one that would directly impact the semiconductor industry. Certainly, there are numerous ideas for improving the analytical side for lab efficiency or capability, but it may not be of interest to the company. After all, we are not making analytical equipment, so a patent in that area isn't as beneficial or profitable to pursue.

> "BEING FAILURE ANALYSTS, WE DIDN'T HAVE THE RESOURCES TO CREATE A WAFER WITH THESE EXPOSED *p/n* JUNCTIONS, AND THEREFORE, WE DIDN'T HAVE AN OPERATIONAL DEVICE, BUT THAT DIDN'T STOP US FROM FILING FOR A PATENT. THE THEORY BEHIND THE PHENOMENON WAS SOLID, AND THE FINDINGS WERE REPRODUCIBLE.. "

Nevertheless, failure analysis personnel are in a key position within the semiconductor process. We interact with virtually every engineering team in the organization, which exposes us to all facets of the business. Failure analysts actually "see" the product—electrically, optically, in the SEM, cross sections, top-downs, and so on. Observation is often the key to inspire creative thinking, which leads to an idea, and an idea can lead to a patent. Of course, that's easier said than done. Looking at circuits all day, every day can lead to autopilot, squashing creativity. However, seeing the same thing over and over can also be beneficial. We tend to eagerly chase things that are observed as being different from the "normal" findings. A new anomaly will receive much more attention and will be studied in greater detail, due to our curious nature. Even an accident, whether in sample preparation or handling, can ultimately lead to a great invention.

A good example of a patentable idea that resulted from observation happened to a colleague and me some years ago. The structure being analyzed was testing gate oxide breakdowns. Several of the failed samples were deprocessed to expose the poly layer, where silicon-selective etching with choline hydroxide was used to uncover the gate oxide. The etch removed the poly layer and, because there was a hole in the gate oxide, it also etched a small amount of the silicon substrate at the breakdown point. The location, size, and pattern of the breakdown can normally be seen through low SEM voltage settings. On these particular samples, a large quantity of particles propagated out of the holes after etching. At first we assumed there was contamination in the oxide and these particles were the root cause of the problem. Energy-dispersive spectroscopy revealed that the particles were comprised of metallic elements—bad news for the gate oxide process. However, the particles were odd-looking, as if they were grown one on top of the other, and they were large enough that they should have been seen optically at the poly stage. So, what was their origin?

A close examination of the sample-preparation process found that metal tweezers were used while etching the poly, and they were the source of the particles. That finding began an investigation into why the particles were attracted to the holes in the gate oxide. It was discovered that when the semiconductor device was optically illuminated, a *p/n* junction was formed as a result of photovoltaic phenomena. The metal ions from the etch solution, where the metallic tweezers had been used, migrated to the oxide hole area due to the voltage pull created at the *p/n* junction, leading to the buildup of ions. What a great way to tell if there's metal contamination in a solution, but who besides failure analysts has access to an SEM to look at the sample after exposure? We needed a device and method that was easy to use and practical for trapping metal ions and detecting the metal ion contamination in a solution.

A very simple circuit design was drawn up with electrical leads connected to two small exposed *p/n* junctions in close proximity. After the circuit is exposed to the solution, the resistance can be measured between the junctions. Depending on the space between the two junctions and the amount of time exposed to the solution, the quantity of metal ion can be determined. Being failure analysts, we didn't have the resources to create a wafer with these exposed *p/n* junctions, and therefore, we didn't have an operational device, but that didn't stop us from filing for a patent. The theory behind the phenomenon was solid, and the findings were reproducible. Illustrations of our circuit were drawn up, a brief description of the process and what it would accomplish was written, and a filing was submitted.[4] It was literally that easy. Of course, from that point the lawyer or patent attorney took over and added any other variations that could be incorporated into the invention, as well as the appropriate wording. Before the patent was finally awarded, it took several years to go through the entire process of searches to ensure that the idea did not previously exist. It was worth the wait.

Now, you're probably thinking, "Wait a minute. This patent doesn't have anything to do with the foundry business." That is true; we most likely will never manufacture this invention, but that doesn't mean the patent has no value for the company. Patents can be licensed or sold to other companies. Through that possibility, we may end up making those circuits for another company, thereby providing profitability for them and for us. So, all those ideas for improving the analytical side for lab efficiency or capability may still be worth the pursuit.

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ABOUT THE AUTHOR

Jason Higgins graduated from ITT Technical Institute with a Bachelor's degree in automation robotics. He joined TSMC WaferTech in 1997 as a reliability FA engineer and lab supervisor. Jason specializes in fault isolation and physical failure analysis on low-yield and field-return samples from a variety of product functions and technologies. He has been an Associate Editor of *EDFA* magazine since 2008.

CANDIDATE PROFILES

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assumed ownership of the FIB circuit edit operation. He later transitioned into management of the Freescale Global Yield FA Laboratories, where he was responsible for FA teams in Arizona and Malaysia.

Before transitioning to the FA world, Ryan worked at Intel's Chandler Assembly and Test location after earning his Bachelor of Science degree in electronic engineering technology from DeVry Institute of Technology.

Active in ISTFA, Ryan was a panelist on the ISTFA 2015 New Product Introduction Panel, authored or co-authored four papers, served as Co-Chair of the Circuit Edit Session (2009), and reviewed submissions for the ISTFA 2012 Photon-Based Techniques Committee.

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