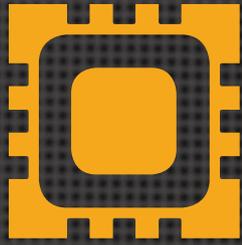


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# ELECTRONIC DEVICE FAILURE ANALYSIS™

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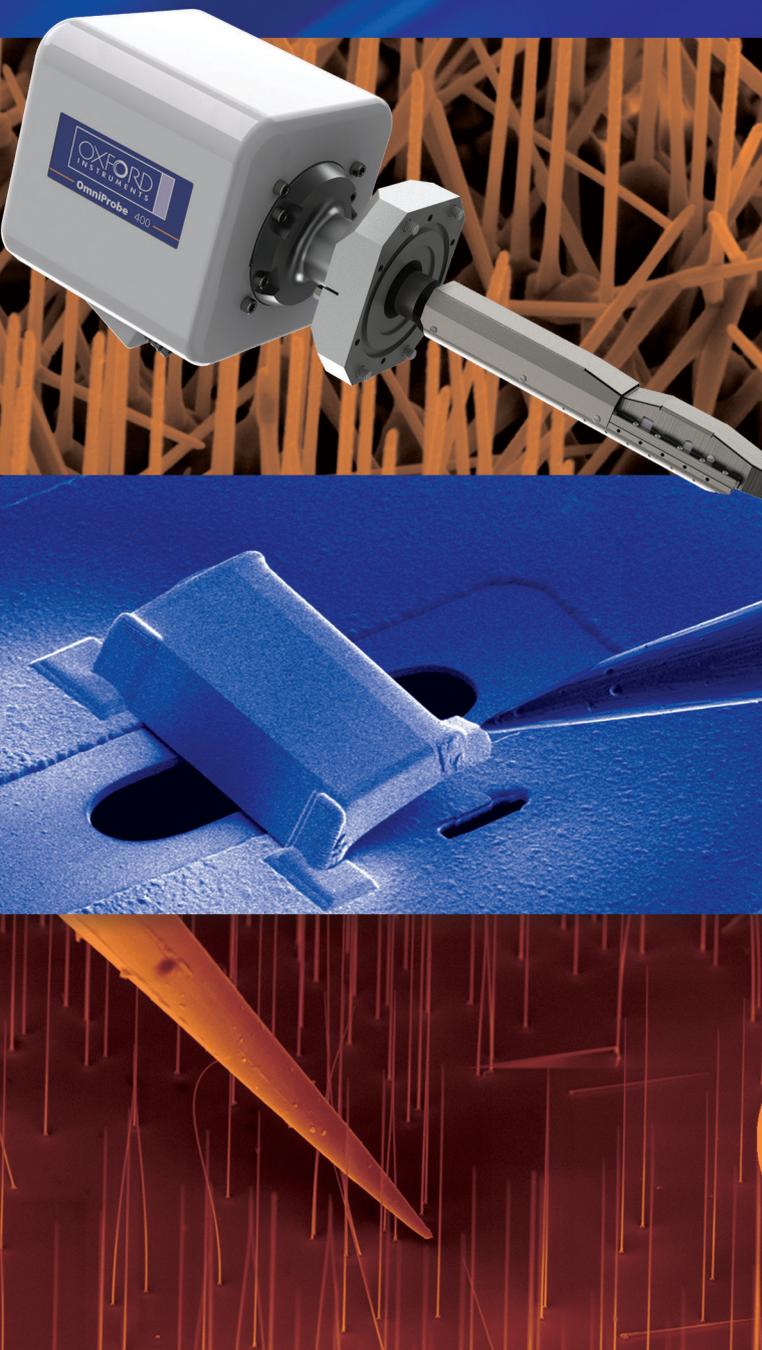


# ANALYSIS

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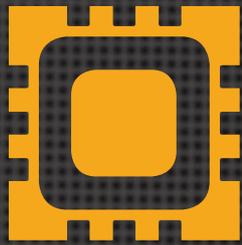
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# ELECTRONIC DEVICE FAILURE ANALYSIS™

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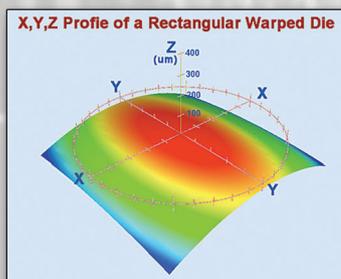
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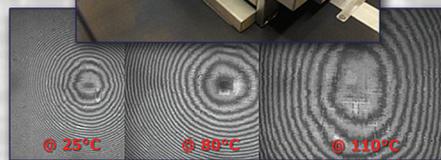
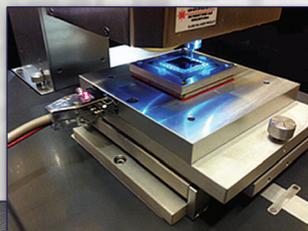


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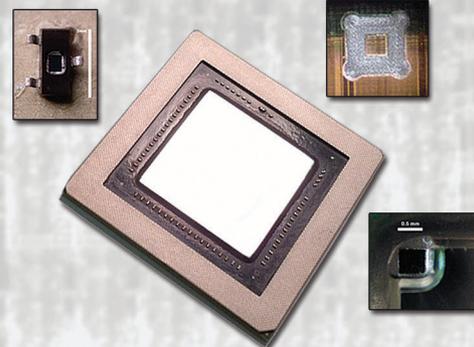
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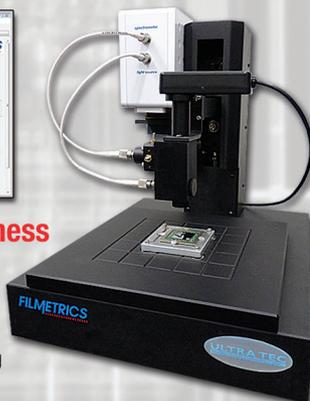
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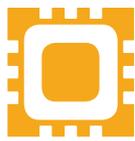


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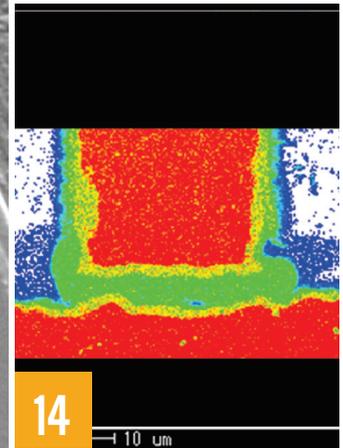
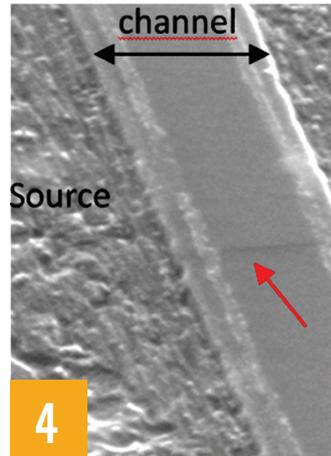
# ELECTRONIC DEVICE FAILURE ANALYSIS™

A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS

## 4 Silicon Pipeline or Dislocation Defect?

Yann Weber

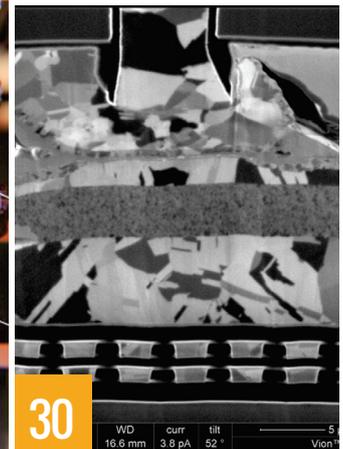
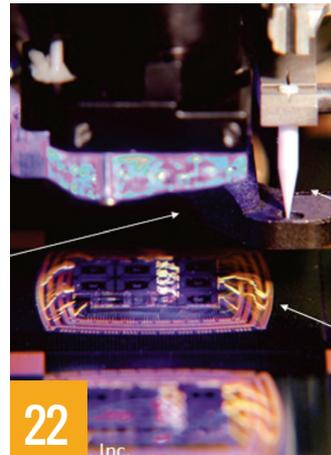
This paper presents case studies of silicon pipeline defects and dislocations found on mixed-mode technology.



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## 22 Wire Bonding

Lee Levine

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A recap of the ISTFA 2015 event includes General Chair James Demarest's wrap-up as well as a list of the ISTFA Best and Outstanding Papers and Posters. A summary of the Panel Discussion and highlights from the four User Groups can be found starting on page S-1

### ABOUT THE COVER

"Shock and Awe." Optical image of an actuator coil wire that had fractured during aging and curing of the encapsulating epoxy. The features observed were secondary shock cracks in the cured epoxy when the wire fractured. *Photo by Michael Woo, Raytheon Failure Analysis Lab, First Place Winner in Color Images, 2015 EDFAS Photo Contest.*

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For the digital edition, log in to [edfas.org](http://edfas.org), click on the "News/Magazines" tab, and select "EDFA Magazine."

**PURPOSE:** To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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## FA TOOLS AND IC SECURITY

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To understand how great the risk of failure analysis (FA) and debug techniques is to electronic hardware security, one should look more closely at what is done while applying FA to a digital circuit. We analyze the digital signal and study the failure mode with, for example, scan path testing, but that is just the beginning of the investigation. We also start to extract analog information and evaluate signal levels, current profiles, and so on. If all of this does not lead us to isolate the failure, then physical interaction becomes our focus in order to trace the signal and identify the failing node. Many of these techniques show not only failing locations but logical states and perfectly operating signal tracks as well. The tools and practices that help us with FA on the flip side also enable hackers to gain access to secret information on the flop side of the IC. The so-called side-channel attacks (SCAs) read personal codes or passwords to open paths into illegal IC operation. In addition, circuit edit (CE) opportunities with the focused ion beam, previously used to gain access to initially secure signals, can be employed to create ones and zeros in memories such as SRAM by producing the proper opens and shorts and thereby write and duplicate access codes into authentication products.

When the knowledge of how to perform such SCAs spreads to attackers, the most important risk drivers will be:

- Easy and low-cost access to the tools and people who own and operate them
- Simple and inexpensive tool alternatives that hackers can easily maintain in their garage labs

As a countermeasure, security circuit designers have developed systematic protection against electrical side channels by cryptologically perturbing the signals. The physical side-channel risk (mainly optical, such as photon emission or laser stimulation; especially interesting is fault injection) has been prohibited by an extra metal layer with a resistor grid that notifies the circuit if it is fully or partially removed. This seemed like good protection in the smart card world, dealing with a low number of interconnect levels, until the first optical attacks through the chip backside were reported. This happened a few years ago, and it opened a new phase of hardware challenges.

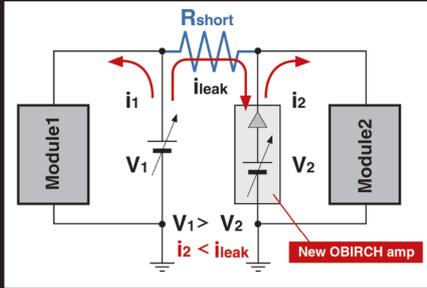
Not only has backside access circumvented topside protection, but the even more threatening fact is that, through the backside, there is no partial covering and shadowing or shielding of metal interconnects in the optical path, so all nodes are quantitatively comparable. That way, reading SRAM

(continued on page 49)

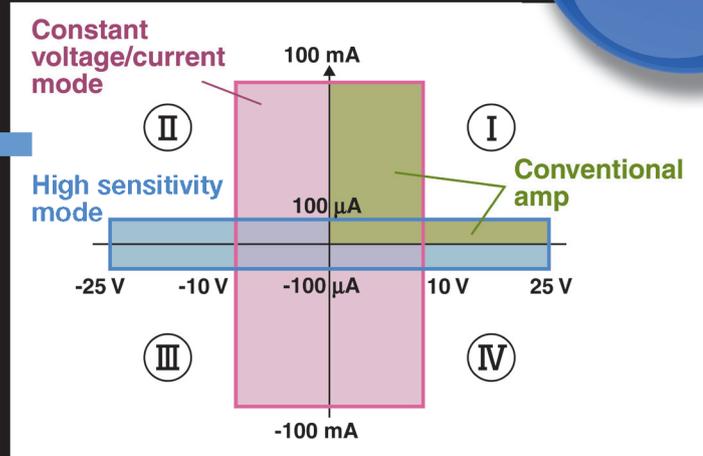
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# SILICON PIPELINE OR DISLOCATION DEFECT?

Yann Weber, Freescale Semiconducteurs France SAS  
yann.weber@freescale.com

## INTRODUCTION

The study of dislocations in semiconductors parallels the development of the electronics industry. These silicon bulk defects commonly affect device technology due to many sources of variation from physical and manufacturing processes.<sup>[1]</sup> Continual quality improvements combined with constant economic pressure require a reduction in the number of these defects, which result in wafer fab manufacturing yield loss qualification failures or customer returns. Upstream from this long-term goal, the first requirement is to better understand and categorize the defect's effect in order to implement corrective actions. In this strategy, the failure analysis (FA) process must overcome traditional limits in terms of efficiency, responsiveness, and the technical methods used. This paper presents case studies of silicon pipeline defects (called "pipeline") and dislocations found on mixed-mode technology. Pipeline defects are specific dislocations that are widely reported to occur in CMOS and BiCMOS devices<sup>[2,3]</sup> and recently in silicon-on-insulator devices; the main distinction is that pipeline defects are considered to connect the source and drain regions of an NMOS transistor by diffusion of *n*-type dopants.

## CHALLENGE OF DETECTING PIPELINE DEFECTS

The two main concerns are the difficulty in screening out silicon crystallographic defects created during wafer fab processing, and how to correctly perform physical investigations to determine their nature. Several authors<sup>[2,3]</sup> have reported this type of defect in semiconductor devices, but there is no proposed methodology to complete any FA work and to separate the different causes. In this study, diverse complementary advanced techniques have been combined to highlight these unusual silicon crystal defects. Starting with electrical investigations, the

electrical impact of those latent defects causes parametric or functional failures. Then, fault localization techniques such as infrared, emission microscopy (EMMI), or thermal laser stimulation (TLS) help to identify the impacted device and to localize defects; direct electrical measurements using a nanoprobe atomic force probe (AFP) determined the defective NMOS pattern fingers. Physical analyses with various techniques, including physical deprocessing and crystalline delineation etches, atomic force microscopy (AFM), scanning microwave microscopy (SMM),<sup>[4,5]</sup> secondary electron microscopy (SEM), and transmission electron microscopy (TEM) analyses, continued the inquiries. The combination of techniques, the defect locations, and their physical signatures are key to discriminating the difference between dislocation and pipeline defects. Finally, the section "Discussion: Pipeline or Dislocation" provides guidelines for distinguishing dislocation and pipeline defects and deals with potential wafer fab manufacturing processes that cause these two types of defects.

## FAILURE ELECTRICAL CHARACTERIZATION METHODS

More than 14 case studies using identical 250 nm mixed-mode devices on standard substrate have been investigated to support the results presented. Different failure modes (parametric or functional) impacted the products at different steps of their lifetime. Customer returns and yield-loss parts were explored. Then, complementary physical investigations were performed. The purpose of this cross-checking data is to determine any influence of the nature of the physical defect and to evaluate the physical analysis, allowing a distinction to be realized with a high level of confidence. The parameters are summarized in Table 1. These types of defects were not limited to one specific element and were found in various types of devices, such as electrostatic discharge

*This article is based on the paper "Advanced Failure Analysis on Silicon Pipeline Defects and Dislocations in Mixed-Mode Devices" by Y. Weber, J. Goxe, S. Alves, T. Zirilli, and M. Castignolles, Freescale Semiconducteurs France (Toulouse); S. Subramanian, Freescale Semiconductor Inc. (Austin, TX); Y. Tsang, Globalfoundries (formerly of Freescale USA); and K. Harber, TriQuint Semiconductor (formerly of Freescale USA), which was presented at the 40th International Symposium for Testing and Failure Analysis (ISTFA), November 9-13, 2014 (Houston, TX).*

**Table 1** Summary of investigations performed on the various products studied

		Case 1	Case 2	Case 3
<b>Failure mode</b>		Parametric leakage	Electrical functional	Parametric leakage
<b>Defect signature</b>		Pipeline defect	Pipeline defect	Silicon dislocation
<b>Impacted device type</b>		NMOS	NMOS	NMOS
<b>FA techniques</b>	<b>TLS</b>	X	X	...
	<b>Photoemission</b>	X	...	X
	<b>AFP</b>	...	X	...
	<b>PVC</b>	X	...	...
	<b>Silicon delineation etch</b>	X	X	...
	<b>SCM/SMM</b>	...	X	X
	<b>Planar TEM</b>	...	X	X

(ESD) structures and single embedded analog transistors inside a block circuit. The commonality in the three cases is that the defective device type is always the same: an NMOS structure.

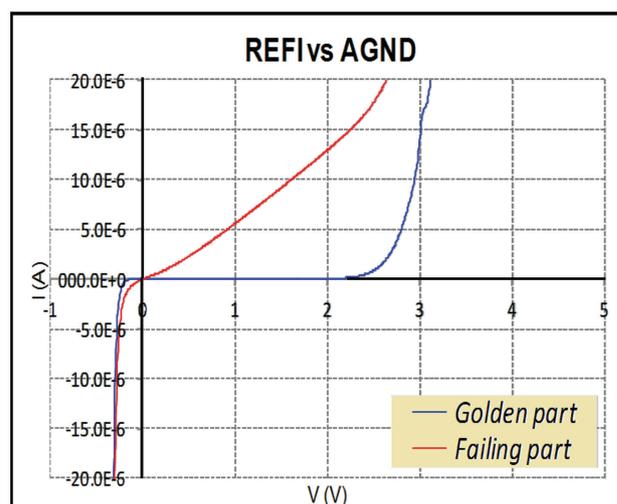
All the products presented failed at ambient temperature. In case 1, the failure was observed between two external pins, REFI and GND, with a leakage of approximately  $2.6 \mu\text{A}$  at 2 V, compared to a few nanoamps on a “good” part (Fig. 1a). In case 2, the failure was due to an offset of 30 mV on the current-sensing circuit of channel 2, generating a functional failure. Microprobing analysis demonstrated that the failure was due to a drain-source leakage of the Mf2 (used in the current-measuring chain) NMOS transistor within the output comparator circuit (Fig. 1b). Based on those results, case 1 was opened from the backside, and the silicon substrate was thinned.

Thermal laser stimulation was carried out by applying 1 V between REFI and GND. In this case, the position of the optical beam induced resistance change (OBIRCH) spot was located within the ESD structure of the pad and especially in a specific area of the NMOS transistor (Fig. 2a). TLS was applied from the frontside in case 2, between the source and drain of this NMOS (Mf2 transistor). The OBIRCH signature was located on one of the four NMOS fingers (Fig. 2b). In both cases, the OBIRCH signatures were located on the NMOS transistor.

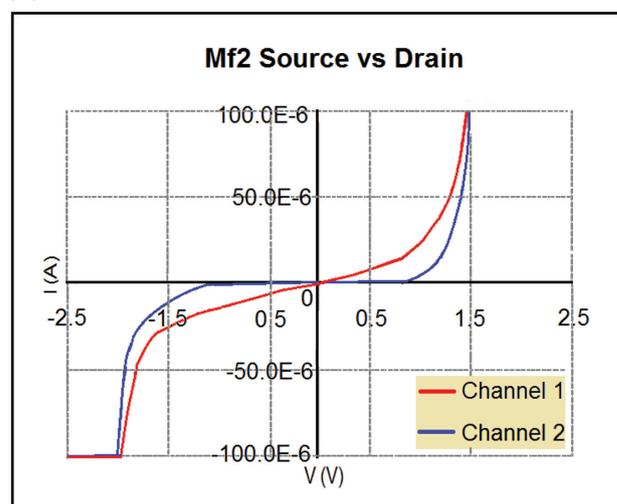
## COMPARATIVE STUDY: EMMI/OBIRCH/InGaAs CAMERA

An experimental study was done in case 1. Leakage was initially detected by using TLS ( $1 \text{ V}/7 \mu\text{A}$ /integration time = 10 s). The aim of this study was to understand what type of defect can be detected by the cameras and to determine the detection threshold of silicon charge coupled device (Si-CCD) or InGaAs cameras. The voltage/current was then

increased until the camera could detect the emission of photons (Table 2). For a voltage below 2 V, the integration



(a)



(b)

**Fig. 1** (a) Parametric leakage characteristic of case 1. (b) Functional failure. Leakage found by microprobing on failing Mf2 NMOS device in case 2

time for the Si-CCD camera was approximately a few minutes, but for a voltage below 1.6 V, the integration time for the InGaAs camera was approximately 30 s (Fig. 3a). The hotspot was visible starting at 1.6 V for the InGaAs camera and at 2 V for the Si-CCD camera (Fig. 3b), confirming Planck's radiation law depends on wavelength camera sensitivity (explained in Ref 6). This experiment confirms that both emission cameras are suitable for silicon defects, with no difference in terms of spectrum emission but with higher sensitivity for the InGaAs camera. When compared to TLS, it is an alternative to photoemission, and TLS has the advantage of selecting the failing path and injecting voltage or current by microprobing.

## ATOMIC FORCE PROBING

Atomic force probing measurements were done in case 2, where the Mf2 NMOS transistor was found to be leaky. This NMOS transistor comprises four fingers. By measuring the subthreshold current of each finger (measurement done by increasing and decreasing the voltage), it was observed that three of the four fingers were leaky (Fig. 4). Finger 3 had normal leakage and was located between two leaky fingers. Despite identifying three leaky fingers, the OBIRCH signature pinpointed the defect only on finger 2. This interesting result was confirmed in other parts, suggesting that the TLS or emission techniques revealed only

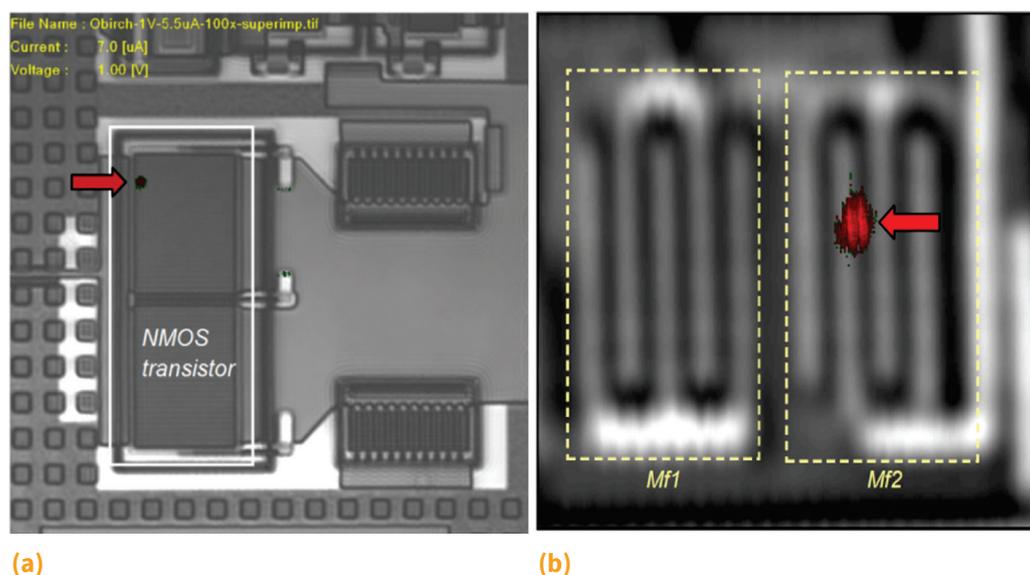


Fig. 2 (a) TLS localization in case 1, within the ESD structure, based on NMOS device. (b) TLS overlay with pattern showing the OBIRCH signature observed on Mf2 NMOS device by microprobing

Table 2 Experimental study of Si-CCD and InGaAs camera detection capability

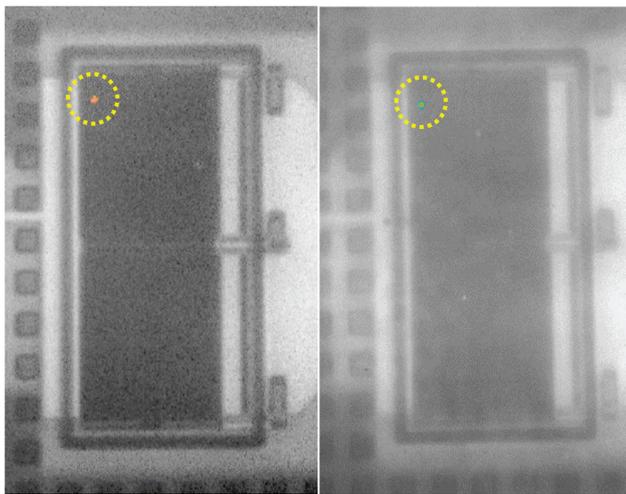
Voltage/current applied	Si-CCD camera detection	InGaAs camera detection		
1 V/5.5 $\mu$ A	No defect detected			
1.1 V/6.24 $\mu$ A				
1.2 V/6.95 $\mu$ A				
1.3 V/7.68 $\mu$ A				
1.4 V/8.14 $\mu$ A				
1.5 V/9.13 $\mu$ A				
1.6 V/9.87 $\mu$ A			Defect detected	
1.7 V/10.63 $\mu$ A				
1.8 V/11.38 $\mu$ A			Defect detected	
1.9 V/12.14 $\mu$ A				
2 V/12.91 $\mu$ A				
2.1 V/13.69 $\mu$ A				
2.2 V/14.47 $\mu$ A				

the leakiest patterns, and the defect can extend further than the TLS/photoemission analysis.

## PHYSICAL INVESTIGATIONS

### PASSIVE VOLTAGE CONTRAST AT CONTACT LEVEL

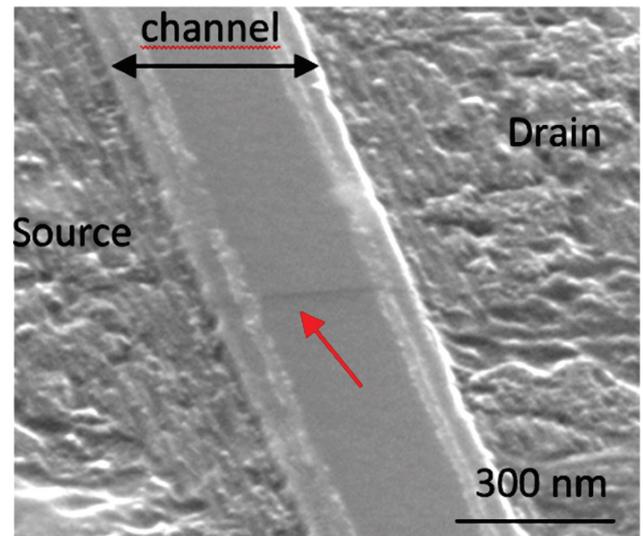
Based on the electrical FA findings obtained in case 1, a step-by-step deprocessing was performed to inspect the metal layers; no anomaly was observed. At contact/ILD0 level, passive voltage contrast (PVC) was executed using SEM, confirming that the NMOS polysilicon gate was properly insulated from the active area. Because the metal layer and polysilicon gate were not involved in the NMOS device leakage, it is most likely that a defect at the silicon level was responsible for the failure.



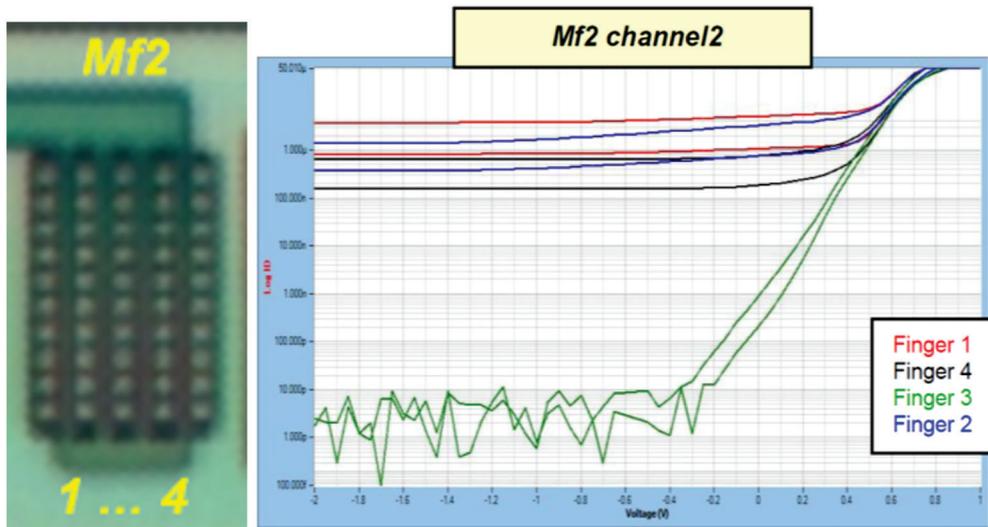
**Fig. 3** Emission localization. (a) Si-CCD camera (>2 V). (b) InGaAs-CCD camera (>1.6 V)

## SILICON ACTIVE AREA SEM INSPECTION AND PVC

Deprocessing was done by removing the polysilicon and gate oxide layers to expose active silicon for SEM inspection. No silicon damage (indicative of ESD damage) was observed, and no wafer fab defect (such as micro-masking or a silicon topography issue) was identified. Low-acceleration-voltage PVC was performed to provide different contrast imaging between differently doped regions.<sup>[7]</sup> A narrow, straight dark line was observed at the NMOS channel area. This hairline passed across all the NMOS channels, and its position and configuration (parallel to one side of the device structure) exactly matched the OBIRCH signature (Fig. 5). In the PVC images, the *n*-type region is darker than the *p*-type area; the observed dark



**Fig. 5** Tilted SEM image at silicon active area level with PVC revealing abnormal dark line in channel region



**Fig. 4** AFP measurement on NMOS in case 2

hairline is suspected to be unexpected  $n$ -doped silicon at the surface of the  $p$ -doped channel. The PVC images were obtained using high-resolution SEM with sample tilt and beam deceleration mode (consisting of the application of a positive voltage to the sample holder). This configuration is highly recommended to detect pipeline defects by improving the collection of secondary electrons.

## SILICON CRYSTALLINE DELINEATION ETCH

To verify the PVC contrast at the silicon substrate level, a silicon delineation etch was performed with Wright etch solution;<sup>[8]</sup> the  $p$ -type etch rate is higher than the  $n$ -type area etch rate<sup>[9]</sup> with this delineation etch. After etching with Wright solution for 2 s, the failing NMOS device was inspected with an SEM; a bump was observed at the dark line location previously observed on the PVC image (Fig. 6). This topographic anomaly is consistent with the hypothesis of an abnormal presence of an  $n$ -type area in the NMOS channel ( $p$ -doped). This unexpected  $n$ -doped area crossing the whole channel width explained the NMOS source-to-drain leakage. In addition to its dopant delineation capability, Wright etch is also widely used to delineate silicon crystalline defects, creating typical etch pit signatures. Those etch pits were observed at the edges of the abnormal silicon bump and revealed the dopant anomaly associated with a crystalline defect<sup>[2]</sup> (circled in yellow in Fig. 6). To confirm and better understand this complex defect, more investigations were performed with advanced FA techniques.

## AFM/SMM TECHNIQUE

A part from case 2 was selected to continue the analysis on the pipeline signature. Surface topography measurements using AFM did not reveal a conclusive anomaly at

the silicon level (Fig. 7). However, SMM analysis showed an anomalous line contrast in the dC/dV response image, which typically provides information about the doping levels. The dark lines observed through the channels of Mf2 (red arrows in Fig. 7) indicate an unexpected doping response in the channel active area. These results were consistent with physical delineation etches that gave similar pipeline results (see Fig. 6 from the part in case 1). In contrast, the same technique was applied on the failing device in case 3, where silicon dislocations were found by physical delineation etch and TEM analysis (refer to the next section). In this case, SMM was not able to highlight a defect signature (Fig. 8); this suggested that the nature of the defect is different. Presumably, the threshold conductivity of free carriers is not in the detection range of SMM as compared to a pipeline defect, even if the defect is considered to be conducting.

## PLANAR TEM ANALYSIS

Based on previous findings, TEM characterization was required. Planar TEM samples were prepared on the defective parts of each product. In case 2 (with pipeline), TEM images showed crystallographic defects in active areas, at the vicinity of the anomalous lines observed during SMM analysis (Fig. 9). The crystalline defects were noncontinuous lines that were only localized in gate areas. The defects were perpendicular to source-drain fingers and appeared to be very close to the surface. Also, continuous lines were observed in the trench area (shallow trench isolation), nearly in the extension of the discontinuous lines (far left in Fig. 9). In this case, it was found to be a pipeline defect in the active area. In case 3, TEM images also showed crystallographic defects in the active areas. However, the defects were long, continuous lines

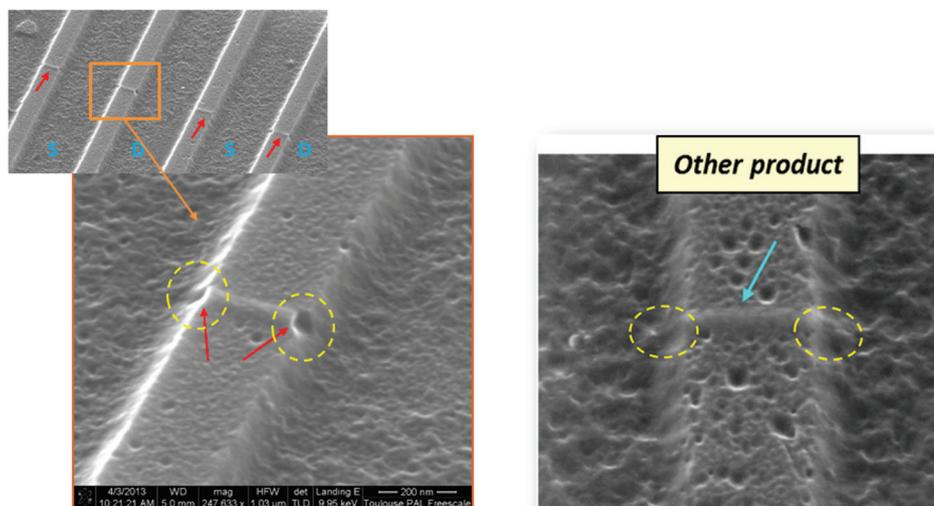
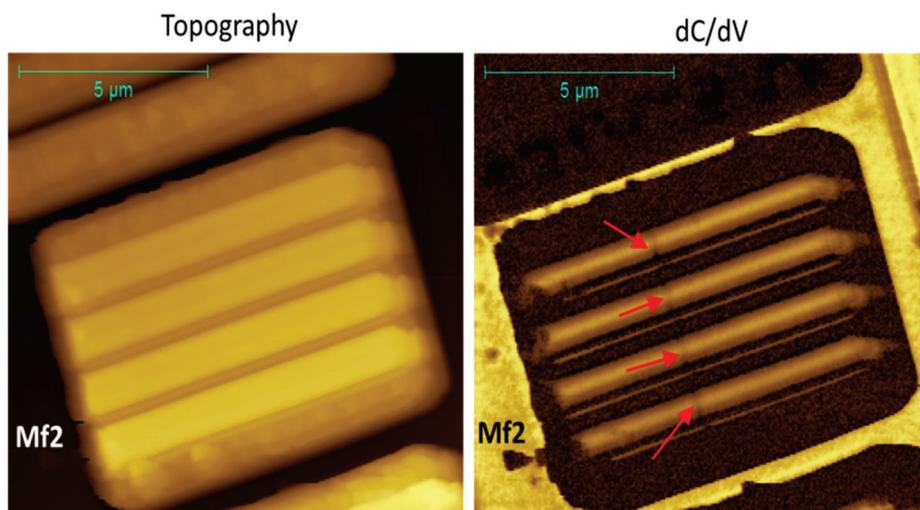


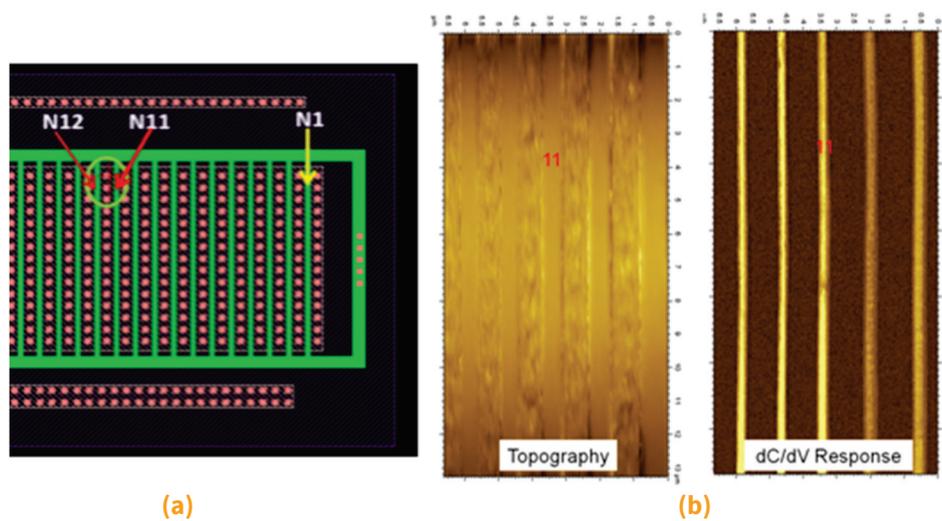
Fig. 6 Tilted SEM image after Wright etch delineation on different product

(several microns long) in the active area, perpendicular to the source-drain fingers (Fig. 10). In case 3, it is suspected to be a dislocation. By comparing TEM signatures

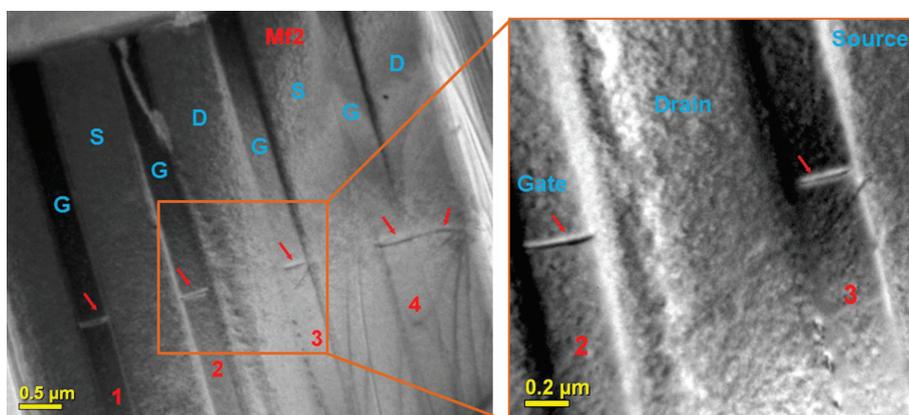
of pipeline and silicon dislocations, it was not possible to make an obvious distinction between these two different signatures by TEM analysis alone. However, TEM analysis



**Fig. 7** AFM/SMM characterization of “pipeline” silicon defect impacting two neighbor transistors and crossing the full active area in a part from case 2. No conclusive anomaly is visible in the topography image; however, the dark line is indicated with red arrows in the dC/dV response image.



**Fig. 8** AFM/SMM characterization of silicon dislocation crossing the full active area in case 3. (a) Localization of failure in device. (b) AFM and SMM characterization. No anomaly in the topography or dC/dV response images



**Fig. 9** TEM images of pipeline defect fingers for case 2

is useful in determining the real size and shape of the physical defect in silicon.<sup>[10]</sup>

## DISCUSSION: PIPELINE OR DISLOCATION

### PIPELINE AND DISLOCATION PHYSICAL DISTINCTIONS

The complementary electrical and physical analyses performed in this work demonstrated that the defects can be imaged, but their natural differentiation is more difficult to identify:

- There is no distinction possible in terms of electrical failure (similar failure mode, current leakage level, etc.).
- There is no distinction of TLS or EMMI signature (spot signature, sensitivity, etc.).

However, based on multiple case studies, the following approaches could be used to distinguish pipeline defects and dislocations. First, PVC at the silicon level using SEM can highlight pipeline defects. Based on the physical behavior of a free carrier introduced by phosphorus implanted in the channel, it is possible to generate PVC at the pipeline. As a result, the SEM electron beam formed a picture with a contrast variation in the defective area. It is believed that this phenomenon is either not possible on a dislocation, or the dopant concentration in the dislocation core is not sufficient to produce PVC in the SEM, allowing their natural differentiation. In addition, another concern is the depth of the defect; it is commonly accepted that dislocations are found in subsurface regions compared to pipelines, which are normally located at the surface of the channel. Therefore, PVC is more effective in localizing pipeline defects.

Crystal delineation etching using Wright etch solution is an interesting complementary analysis to PVC in the SEM. Typically, the pipeline defect appears as a three-dimensional bump (relief) in the channel, whereas the

dislocation creates an overetched line area, as a cavity (Fig. 11). While this method offers another way to differentiate pipeline and dislocations, this approach suffers from the following limitations:

- If the defect is located a few nanometers from the surface of the active area, etching can consume the defect.
- If the defect is located in the substrate volume, it could be difficult to define the correct etching time to expose it.

Furthermore, the problems of reproducibility in the etching process can easily destroy the defect. Alternatively, nondestructive dopant profiling techniques (SMM or scanning capacitance microscopy, or SCM) can be used on a single defective unit to improve analysis success. The surface-level capacitance change due to a pipeline defect is activated by phosphorus atoms (*n*-type) by creating an inversion line in the channel; it produces a line contrast in the dC/dV response image. However, it was demonstrated that the dislocation did not produce such dC/dV contrast, possibly because of the depth location of the dislocation or a too-low concentration of active dopant. This point was not studied in this work and is considered a prospect for future work.

Planar TEM analysis offers the best solution for determining the size and shape of both pipeline and dislocation defects. Unfortunately, it is not easy to distinguish between pipeline and dislocation because of similar physical signatures on TEM images. Advanced transmission electron microscopes equipped with high-spatial-resolution electron energy-loss spectrometry capability may be an option for detecting phosphorus atoms in the pipeline.

Based on the multiple experiments presented, a methodology for analyzing those failures is proposed:

- *When several parts are available:* The best practice should be to first perform Wright etch delineation

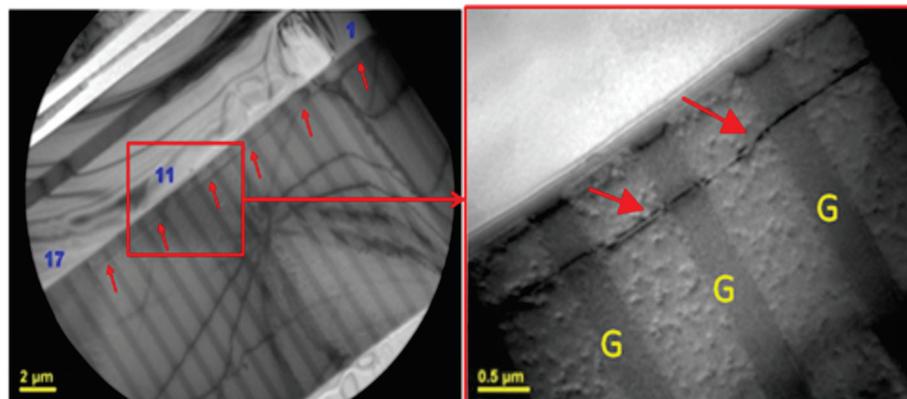


Fig. 10 TEM images of dislocation in silicon in case 3. The gates are indicated by the letter “G.”

(knowing that it can destroy the defect) at the silicon level. Then, planar TEM can finalize the study of a different part to confirm the nature of the silicon defect.

- *When only one part is available:* The FA strategy should be different. The analysis can start by SEM PVC at the silicon level to make a first distinction; it should be positive in the pipeline case. Then, AFM-based dopant profiling techniques should be employed to detect surface-level anomalies. Depending on the sample state after SMM, planar TEM can be used to localize and image the defect.

## HYPOTHESIS OF PIPELINE VERSUS DISLOCATION FORMATION

As demonstrated, pipeline silicon defects are observed in NMOS transistors and are generated by the formation of “diffusion pipes” at an active area channel surface under certain process conditions, causing leakages between implanted drain and source regions. The origin of the defect formation is not completely understood. Based on the literature,<sup>[11]</sup> reported hypotheses concerning the formation of pipeline defects include potential stress generated during sidewall mask isolation etch at island corners, implant-induced silicon damage, possible physical correlation between a type of etch pit pairs, and some design/mechanical considerations on isolation trench walls. Despite these different aspects, it is well known that the main solution for improving yield is to use suitable furnace recrystallization steps to eliminate this type of defect.

A hypothesis is proposed that defines a link between dislocation and pipeline defects. It is possible that dislocations are the first step in the silicon substrate defect, which can evolve into a pipeline defect under various particular process conditions, depending on wafer fab processing, deep-trench pattern design, process aspect (annealing,

implantation, surface oxidation), and so on.<sup>[12]</sup> In other words, pipeline defects can either be the same type of dislocations formed on the surface, or they can be formed through dislocations pinning at the surface region.

## CONCLUSIONS

Depending on the choice of FA techniques, the distinction between a dislocation and a pipeline defect in NMOS transistors can be very difficult. Electrical investigations through fault localization techniques are useful in determining the impacted device and its localization. Atomic force probing enables further localization of the defective device. However, no distinction between a pipeline and a dislocation was observed during the electrical characterizations. Nevertheless, physical investigations with a combination of SEM PVC at the silicon level, Wright etch delineation, nondestructive dopant profiling techniques, and TEM techniques could be used to distinguish a pipeline defect from a dislocation. Proper classification, based on interpretation of the physical signature observed through the various methods, will determine the appropriate corrective actions in wafer fab manufacturing, thus allowing continuous improvement.

## ACKNOWLEDGMENT

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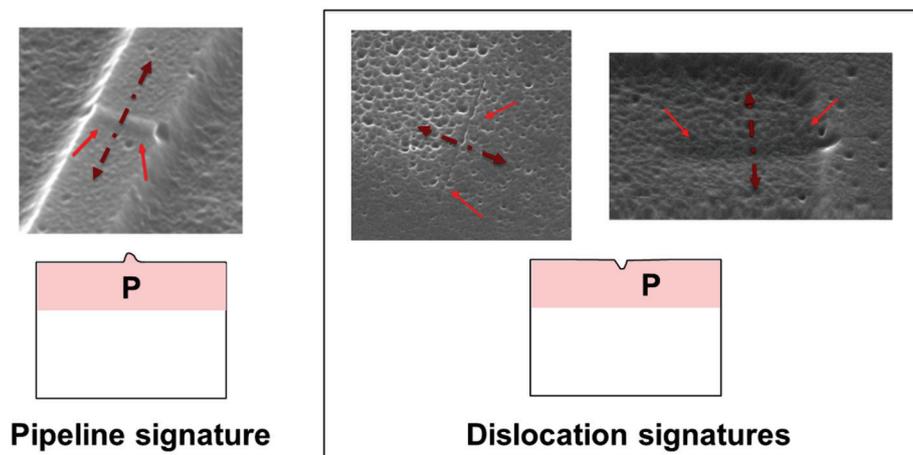


Fig. 11 Schematic cross-sectional views of silicon pipeline defect in relief compared to dislocation in silicon

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## ABOUT THE AUTHOR



**Yann Weber** received his M.S. degree in electrical engineering in 2004 from Polytechnic Orsay France and his second M.S. degree in nanostructures and microsystems for electronics from Paris Sud Orsay University the same year. He started his professional career by completing a Ph.D. under the public laboratory collaboration of Freescale and the Laboratory for Analysis and Architecture of Systems/French National Center for Scientific Research at Toulouse, where he developed alternative structures in semiconductor power VDMOS devices to increase breakdown voltage and on resistance. He graduated in 2008 and received honorific distinction from the "Académie des Chiffres et Belles Lettres" of

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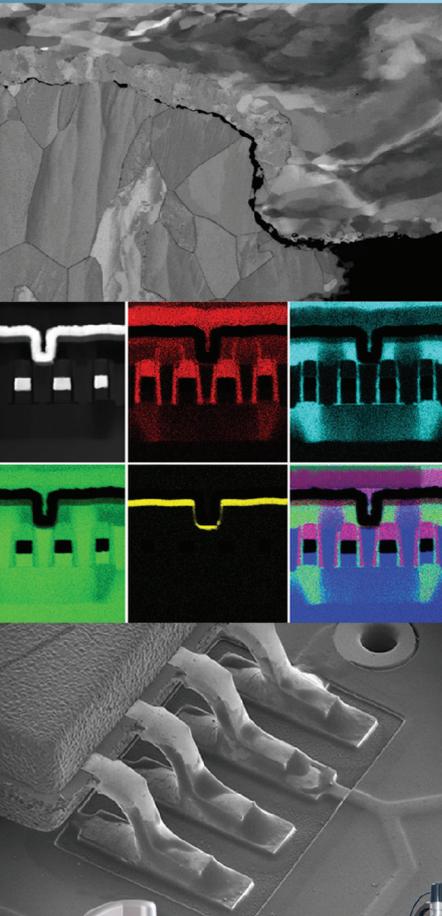
## NOTEWORTHY NEWS

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The ninth annual FIB/SEM Workshop will be held on Thursday, **February 25, 2016**, at the Kossiakoff Center at Johns Hopkins Applied Physics Laboratory in Laurel, Md. It features a full day of presentations and posters by FIB users and vendors highlighting interesting new FIB applications and the latest technology. As always, there will be plenty of opportunities for informal discussion of new techniques and applications as well as time for (re)connecting with fellow FIBers. There is no fee to attend the meeting, and breakfast and lunch are provided. **Registration deadline is February 19.**

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# 3-D ANALYSIS OF A COPPER FLIP-CHIP INTERCONNECTION USING FIB-SEM SLICE AND VIEW

Mototaka Ito and Jun Kato, Toray Research Center  
Mototaka\_Ito@trc.toray.co.jp

Recently, flip-chip assembly has become mainstream for fine-pitch interconnection in large-scale integration packages. Gold studs and copper pillars with solder caps are two types of bumps in common use.<sup>[1]</sup> Gold stud bumps are commonly used for interconnecting dice with peripheral layouts. Gold-gold bonding has the advantage of a low process temperature, and gold-solder with adhesive has good wettability of the joint without flux.

The use of copper pillar with a solder cap has the advantage of gang fine-pitch bumping by wafer plating. Increases in the number of bumps, narrowing of pitch, and cost pressures have driven the adoption of copper pillar/solder cap bumping in high-performance mobile devices. Copper pillar bumps on the die are interconnected to the copper pad on the substrate in a solder reflow process. The use of thermal compression bonding (TCB) and preapplied underfill for fine-pitch interconnection is growing due to its precise alignment of bump and pad and the minimization of global stress on the assembly. Concerns with the technology, however, include entrapment of adhesive components and voids in the joint due to solder shrinkage.

## FIB-SEM FOR FLIP-CHIP JOINT ANALYSIS

Three-dimensional (3-D) analysis techniques can be used to study copper pillar bump joints. X-ray computed tomography (CT) is one major 3-D analytical method, but its spatial resolution is currently limited to the submicron level. The slice-and-view method using a focused ion beam-secondary electron microscope (FIB-SEM) has high spatial resolution on a nanometer level, which makes it superior to x-ray CT.<sup>[2]</sup> This method has already been used to investigate the inner wiring of a semiconductor device. The authors used the method to evaluate the solder joint and what appeared to be preapplied underfill between a copper pillar bump and a copper trace on a substrate.

The authors removed a memory and application processor (AP) packaged in a package-on-package (PoP) from a commercial tablet personal computer (PC). First,

mechanical polishing was used to expose the structure of the PoP, and then the microbump interconnecting the AP to the copper wiring on the package substrate was located. The authors then made a 3-D observation by the slice-and-view method using an FIB-SEM equipped with a dual-electron beam. An SEM image was taken every 200 nm of etching by FIB, for a total of 240 SEM images. Then, 3-D images were reconstructed using these SEM still images.

The authors also investigated the composition distribution of the solder joint area by electron probe x-ray microanalysis (EPMA). To observe thermal changes in the bumps, another sample of the PoP was subjected to a thermal cycle test (TCT) of 1000 cycles from -55 to 125 °C with a 1 h cycle.

## COPPER PILLAR JOINT ANALYSIS RESULTS

A cross-sectional microscopic image of the flip-chip bump interconnection of the AP die prepared by

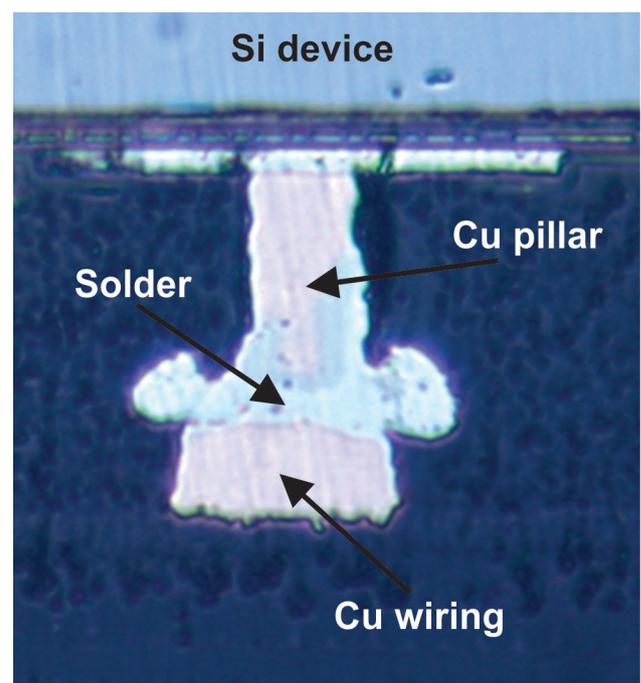
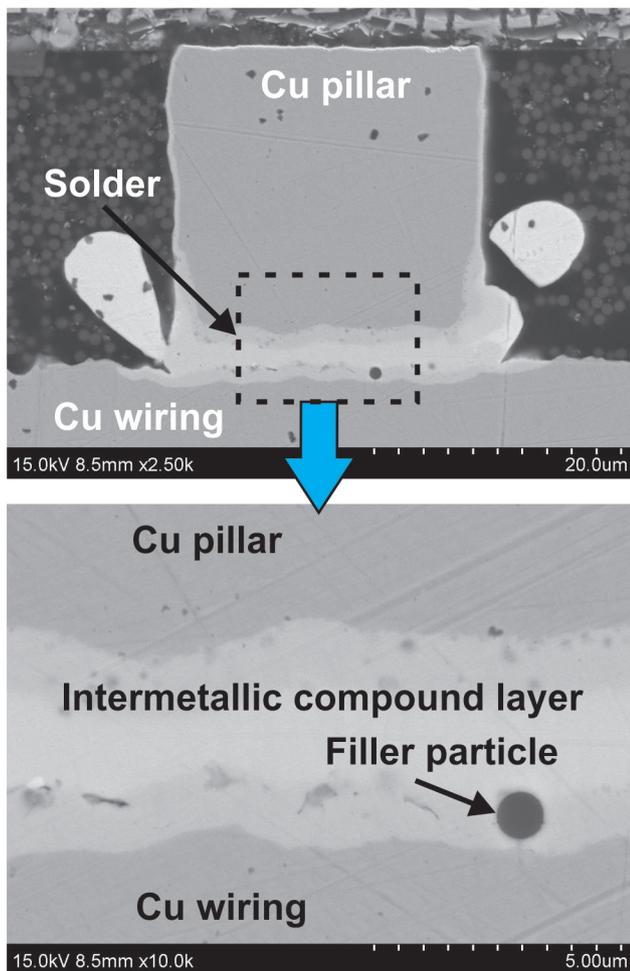


Fig. 1 Cross-sectional micrograph of the flip-chip joint

**“THE USE OF COPPER PILLAR WITH A SOLDER CAP HAS THE ADVANTAGE OF GANG FINE-PITCH BUMPING BY WAFER PLATING. INCREASES IN THE NUMBER OF BUMPS, NARROWING OF PITCH, AND COST PRESSURES HAVE DRIVEN THE ADOPTION OF COPPER PILLAR/SOLDER CAP BUMPING IN HIGH-PERFORMANCE MOBILE DEVICES.”**



mechanical polishing is shown in Fig. 1. It seems that the copper pillar was bonded to the copper wiring on the substrate by TCB using a preapplied underfill. Figure 2 shows higher-magnification images taken by SEM. An entrapped filler particle from the preapplied underfill is visible in the solder joint area.



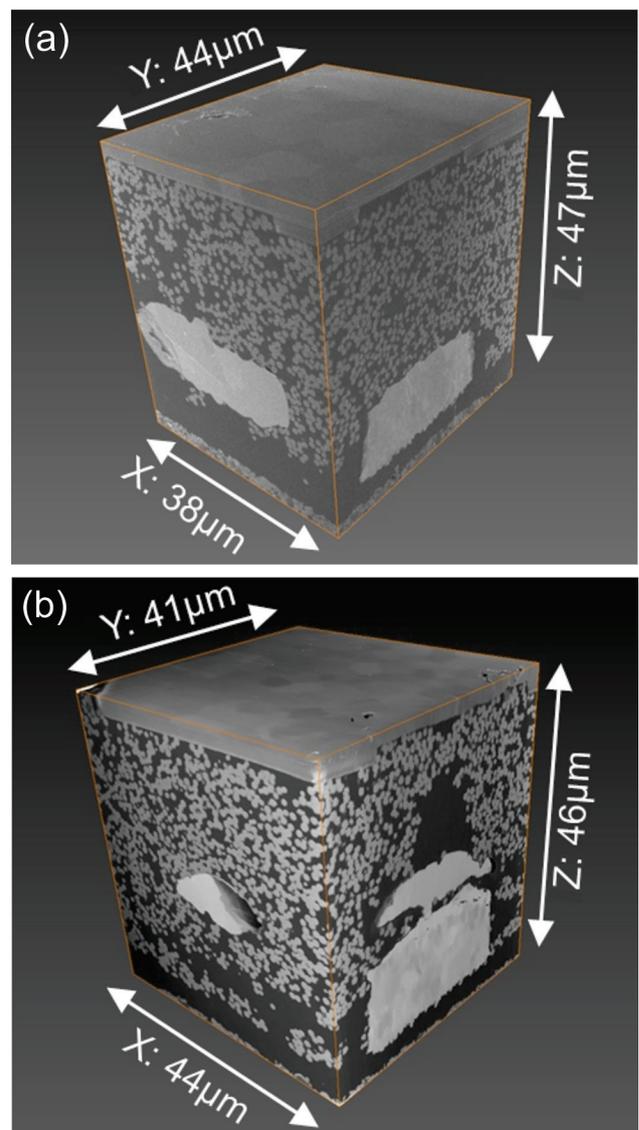
**Fig. 2** Cross-sectional SEM images of the flip-chip joint

## 3-D TOMOGRAPHIC RECONSTRUCTION

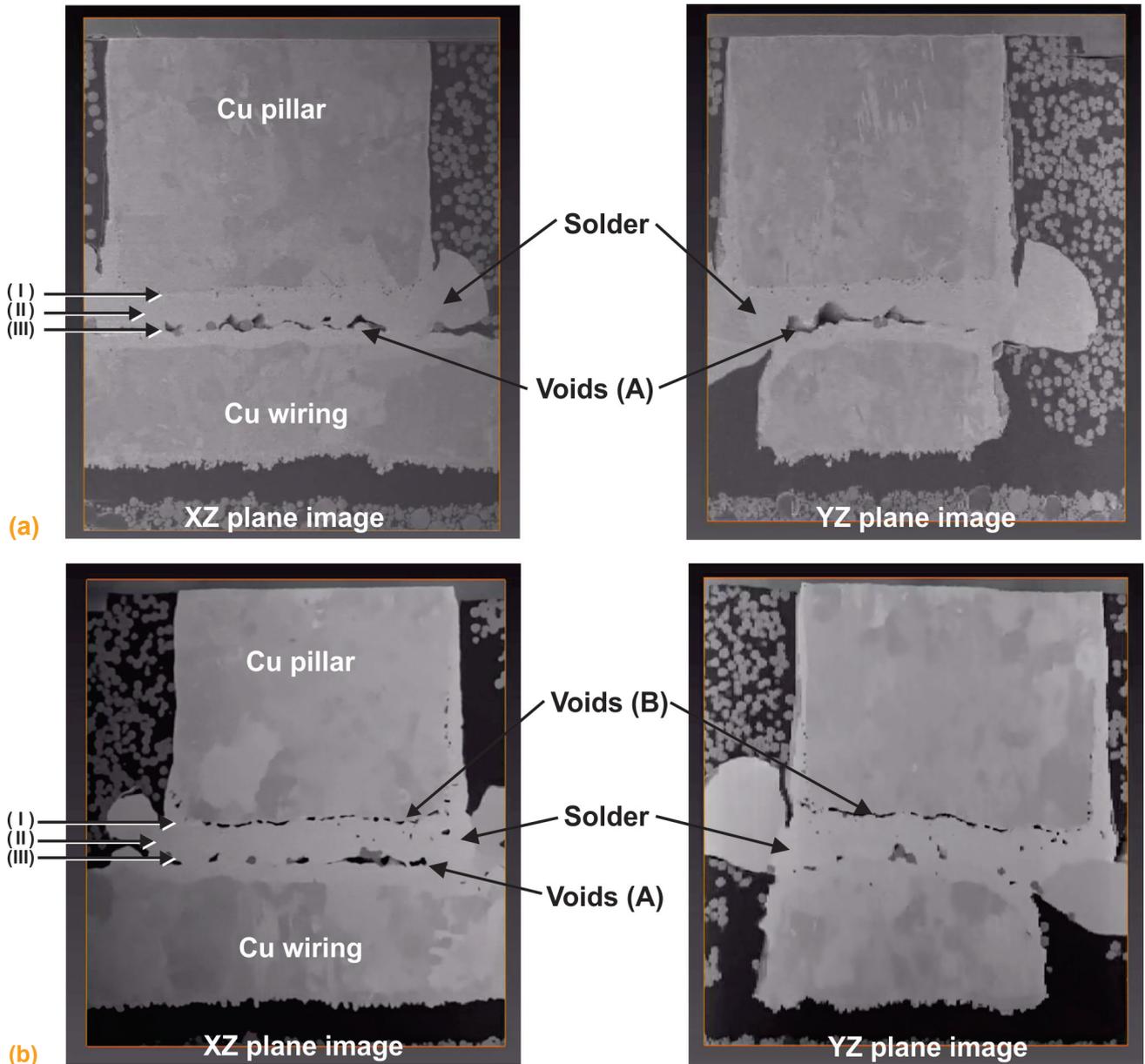
Figure 3 shows 3-D reconstructed images of the joint before and after TCT. The volume of the reconstructed space of the joint before TCT is  $38 \times 44 \times 47 \mu\text{m}^3$ , and the volume after TCT is  $44 \times 41 \times 46 \mu\text{m}^3$ . Tomographic images of the XZ- and YZ-planes of the bump center are shown in Fig. 4.

The XY-plane is parallel to the substrate plane. The X-axis is parallel to the copper trace on the substrate, and the Y-axis is perpendicular to it. The authors observed large voids, shown in Fig. 4(a) and (b) as “Voids (A).” The authors believe these were generated by solder shrinkage.<sup>[3]</sup>

The authors subjected another sample of the same package to the previously mentioned TCT and then performed 3-D SEM analysis of the solder joint. Another type of void at the interface of the copper pillar and the



**Fig. 3** Three-dimensional reconstructed images of the flip-chip joint. (a) Before TCT. (b) After TCT



**Fig. 4** Tomographic images of the XZ- and YZ-planes in the center of the copper pillar. (a) Before TCT. (b) After TCT ( $-55\text{ }^{\circ}\text{C}/125\text{ }^{\circ}\text{C}$ , 30 min/30 min, 1000 cycles)

intermetallic compound (IMC) was clearly visible. These are indicated as “Voids (B)” in Fig. 4(b).

## ANALYSIS OF XY-PLANE SLICES

Figure 5 shows XY-plane tomographic images of the solder joints of the packages without TCT (Fig. 5a to c) and with TCT (Fig. 5d to f). The images were extracted at three different Z-heights:

- Figures 5(a) and (d), at level I (shown by arrow I in Fig. 4), are slice views of the copper pillar and IMC interface.
- Figures 5(b) and (e), at level II (shown by arrow II in Fig. 4), are slice views of the IMC layer.

- Figures 5(c) and (f), at level III (shown by arrow III in Fig. 4), are slice views at the level of the shrinkage voids.

Comparison of the two level-I views (Fig. 5a and d) shows that the copper pillar and IMC interface changed significantly with TCT treatment: although only small voids are observed prior to TCT, numerous large voids appear after TCT. At level II, very few voids were detected in the IMC layer either before or after TCT. At level III, numerous shrinkage voids and entrapped filler particles from the preapplied underfill are observed. In addition, the authors were able to observe the 3-D distribution of filler in the underfill, as well as gaps between the copper pillar and the adhesive.

*(continued on page 18)*

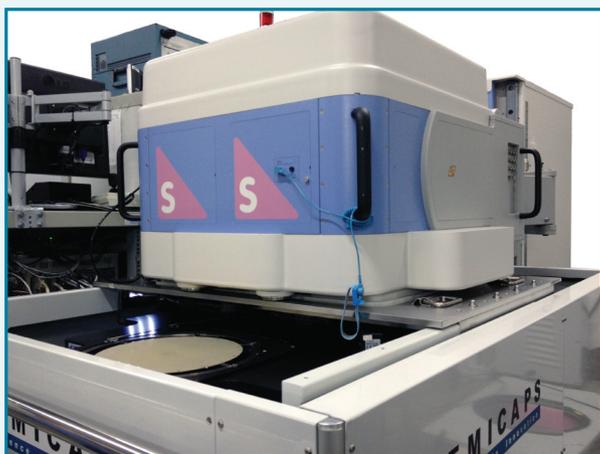
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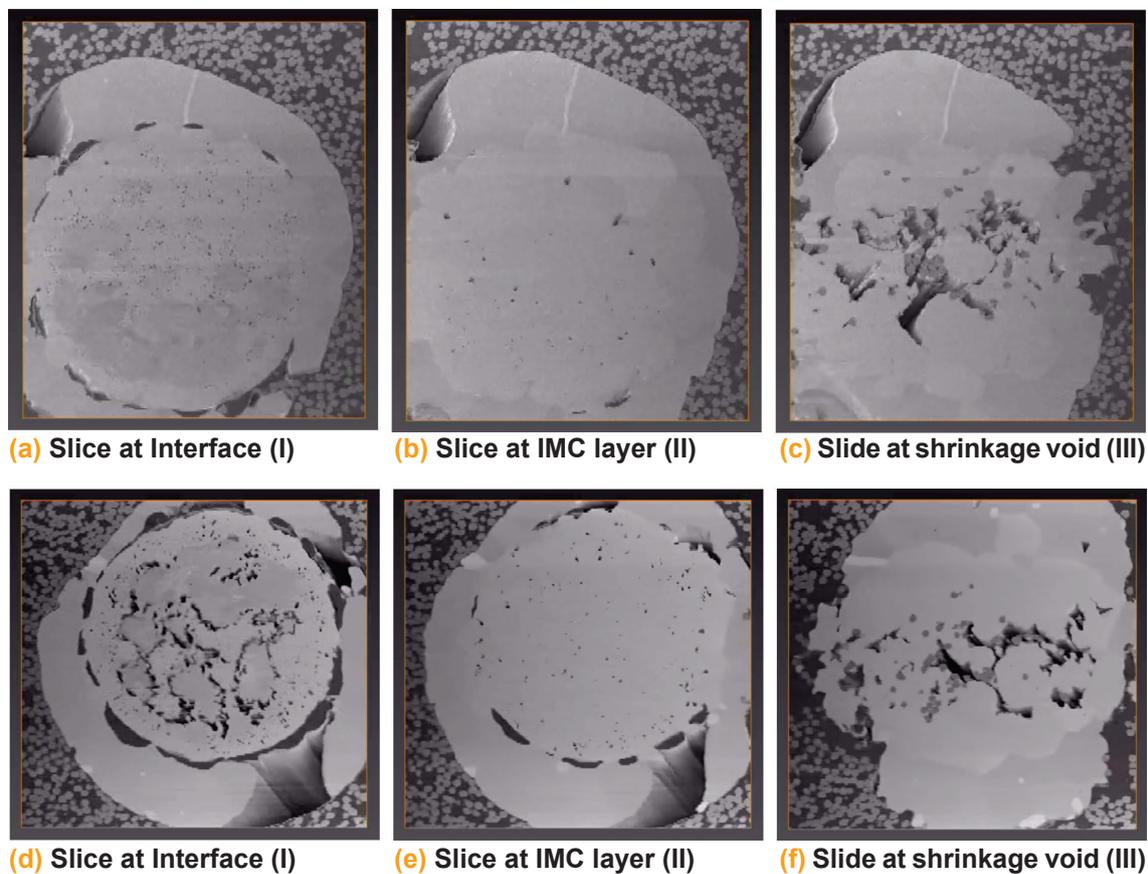
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### 3-D ANALYSIS OF A COPPER FLIP-CHIP INTERCONNECTION *(continued from page 16)*



**Fig. 5** Tomographic images in the XY-plane of the interface between copper pillar and IMC layer. (a) to (c) Before TCT. (d) to (f) After TCT

## DISCUSSION OF VOID FORMATION MECHANISM

The mechanism of void formation at the interface between the copper pillar and IMC layer that occurs during TCT is discussed below.

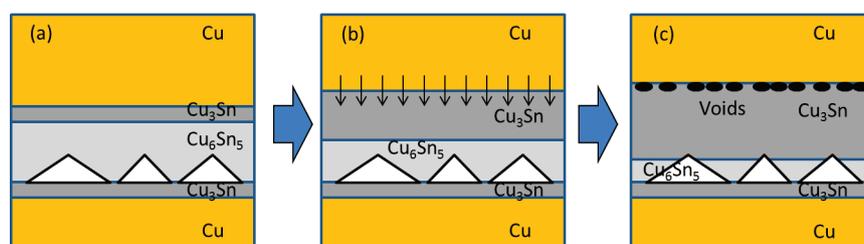
### KIRKENDALL EFFECT

The Kirkendall effect, which describes the formation of voids at the interface of different metals due to differences in the metals' thermal diffusivity, is well known.<sup>[3,4]</sup> In a copper/tin system, as shown in Fig. 6, a  $\text{Cu}_3\text{Sn}$  IMC layer can easily grow, which creates the

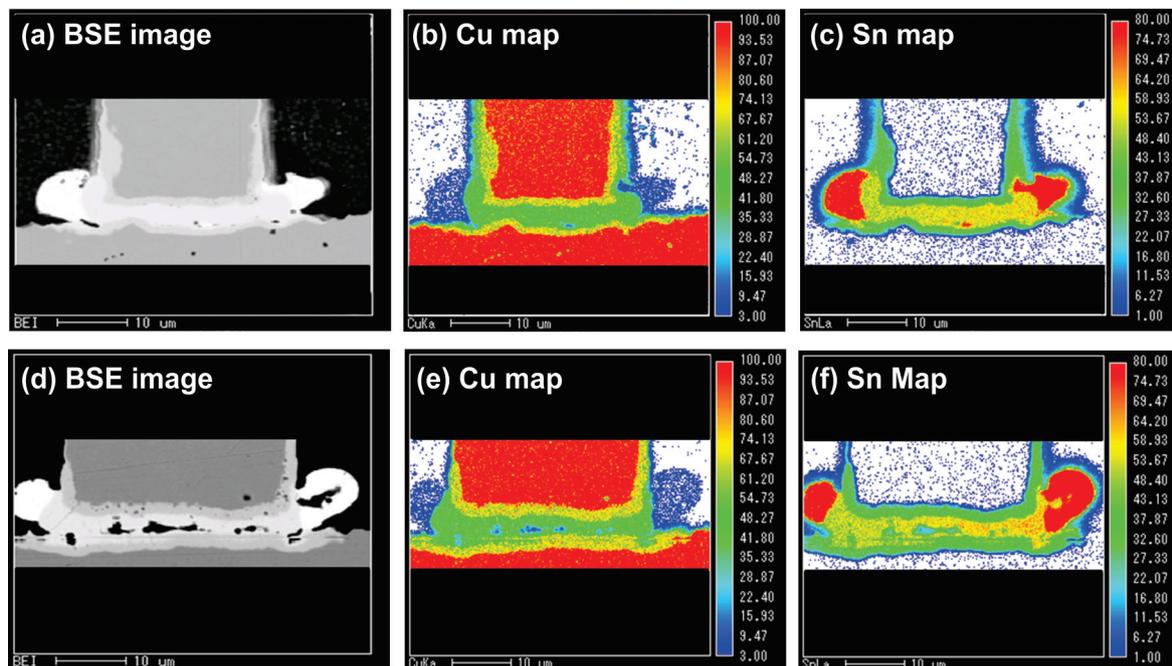
Kirkendall effect. The EPMA mapping results of the IMC layer in the authors' system are shown in Fig. 7. Because there is not much growth of the  $\text{Cu}_3\text{Sn}$  layer, it does not appear that the large-volume voids shown in Fig. 5(d) were formed by the Kirkendall effect. This is supported by the fact that no such voids were observed at the interface of the substrate copper and the IMC.

### GAS EXHAUST PHENOMENON AND SOLID-PHASE DIFFUSION

Studies have shown that volatile constituents inside a plated copper film can move during soldering processes, which can lead to void formation in the solder.<sup>[5]</sup>



**Fig. 6** Mechanism of void formation in the system of copper diffusion model. (a) Before TCT. (b) Growth of  $\text{Cu}_3\text{Sn}$ . (c) Kirkendall voids formation



**Fig. 7** EPMA mapping of solder joint on flip-chip. (a) to (c) Before TCT. (d) to (f) After TCT. BSE, backscattered electron

Void formation based on this gas exhaust phenomenon is illustrated in Fig. 8. A copper pillar is formed by microplating with a certain aspect ratio, whereas the copper trace on the substrate is formed from dense electrolytic copper foil. Volatile constituents in the copper pillar are released as gas during the TCT by interface reaction with the solder.

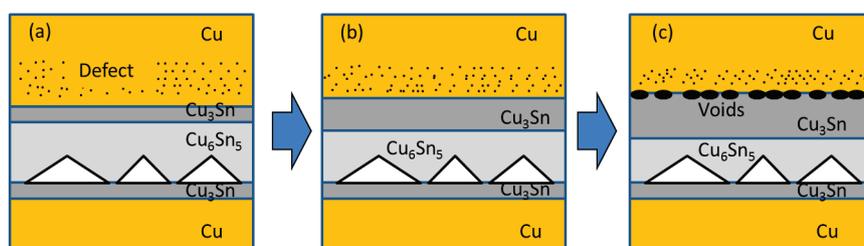
## SUMMARY

The authors used 3-D SEM analysis to investigate the flip-chip bump interconnection of an AP taken from a commercial tablet PC. The analysis technology is based on the repetition of FIB etching and SEM image capture. Three-dimensional views were reconstructed from 240 SEM images that were taken after repeated FIB etching at 200 nm intervals. The authors believe the interconnection to be a copper pillar with a solder cap connected to a copper trace on the substrate by thermal compression bonding with a preapplied underfill. Our analysis showed that

the interconnection joint in the AP as received included filler entrapment and many voids. With this method, the generation of a number of voids was clearly observed at the interface of the pillar copper and the IMC after 1000 cycles of TCT between  $-55$  and  $125$  °C.

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**Fig. 8** Mechanism of void formation in the system of gas exhaust model in solid-phase diffusion. (a) Before TCT. (b) Slight growth in  $\text{Cu}_3\text{Sn}$ . (c) Void formation by accumulation of defects

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**Mototaka Ito** joined Toray Research Center in 1991, where he conducted analysis of semiconductors and various industrial materials using Auger electron spectroscopy. He is currently engaged in the 3-D FIB-SEM analysis of semiconductor package interconnections and the investigation of thermally induced deformation in large-scale integration packages. Dr. Ito received a master's degree from Nagaoka University of Technology and a doctorate from Osaka University, where he studied diffusion phenomenon in the interface between SnAgX solder and electroless Au-NiP plating.

**Jun Kato** has been engaged in electron microscopy for over 20 years and has worked extensively in the analysis of materials in semiconductor devices and other advanced materials. Most recently, he has specialized in FIB. He is currently in charge of FIB/SEM analysis at Toray Research Center.



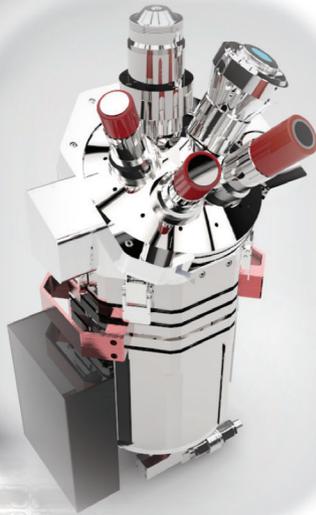
## NOTEWORTHY NEWS

### ENGINEERING EXCELLENCE AWARD WINNER

The Optical Society named the Logic Analysis Tool (LAT) team as the winner of the 2015 Paul F. Forman Team Engineering Excellence Award. The research team was formed in response to a call from the Intelligence Advanced Research Program Activity (IARPA) for innovative solutions to circuit analysis. The team developed an optics-based LAT that detects the time-resolved emission of light from switching transistors within integrated circuits (ICs) operating down to 0.5 V, thus creating a new tool for device analysis in advanced process technologies. The group, led by Dr. Euan Ramsay of DCG Systems, was comprised of the following:

- **The DCG Systems team** (Euan Ramsay, Herve Deslandes, Tom Kujawa, Ted Lundquist, and Benjamin Cain) was responsible for the construction of a system to measure the spectrum of light emitted by leaking and switching transistors so that the wavelength range of the final optical system and detectors could be defined. On the basis of these measurements, DCG also developed the optics for collecting the emitted light and bringing it to the Photon Spot fiber for time-resolved emission measurements from ICs. DCG performed the assembly and initial testing of all subsystems into one integrated tool. The final prototype configuration allowed diffraction-limited performance over a broad spectral range with a numerical aperture of more than 2.5.
- **The MIT team** (Karl Berggren, Kristen Sunter, and Faraz Najafi) designed and fabricated superconducting nanowire single-photon detectors, delivering high gain, low jitter, and low noise, for the required time-resolved measurements of the emission from switching transistors. These detectors were optimized in wavelength based on the measurements made by IBM and incorporated several novel features.
- **The Photon Spot team** (Vikas Anant, Brian Ma, and Juying Shang) developed a closed-cycle cryostat to cool the superconducting detectors to 800 mK. They also designed a low-jitter electronic interface between the fiber delivery system from the output port of the tool to the superconducting detector and the DCG Systems electronics and software.
- **The IBM team** (Peilin Song, Franco Stellari, Andrea Baghat-Shehata, Seongwon Kim, Herschel Ainspan, Christian Baks, Alan Weger, and Ulrike Kindereit) used the spectral measurement system to determine the emission spectrum trend from 45 and 32 nm process technologies at various operating voltages. IBM developed a unique test chip with features stretching the design rules for prototype characterization and performed the qualification of the various versions of the prototype tool, including on various 22 and 14 nm test chips (10 nm chips are yet to be available) using proprietary IBM test technologies. Final testing was carried out by the IBM team.

## Extended Wavelength IREM-IV Photon Emission Microscope

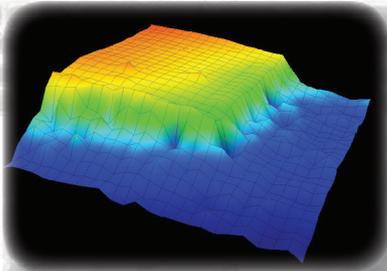


Demonstrated sensitivity at 0.4V<sub>dd</sub>  
on 14 nm Tri-gate and FinFET devices:

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- 5-position motorized lens turret
- 1016 X 1016 pixel image
- 800 – 2500 nm responsivity
- Dual internal cooled filter wheels
- Motorized sample tilt table

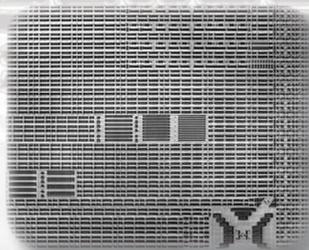
### NEW! LASER SURFACE PROBE

Measure device tilt and profile



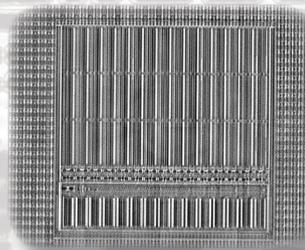
### HIGHEST RESOLUTION

3.3 NA SIL Objective



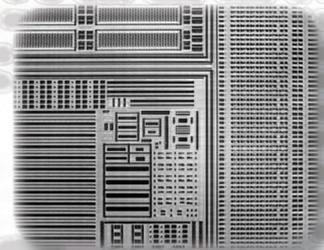
### MOST SENSITIVE

22nm Tri-Gate Device



### LARGEST FIELD OF VIEW

Custom Optics



# WIRE BONDING

Lee Levine, Process Solutions Consulting, Inc.  
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The dominant process for interconnecting semiconductor chips to the outside world is an ultrasonic welding process called wire bonding. More than 90% of the chip interconnections produced annually (more than 15 trillion wires) are produced with this process. Welding is a process where an intermetallic alloy is formed from the materials to be joined. Generally, intermetallic alloys are stronger and also more brittle than their constituents. Welding is superior to other joining methods such as soldering, which requires that a low-melting-temperature material melt and solidify within the joint. Low-melting-temperature materials such as solders have significantly lower strength and are more subject to creep and fatigue failures than intermetallics. There are two major variations of the wire bonding process: ball bonding and wedge bonding. Ball bonding is the larger portion, with approximately 90% of the entire wire bonding market. The fastest ball bonders can bond more than 20 wires/second compared to less than 10 wires/second for wedge bonding. Ball bonding also has more advanced capabilities than wedge bonding. However, ball bonding is limited to wires below approximately 50  $\mu\text{m}$  in diameter. All interconnections that require larger-diameter wire are produced by wedge bonding aluminum or copper, using either round wire or ribbon (a flattened form of round wire).

During the past 5 years there has been a major transition in our industry from ball bonding with gold wire to the use of copper, palladium-coated copper, or silver wire. This year will be the first year where market share for gold wire falls below 50%. Cost, yield, and reliability have all played a major part in this transition. In 2009, when gold rose in price above \$1000/troy ounce and remained there, gold reduction became a mandate in semiconductor packaging. Gold wire represented a large portion of the gold used in semiconductor packaging. Copper had been discussed<sup>[1]</sup> and demonstrated since the early 1980s but had not been widely adopted. Copper was more difficult to bond and had package reliability issues. As these issues (optimum bond pad metallization, encapsulation chemistry for long-term reliability, bonder recipe improvements) were resolved, the transition became a stampede and in 5

years became a new paradigm. Silver is also less expensive than gold. Silver is used for bonding light-emitting diode devices because it has better reflectivity properties than either copper or gold. Early problems with silver wire in 85 °C/85% relative humidity testing were resolved using silver-palladium alloy wire. Silver market share is now approaching 10%.

Figure 1 is a photo of the bond head with capillary, wire, and electronic flame-off (EFO) wand. In ball bonding, the tip of a fine-diameter metallic wire (protruding from the capillary) is melted by a spark from the EFO. Surface tension in the metallic liquid pulls the liquid into a sphere; the sphere solidifies, with more than 80% of the heat transferring back into the wire. This leaves a short region above the ball, called the heat-affected zone (HAZ), that has been rapidly heated to just below the melting temperature and then cooled rapidly to near room temperature. The HAZ is the weakest portion of the wire. The bond head, with capillary and ball dangling below it, descends at high speed toward the surface (normally the bond pad on a die). At a programmed height above the surface, the bond pad velocity transitions to a slower, constant velocity, and the bonder begins searching for the surface (surface height can vary due to the many tolerances from material and prior operations). Surface detection can occur by a number of methods, including mechanically opening a contact spring, as in older machines, or high-speed sensing of a current rise in a voice coil motor when the coil stalls on contact. After contact detection, the bond head continues downward to apply a programmable force on the ball. Ultrasonic energy from a piezoelectric transducer is added for a programmable time (8 to 12 ms is typical for a high-speed ball bonder). The die and substrate are normally heated to 125 to 200 °C, depending on the process and materials. These four factors—ultrasonic energy, bond force, heat, and time—constitute the principal variables for ultrasonic weld formation.

After completing the ball bond cycle, the bond head rises and a series of very precise coordinated motions occur, forming a loop between the ball bond and the second bond. Loop height and uniformity are very

important packaging requirements. The demand for thin and stacked-dice packages that are as thin as possible led to the development of improved bond head control algorithms and many new loop shape options. Memory devices often have their bond pads located down the center of the die surface rather than around their periphery. This allows better signal and voltage distribution and results in faster devices that command premium values. Figure 2(a) is a photo of low loop wires for memory. These loops rise to a low height and then travel parallel to the edge of the die, where they descend to the second bond. Stacked-dice packages (Fig. 2b) often employ a hybrid bond called a stand-off stitch (SOS). In an SOS bond, a ball is formed and bonded with the wire intentionally broken in the HAZ. Another ball is formed and bonded to the substrate side of the package. The stitch (second bond) side of the wire is then bonded on top of the original ball. Because it requires the formation of three bonds rather than two, the SOS bond is approximately 40% slower than a standard bond, but it provides the lowest loop height available. Every smart phone (more than 1 billion annually) has at least one stacked-dice package. Stacked dice, because each die can

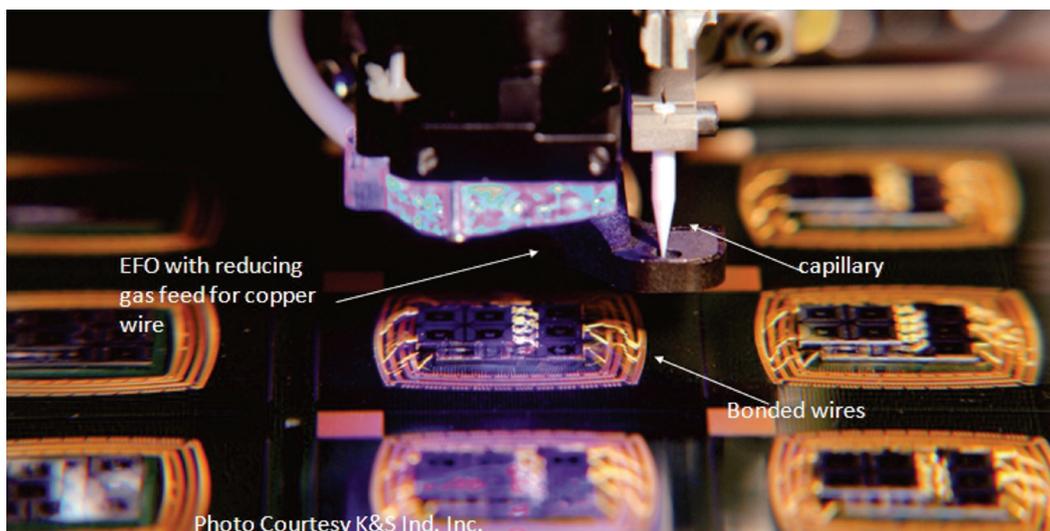
contain a separate technology (analog, digital, memory, radio frequency), enable integration of the entire system within the package. Earlier attempts to integrate all of these technologies on the same chip proved costly and decreased reliability. Joining the technologies by stacking them within the package became the dominant method.

The second bond is formed by a different portion of the capillary tip than the ball bond. Figure 3 is an illustration of a capillary tip and the portions of the tip that produce the ball bond, the loop, and the second bond. In forming the second bond, the capillary face and outer radius are pressed on the top of a round wire. The combination of ultrasonic energy, bond force, heat, and time deform the round wire into the fishtail shape and form the initial intermetallic bond.

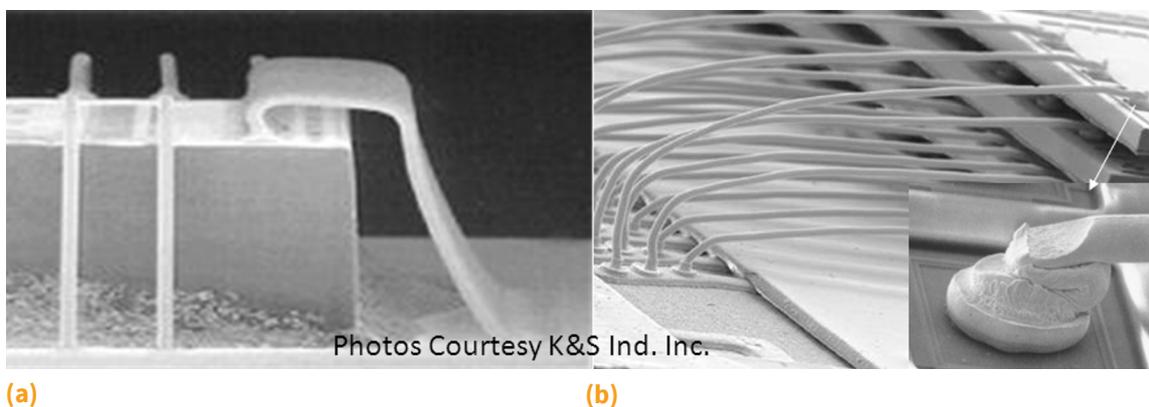
The mechanical and other materials properties of the ball and the wire are significantly different. The second bond is more diffusion-controlled than the ball bond.

## WIRE BOND FAILURE MECHANISMS

Semiconductor packages must normally pass a battery

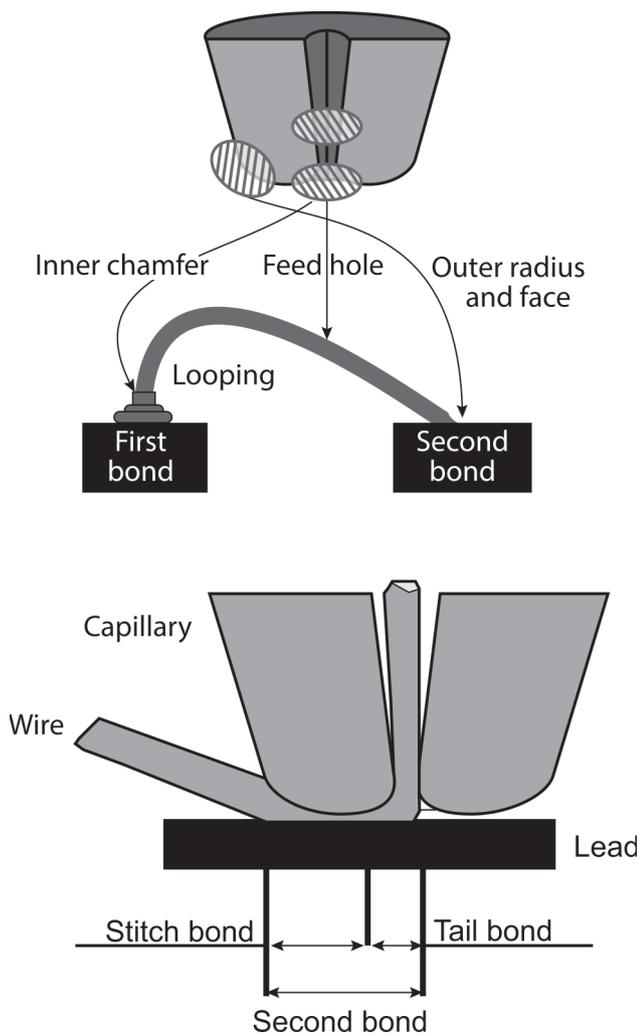


**Fig. 1** Wire bonding bond head for copper wire. Courtesy of Kulicke & Soffa Industries Inc.



**Fig. 2** (a) Worked loop. (b) Stand-off stitch loop. Courtesy of Kulicke & Soffa Industries Inc.

of short- and long-term reliability testing during package qualification prior to market introduction. Once manufacturing and sales begin, mechanical testing is commonly done on each material lot. Mechanical testing normally consists of both wire bond pull testing and shear testing. Because the weld areas for both the ball bond and the second bond are several times larger in cross section than the wire cross section, the pull test is not capable of testing the strength of either bond (the wire breaks first). However, it is capable of detecting very poor bonds, wire damage, damage to the HAZ, or a second bond that has been overdeformed and has a thin cross section at the heel of the bond. The pull test measurement can be understood from a simple resolution of forces. However, once a history of data exists and statistical process control has been established, the use of control charts can be a very powerful quality tool. The shear test is capable of measuring ball bond strength and should be a standard test for each lot. Average shear strength of 5.5 g/mil<sup>2</sup> (85 MPa) meets the JESD-22-B116A standard for shear testing required by the automotive industry.



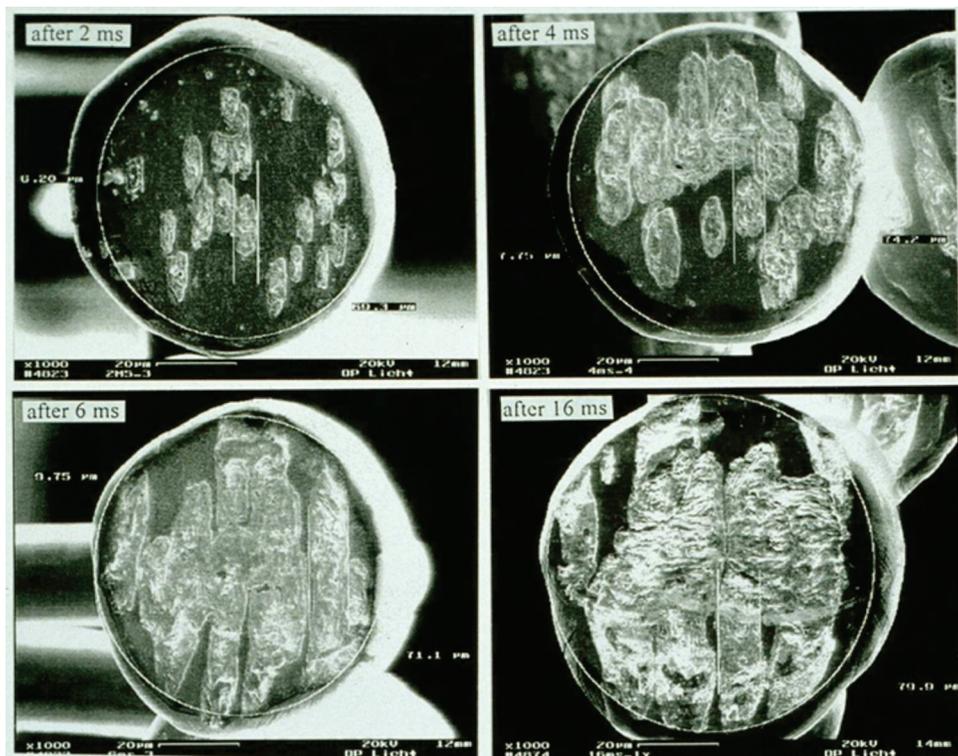
**Fig. 3** Capillary tip showing features that effect portions of the bond

The life and subsequent failure of gold ball bonds on aluminum bond pads by Kirkendall voiding has been well documented. At temperatures above 150 °C for some packages, this can occur quickly and catastrophically. Bonds literally fall off with almost no stress. New 99.9% gold alloy wires (standard gold bonding wire is 99.99% gold) with additional impurities added to stabilize intermetallic formation can improve reliability. Gold ball bonds on gold bond pads in high-temperature environments do not exhibit the problem.

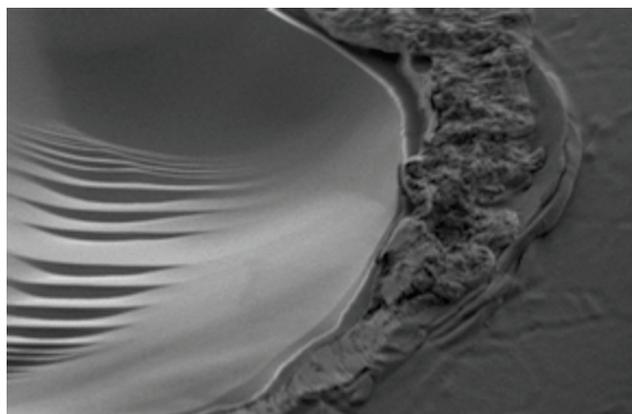
Analysis of intermetallic coverage and morphology should be a standard part of qualification testing and should be repeated periodically through the life of a product. Aluminum bond pads can be easily etched with sodium hydroxide or potassium hydroxide to release the bonded balls. Etching will not remove the intermetallic on the bottom of the balls. The balls can be flipped with a dental pick, or the die paddle tie bars can be removed to reveal the bottom side of the balls. Intermetallic coverage should exceed 80% as bonded. Figure 4 demonstrates the evolution of bond coverage as a function of bonding time. After 16 ms bond time, the intermetallic coverage is over 80%. To expose the bonds in encapsulated packages, it is often necessary to remove the encapsulating material with hot, fuming nitric acid. This will reveal gold ball bonds but will immediately attack copper bonds. Several techniques, such as laser ablation and very controlled etching in an inert atmosphere, have been used for copper ball bonds.

Copper-aluminum intermetallic requires both a higher formation temperature and longer time (slower growth rate) than gold-aluminum. Therefore, copper ball bonds can be more reliable than gold bonds at high temperature. Encapsulation to protect copper bonds is critical. The presence of Cl<sup>-</sup> ions is autocatalytic to copper. Chlorine corrodes copper and then is released to continue corrosion. Molding compounds that contain less than 30 ppm chlorine and have a controlled pH of 4 to 6 are now available for copper and are necessary for high-reliability products.<sup>[2]</sup>

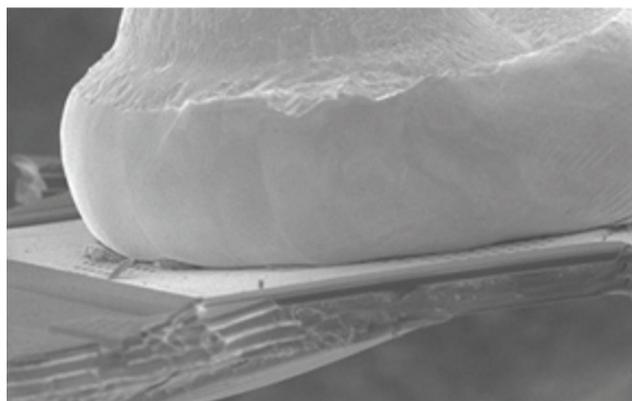
Figure 5 shows scanning electron microscopy images of two failure modes that can occur as a result of wire bonding. Normally, ultrasonic energy is the most aggressive variable affecting bond pad failures, but poor design of the bond pads is also a root cause. Designed-in reliability resulting from careful design of experiments and the development of internal design guidelines focused on the use of robust bond pad structures cannot be ignored. Modern bond pads often contain multilevel stacks of metal and dielectric layers. In some cases, low-k dielectrics with poor mechanical stability are required for functionality.



**Fig. 4** Thermosonic (120 kHz) ball etch-off patterns showing weld-growth formation. Courtesy of ESEC (now BESI North America)



(a)



(b)

**Fig. 5** (a) Fracture of silicon die below bond. (b) Fracture of multilevel bond pad

Instances of failures in layers below the surface, allowing electromigration and eventually resulting in interlayer shorts, are well documented. Often these failures can occur while the top metal layers and wire bond are unaffected.<sup>[3]</sup> They are difficult to detect and analyze. A team approach, involving fab, assembly, and reliability engineers, must focus on the development of pad structures that not only can achieve electrical design requirements but are robust enough to withstand manufacturing and reliability.

## CONCLUSION

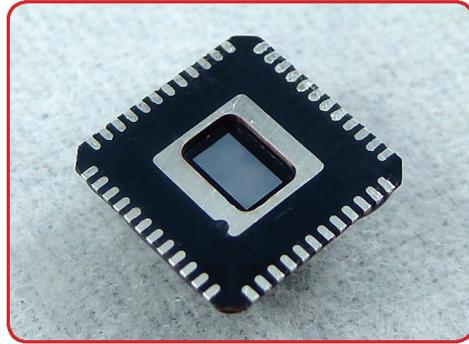
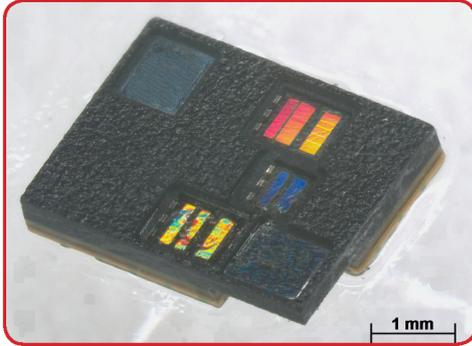
Wire bonding continues to be the lowest-cost, highest-reliability, most flexible semiconductor interconnection method. It continues to reinvent itself; as new demands are understood, machine, wire, tool, and end users come together to find solutions that enable successful implementation of the new requirements. Each new generation of devices has required increased capabilities for both manufacturing and metrology. Wire bonding has met these challenges and added the capabilities necessary for its continued growth as the leading semiconductor interconnection method.

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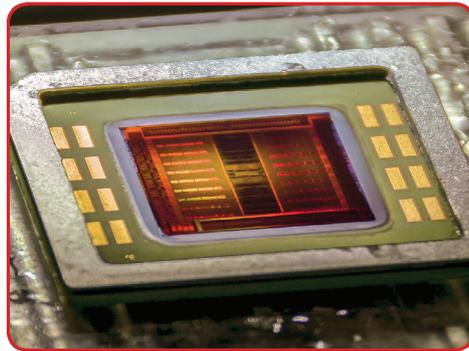
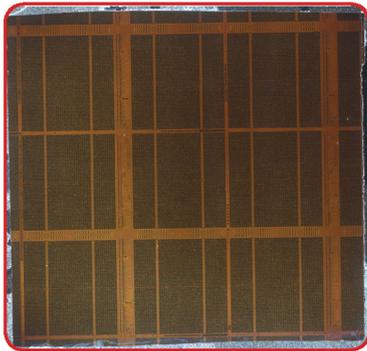
(continued on page 28)

## Small Device Preparation



- Open areas as small as  $100 \times 100 \mu\text{m}$

## Ultra Thinning

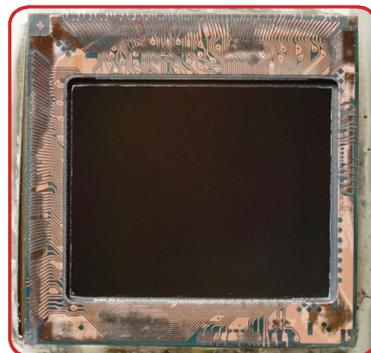


- Uniform silicon thinning to less than  $2 \mu\text{m}$

## Complex Device & Stacked Die Deprocessing



- TSV exposure



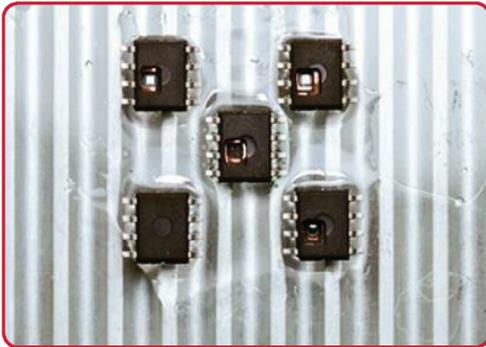
- Targeted stacked die exposure

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## WIRE BONDING *(continued from page 25)*

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## ABOUT THE AUTHOR



**Lee Levine's** previous experience includes 20 years as Principal and Staff Metallurgical Process Engineer at Kulicke & Soffa Industries Inc. and Distinguished Member of the Technical Staff at Agere Systems. Currently he runs his own business, Process Solutions Consulting, Inc., where he consults on packaging reliability, wire bonding, and provides scanning electron microscopy/energy-dispersive spectroscopy and metallography services. He has been awarded four patents and has published more than 70 technical papers. His awards include both the 1999 John A. Wagnon Technical Achievement award and the 2012 Daniel Hughes award for technical achievements from the International Microelectronics Assembly and Packaging Society (IMAPS). Major innovations include copper ball bonding, loop shapes for thin, small outline packages (thin-shrink small outline packages and chip-scale packages), and introduction of design of experiments and statistical techniques for understanding assembly processes. He is an IMAPS Fellow and a senior member of IEEE. Lee previously was IMAPS Vice President of Technology. ■



# EDFAS BOARD OF DIRECTORS

## 2016 ELECTION—CALL FOR NOMINATIONS

Jeremy Walraven, Chair, EDFAS Nominating Committee  
Past President, EDFAS  
jawalra@sandia.gov

**E**DFAS is soliciting nominations for candidates for the EDFAS Board of Directors. Nominations are for member-at-large Board positions for four-year terms beginning September 1, 2016, through August 31, 2020. There are expected to be up to five positions open for nomination, and any members of EDFAS in good standing are encouraged to nominate themselves or another member for one of these positions. The incumbents may also seek re-election by notifying the Nominations Chair, Jeremy Walraven (jawalra@sandia.gov).

Nominations are due March 1, 2016. Candidates who initiate or accept nomination will be asked to provide a three-page nomination package that includes the candidate's:

- Academic/business biography
- EDFAS and ISTFA involvement
- Photograph and contact information
- Failure analysis background
- Vision for the future of EDFAS

Nomination packages should be sent to Joanne Miller at 9639 Kinsman Rd., Materials Park, OH 44073-0002 or joanne.miller@asminternational.org. For more information or questions, call 440.338.5151, ext. 5513.

These nominations will be posted on the EDFAS website and published in the May issue of *EDFA* magazine. Voting will be electronic and open to all EDFAS members. Voting will take place in June 2016, with the winners invited to join the Board for the September 2016 teleconference.

Service on the EDFAS Board of Directors involves planning and driving the future strategy of your society. The Board of Directors meets between quarterly and monthly by conference call, and face-to-face meetings at least once a year at ISTFA. Board members also provide liaison support to the several EDFAS committees, which may involve a few additional conference calls.

Candidates are encouraged to ensure that they have the support of their employer for this activity. ■

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# PLASMA FIB PROVIDES VITAL DELAYERING AND SITE-SPECIFIC FAILURE ANALYSIS CAPABILITIES FOR LARGER-SCALE STRUCTURES

Surendra Madala, FEI  
Surendra.madala@fei.com

The plasma focused ion beam (PFIB) differs from the conventional FIB in its use of a xenon plasma-based ion source instead of the gallium liquid metal ion source. The PFIB can generate ion beams with much higher current and therefore is able to remove larger volumes of material at much faster rates while still maintaining precise control of the beam and its milling action. PFIBs can deliver beam currents ranging from 1.5 pA to  $>1 \mu\text{A}$ , with milling rates some 20 to 100 times higher than a gallium beam due to the much higher maximum beam current achieved by the inductively coupled plasma source, leading to new applications in delayering/deprocessing and site-specific failure analysis.

## CROSS SECTIONING COPPER-FILLED TSVs

One of the first PFIB applications was cross sectioning copper-filled through-silicon vias (TSVs).<sup>[1,2]</sup> The large dimensions of TSVs require the removal of a little more than a million  $\mu\text{m}^3$  to create  $100 \times 100 \mu\text{m}^2$  cross sections. The PFIB milling rates can accomplish the task in a reasonable time. Figure 1 shows an example of a cross section of a 50- $\mu\text{m}$ -diameter  $\times$  150- $\mu\text{m}$ -deep copper-filled TSV.

## PACKAGE-LEVEL CIRCUIT MODIFICATIONS

PFIB systems have now been used successfully to create prototypes that incorporate package-level modifications.<sup>[3]</sup> Making design changes and creating new prototypes typically takes one to two weeks. PFIB technology can make modifications in less than a day, significantly shortening the design and test cycle.

In some cases, packaging structures are large enough ( $>100 \mu\text{m}$ ) to permit modifications with laser-based systems;<sup>[3]</sup> however, advanced packaging processes now coming into production frequently use signal traces in the middle range (10 to  $100 \mu\text{m}$ )—too big for conventional FIB modification and too small for lasers. PFIB permits modifications of these advanced package circuit elements within a practical time frame and with none of the thermal- or debris-associated issues of laser processing. Figure 2 shows an example of a prototype created by temporarily relocating gold bond wires to access copper traces below. Note the cutting of adjacent traces and rerouting of the signal with cuts, connections, and insulation.

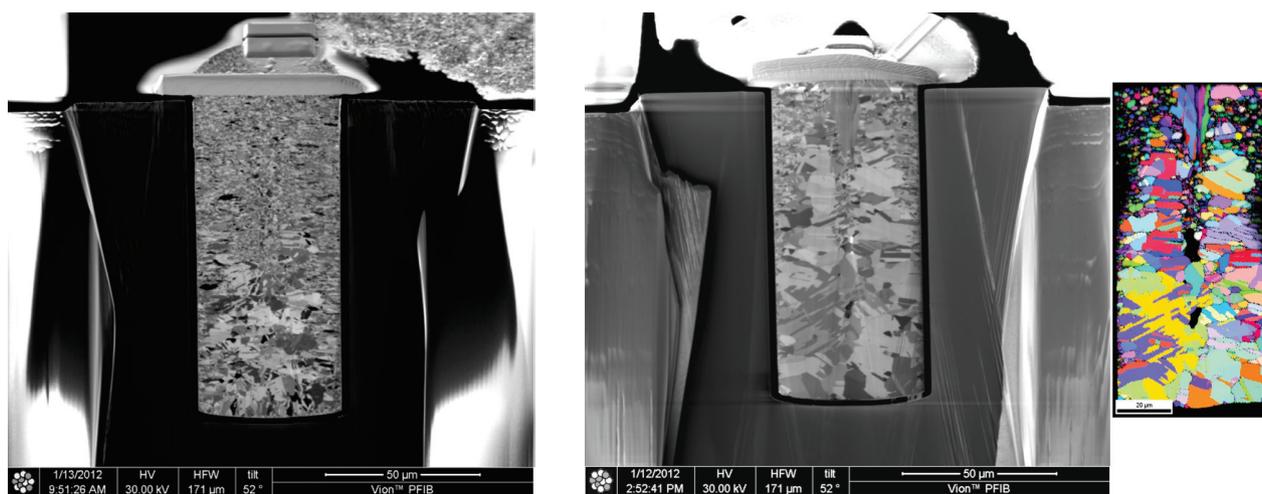
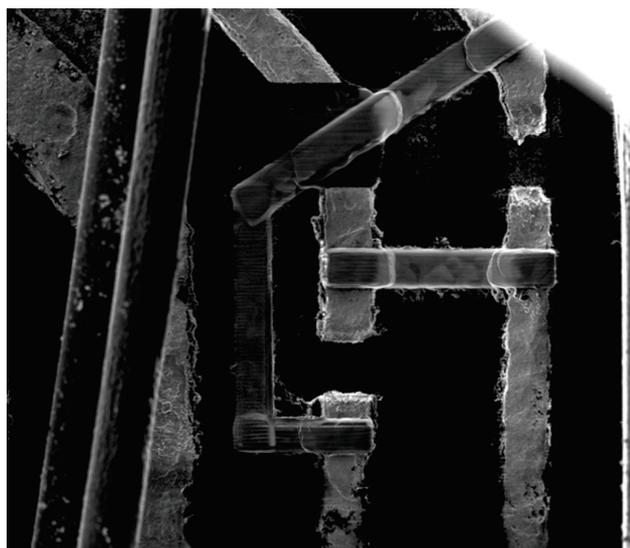


Fig. 1 PFIB cross section of 50- $\mu\text{m}$ -diameter  $\times$  150- $\mu\text{m}$ -deep copper-filled TSV followed by electron backscatter diffraction analysis

## DELAYERING/DEPROCESSING

Delayering of integrated circuit (IC) devices is an important tool for semiconductor failure analysis, reverse engineering, and circuit edit activities.<sup>[4]</sup> Once a defect has been localized, it is necessary to isolate, inspect, and perform failure analysis. One method to enable this is to remove layer after layer until the defect is exposed. Traditionally, this was performed by mechanical polishing, followed by observation in either an optical or electron microscope. While this method can provide reproducible results in older process nodes over large areas (which is important for reverse engineering), it is neither site-specific nor planar. In addition, this method does not have predictable end-pointing, and the functionality of the entire chip is lost due to the destructive nature of the polishing.

The FIB offers the means to retain chip functionality while removing only localized regions during delayering. This is a great advantage, allowing further analysis (voltage contrast, defect analysis, electrical probing, etc.)



**Fig. 2** Package-level edit with xenon PFIB consisting of two copper trace cuts and two platinum connections while preserving electrical functionality with insulator deposition

or circuit edit to be performed when the layer of interest has been reached. However, it is no easy task to delayer modern IC devices in the FIB, due to the large number of different layers (with vastly differing milling rates) that are present with varying thicknesses and mechanical properties. The divergent milling rates of the different materials present result in nonplanar delayering, often with many layers visible at one time.

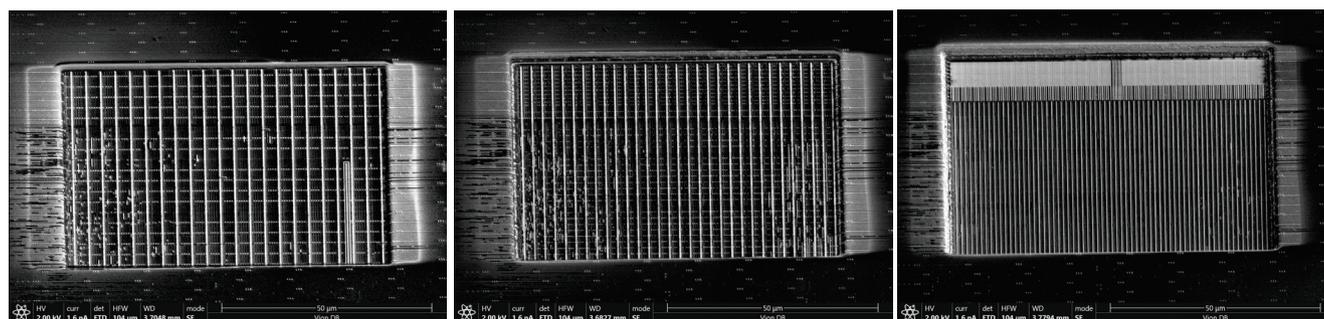
A new beam chemistry, Dx,<sup>[4]</sup> has been developed to deliver planar delayering. It can mill both dielectric and mixed-field regions uniformly. In addition to better end results, the process is simpler because it is continuous, without the need to stop the milling to change gas chemistries when different layers are encountered. In addition, the reduced enhancement of the milling improves controllability, which is an important consideration when dealing with sub-100-nm-thick layers.

An example of the delayering possibilities when Dx is combined with the xenon beam can be found in Fig. 3. Here, a 22 nm device has been delayered from the front-side. The images show the excellent planarity achieved by delayering through a stack of six copper metal layers and SiO<sub>2</sub> and low-k dielectrics using the significantly larger beam currents than are available on the gallium FIB for delayering. Despite these larger currents, no degradation of the planarity in the trench is observed.

The combination of delayering with Dx and the xenon PFIB produces a more representative surface, which is important for (in situ) nanoprobe experiments. Implantation from the xenon ion species is lower than gallium, but gallium, being a metal, produces some conductive redeposit on the surface. This does not occur when the xenon beam is used, and a more pristine surface results. This allows proper electrical characterization to be carried out through nanoprobe.

## SITE-SPECIFIC FAILURE ANALYSIS

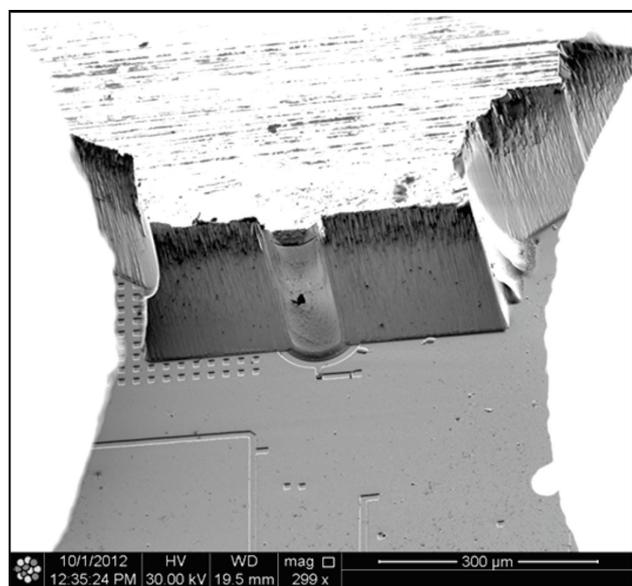
Today, 3-D system-in-package integration together with advanced interconnect technologies based on TSVs,



**Fig. 3** 100 × 100 μm trench exposing (left to right) M9, M7, and M5 on a 22 nm device

through-encapsulant vias, and microbumps are considered some of the most promising enabling technologies for “More than Moore” solutions.<sup>[5]</sup> These technologies involve vertical dice stacking or chip embedding with high-density interconnects and are based on combinations of process steps that come from formerly strictly separated technology areas. Thus, there is an increasing need to understand a large number of different interface properties between different interconnects and, with any encapsulation or lamination materials, to control and optimize process steps and layer thicknesses and to avoid any defect formation that potentially could affect the component’s reliability. This complexity in terms of design, new materials, and material combinations also requires the development of new system-adequate failure analysis tools capable of providing information on adhesion mechanisms, interdiffusion, and phase formation processes, or on electrical short, crack, and void formation issues. Therefore, there is a demand for metrology, physical characterization, and failure analysis of a wide range of 3-D interconnect technologies and relevant processes, and also for preparation and analysis techniques that allow access to buried structures providing physical information at the nanometer scale within a large field of view. Depending on the material under investigation, both the higher current and the higher sputter efficiency of xenon significantly improve the range of application fields and/or the analysis throughput. This makes the PFIB a very attractive tool for the analysis of relatively large interconnect structures without any need for mechanical preparation steps.

An open TSV interconnect technology has been developed as an alternative to copper-filled TSVs. The Bosch



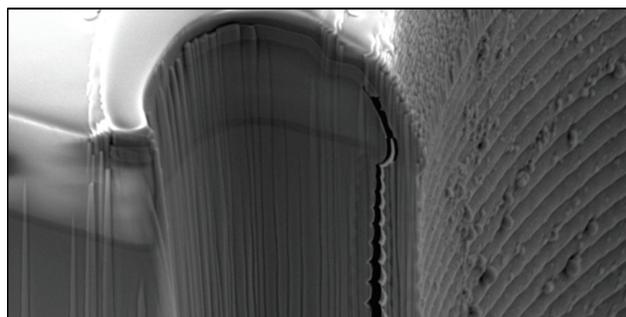
**Fig. 4** Delamination of sidewall in open TSV, milled with PFIB. Source: Ref 2

etching process, combined with further IC processing steps, is used to form TSV structures with sidewall isolations and metallization with titanium/TiN, tungsten, and aluminum. Finally, the TSVs are capped by a silicon dioxide film and silicon nitride layers. For process optimization and failure analysis, the sidewall layer structure must be imaged and measured. Rapid PFIB milling can provide precise cross sectioning to gain access to specific TSV areas of interest or to defect sites within the TSV structure.

Figure 4 shows an open TSV with localized delaminated sidewall layers. To find the root cause, the delaminated sidewall interface should be analyzed by scanning electron microscope (SEM) and transmission electron microscope imaging. In this case, mechanical grinding was not an option for rough cross sectioning, because of the high risk to fully detach the delaminated sidewall layer. Therefore, rapid PFIB milling with a 1.3 μA xenon beam was applied to obtain a cross section through the middle of the TSV. A box of 700 × 300 μm and 500 μm was milled within only 5 h. Then, local sidewall polishing at 70 nA was done at the upper left of the TSV, followed by SEM imaging of the delaminated sidewall layer.

## DIE-TO-DIE INTERCONNECTS

A fundamental requirement for any 3-D interconnect scheme is a method for connecting the stacked dice to each other and/or to any interposers used. Stacking schemes may use a combination of face-to-face, face-to-back, and die-to-interposer bonding and could also involve a direct connection between the dice or include a redistribution layer added to the front/back of the originally manufactured die. Whatever the scheme, there are typically some similar challenges for creating site-specific sections of the interconnects, in particular, locating the



area of interest within the stack and then gaining access to the interface in a timely manner, often through a full die thickness.

Figure 5 shows examples of three bonding schemes: face-to-face, face-to-back, and silicon interposer. The first example (Fig. 5a) is a face-to-face bonding layout, where a series of Kelvin structures had been created in a reliability test structure. In such a structure, the part of the device stack accessible to the ion beam is the silicon substrate of the upper die. An in situ infrared microscope was used to image through the silicon substrate to locate the area of interest.

After locating the area of interest, the PFIB preparation took 41 min to expose the section (using beam currents from 1.3  $\mu\text{A}$  to 59 nA). Like earlier figures, these images show the utility of ion beam microscopy on the cross-sectional face. In particular, the different components (intermetallic compounds, or IMCs) that make up the interconnect stack can be observed as layers of differing contrast and grain structure (e.g., large, small, or no grains visible), which will be characteristic of each material composition. By characterizing a comparable device with electron backscatter diffraction (EBSD) or similar technique, a translation from FIB contrast and grain structure to metallurgical composition can often be made, allowing analysis of the bonding process, including layer thicknesses, to be obtained directly from the FIB image.

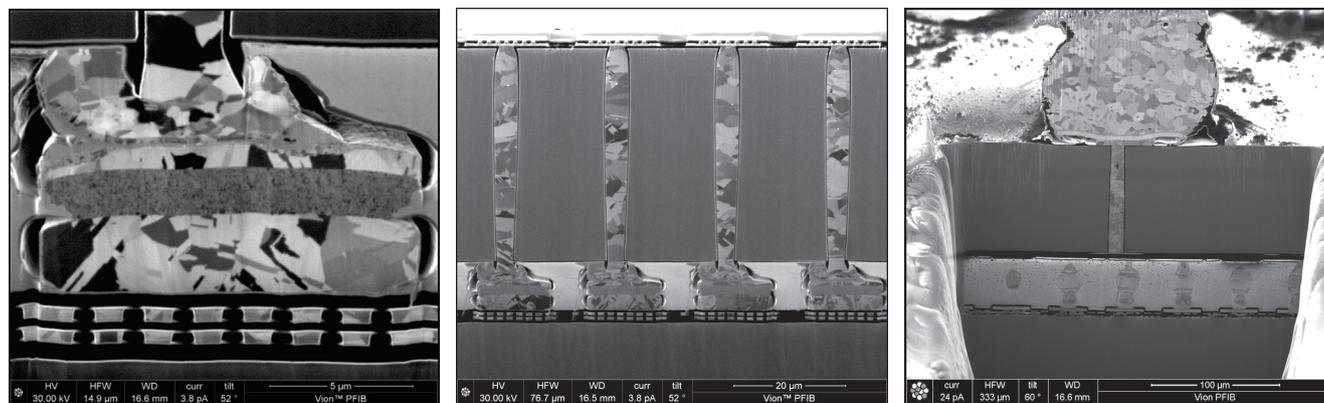
Figure 5(b) shows a face-to-back bonding scheme incorporating TSVs. Here, a series of 31 TSVs and associated die-to-die bonds were sectioned. The sample preparation took  $\sim 2.5$  h. In a subsequent step, the cross-sectional face was milled further to expose the next set of TSVs; this took an additional 61 min of milling. The FIB images again show the details of the bonding process as well as some voids in the underfill around the bonds. Such images could also be used to assess die-to-die

alignment or make other critical measurements that can only be assessed once the completed 3-D structure has been assembled. In addition, the localized nature of the sectioning means that multiple sections can be made, even at different angles, which allows more data to be collected from a single device.

Figure 5(c) is a failure analysis investigation on an interconnect stack that included a packaging bump onto a silicon interposer with a TSV, which was then microbumped to the lower die. The sample was part of a reliability burn-in test, and the sectioning was targeted at microbumps thought to be responsible for sample failures. The main section took  $<2$  h. When the microbumps were imaged with the FIB, evidence of a problem at one of the interfaces was noted. Higher-resolution SEM imaging of a subsequent slice through the defect showed a clear delamination. Further delamination examples on other microbumps were also found with the PFIB.

## DIE-TO-PACKAGE INTERCONNECTS

Strength, quality, and reliability properties of interconnects in microelectronic packaging and microsystem integration are closely related to the formation, growth, and physical properties of the different IMCs formed in the interfaces of solder joint contacts. Metallographic grinding techniques are typically used for cross sectioning to characterize the IMC and interfaces to the upper and lower metallization. However, mechanical grinding could cause artifacts such as smearing effects or crack formation caused by the mechanical impact during grinding. Additionally, sometimes it is helpful to access selected solder bump contacts on one device from different directions, which is not possible with mechanical grinding. The PFIB preparation provides a very precise navigation to the region of interest by sample imaging. Cross sections can easily be aligned in different directions.



**(a)** **(b)** **(c)**  
**Fig. 5** (a) Face-to-face, (b) face-to-back, and (c) silicon interposer cross sectioned by PFIB

High-current PFIB milling offers a new opportunity to cut through the whole silicon die and solder bump contact without any need for mechanical grinding procedures. In this case, the solder joint contacts have a diameter of 150  $\mu\text{m}$ , which is a typical dimension. As a first step, rapid cross sectioning was done at the highest achievable xenon beam current of 1.3  $\mu\text{A}$ . The coarse PFIB milling of a 500- $\mu\text{m}$ -long and 1-mm-deep box takes  $\sim 10$  h of milling time. The final polishing was done by rocking beam milling at  $\pm 8^\circ$  sample tilt by using a 1.3  $\mu\text{A}$  xenon beam.

Figure 6 compares the PFIB-sectioned<sup>[6]</sup> solder joint contact to a standard metallographic cross section. The cross-sectional surface using PFIB preparation has a remarkably improved quality; nearly no preparation artifacts, for example, curtaining, are detectable. The microstructural investigations show interface reactions between solder joint contact and underbump metallization. The underbump metallization shows the typical depletion zone of the nickel-phosphorus ( $\text{Ni}_3\text{P}$  layer) that occurs because of the interdiffusion of nickel into the tin solder material and the nickel-tin IMC formation at this interface, respectively.

## IN SITU ELECTRICAL FAULT ISOLATION

Transistor and interconnect-level characterization plays a critical role during semiconductor process development, for which samples are historically prepared using wet/dry etch, mechanical polishing, or conventional FIB techniques. Using PFIB-based deprocessing techniques, it is now possible to prepare advanced-technology-node samples for electrical fault isolation (EFI) over large areas (hundreds of micrometers) with higher yield and repeatability. The EFI samples are further analyzed using SEM image-based inspection and analysis, SEM-based nanoprobing, or atomic force probing (AFP). Historically, samples were polished on mechanical polishers by a

sample-preparation expert, followed by inspection on an optical microscope or SEM to ensure that the desired layers were reached. Then, the samples were moved to an SEM- or AFP-based prober for further analysis by a different set of probing experts. These two steps were repeated for a few cycles as long as further deprocessing was possible or until the fault was isolated. There was a long wait time between each stage in the queue from sample submission to final results, due to tool and operator availability, resulting in lower yields due to required operator skills and tool capabilities.

Recent advances have enabled the integration of sample-preparation and fault-isolation capabilities inside a DualBeam PFIB system, thereby creating a single-tool, single-operator solution that takes the sample from delayering through high-resolution imaging and SEM-based nanoprobing without sample transfers, wait times, or multiple experts. This in situ preparation and analysis approach provides faster results at a much higher yield and in a more predictable manner. PFIB-based deprocessing, in combination with SEM-based imaging and nanoprobing for localizing electrical faults, has been performed on samples at the 10 nm node with transistor I-V characterization, electron beam induced current (EBIC) on diffusion, and electron beam absorbed current (EBAC)-based analysis on a copper, low-k dielectric interconnect stack. High-resolution imaging with low-beam-energy SEM down to 350 eV combined with low-drift probes enables easier setup resulting in analysis, as shown in Fig. 7(a) and (b).

With material-removal rates 20 to 100 times greater than gallium liquid metal ion source FIB, PFIB is becoming an essential tool for failure analysis of larger structures created by new advanced packaging processes. Failure analysis and fab support labs can also take advantage of the DualBeam PFIB's targeted chemistries for physical

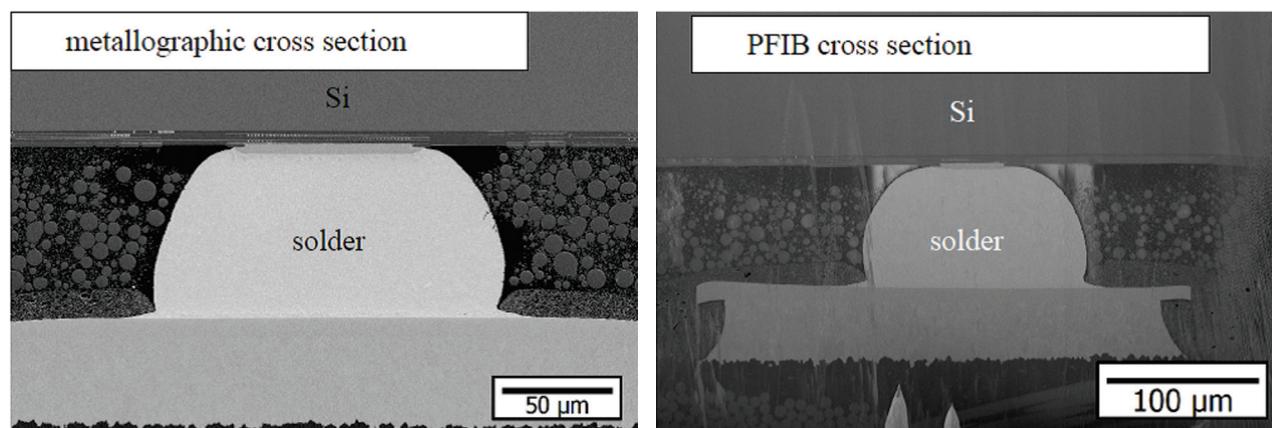
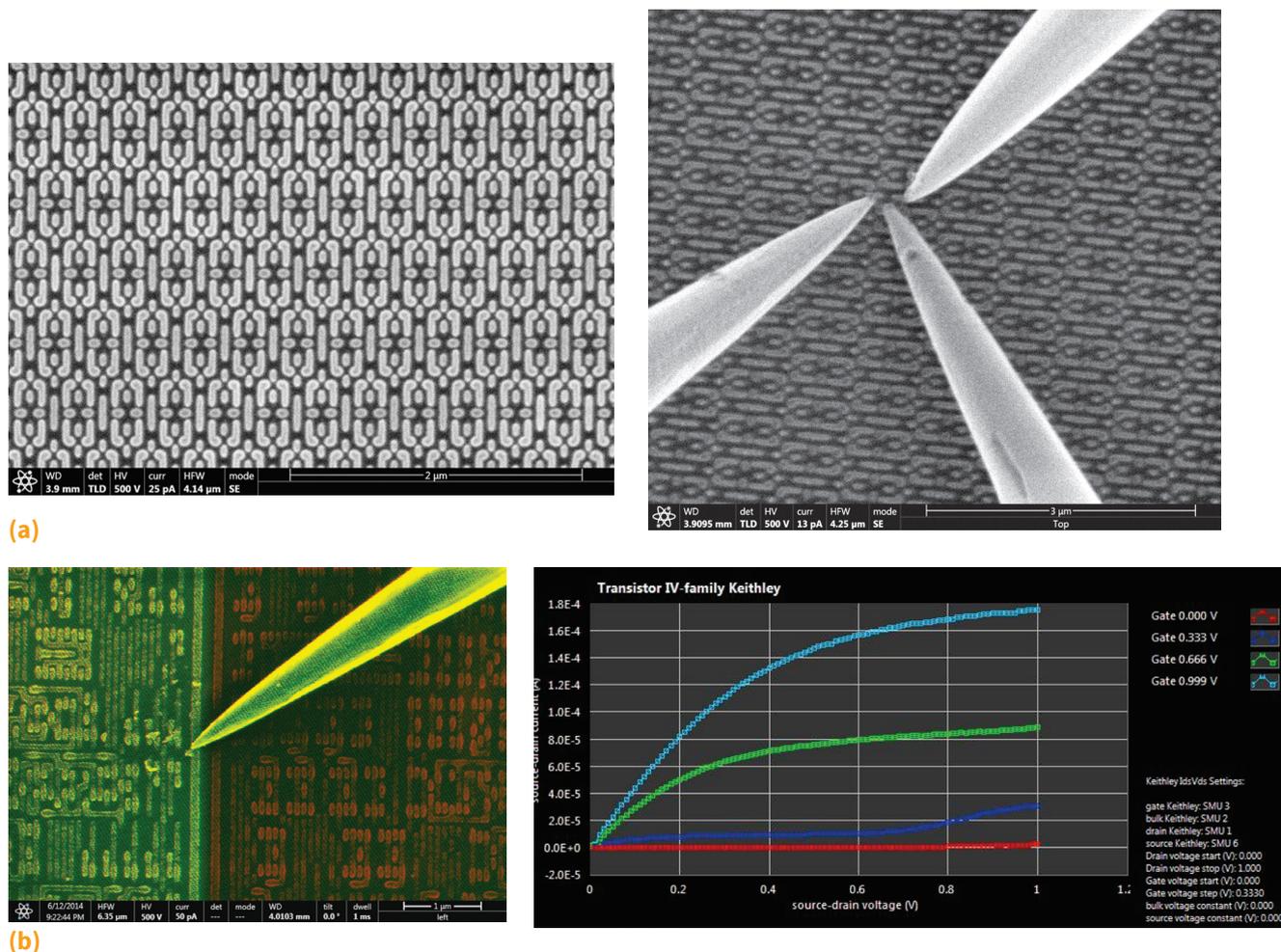


Fig. 6 PFIB-sectioned solder joint compared to metallographic cross section



**Fig. 7** (a) 22-nm-node sample deprocessed to contact level with PFIB with probe touchdown. (b) Transistor characteristics of a 22-nm-node device

failure analysis, deprocessing and device modifications, and workflow solutions, such as EFI sample preparation, nanoprobing, and EBIC and EBAC for fault isolation. The DualBeam also offers analytical capabilities, such as EBSD and energy-dispersive x-ray for chemical, structural, and compositional analysis.

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## ABOUT THE AUTHOR



**Surendra Madala** is a product marketing manager at FEI in Hillsboro, Ore., focusing on large-area sample preparation and advanced packaging analysis solutions. He has 20 years of experience in the areas of IC diagnostics, circuit edit, IC product engineering, physical and electrical failure analysis and fault isolation, and semiconductor analytical equipment development and marketing. He holds an MBA from Southern Methodist University, a Master's in electrical engineering from the University of Houston, and a Bachelor's degree in electrical engineering from Nagarjuna University, India. Surendra is a member of EDFAS and SEMI.

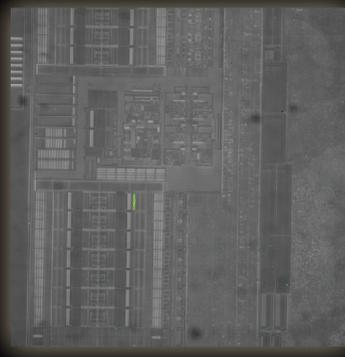
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# ISTFA 2015 WRAP-UP

James Demarest, ISTFA 2015 General Chair  
IBM  
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The 41st International Symposium for Testing and Failure Analysis (ISTFA 2015) occurred in Portland, Ore., this past November. The theme of the conference was “Follow the Data,” which appears time and time again in our professional lives. The conference was an outstanding success from my point of view, as we had the highest conference attendance in the past five years and, more importantly, everyone I talked to was enjoying themselves and learning something new.



Keynote Speaker Dr. Albert Lin addressing the audience

## KEYNOTE SPEAKER: DR. ALBERT LIN, NATIONAL GEOGRAPHIC EXPLORER—SEEING THE UNKNOWN: THE HIGH-TECH SEARCH FOR GENGHIS KHAN

The keynote speaker, Dr. Albert Lin, was phenomenal. He spoke for an hour about his experiences traveling the world and, specifically, his use of noninvasive technologies to determine the location of Genghis Khan’s tomb. In addition, Albert was one of the first to use crowd sourcing to sift through vast amounts of imaging data to narrow down his search. I was captivated by the very personal story he told, inspired by his enthusiasm and use of technology, and greatly enjoyed my personal conversations with him at the conference on the eclectic topics we covered. On one or two rare occasions during Albert’s talk, I was able to look back at the rest of the audience and see everyone else equally engrossed in his tale.

## THE TECHNICAL PROGRAM

The conference launched on October 31 with the short courses, followed by the main block of tutorials.

These were organized by Susan Li of Spansion, Mayue Xie of Intel, and their team. The tutorials ran as a triple track on Sunday, and I hope everyone was able to take

advantage of the educational opportunity they represent. Two tutorials were integrated into the technical program this year; these covered medical devices and package-level fault isolation.

Sam Subramanian of Freescale did an amazing job as Technical Program Chair. He and his team of session chairs put together a great week of more than

60 podium presentations and a very full poster session. As we have come to expect at ISTFA, the talks ran the gambit of failure analysis topics, from microscopy to sample preparation to electrical characterization. There was even a very well-represented counterfeit microelectronics technical session, which contained five talks.

Becky Holdford greatly assisted all of the platform presentations in her role as Audio/Visual Chair. I’m sure all the presenters benefited from her wealth of experience and knowledge. I know the poster session was very popular this year as well. The photo and video contests went off without a hitch. Rose Ring of Globalfoundries oversaw the video contest, which had at least five video submissions.

## SOCIAL EVENT, PANEL DISCUSSION, AND USER GROUPS

The social event, organized by Rick Livengood of Intel, was held at the Punch Bowl Social in downtown Portland; it was a tremendous success. Approximately 300 people attended the event, and it was a great way to start off the conference week on Monday night. The venue had something for everyone, and I saw many smiles on faces and light sabers in hands throughout the evening.

The panel discussion, organized by David Grosjean of Qualcomm and consultant Kendall Scott Wills, was extraordinarily well received. The topic was “First Silicon Debug: Rapid Identification and Correction of Product Systematic Failures.” People were still coming up to me the next day to tell me how much they enjoyed the topic and discussion.

Nicholas Antoniou of ReVerA and Rose Ring of Globalfoundries put together the four User Groups at this year’s ISTFA. These targeted discussion topics are a great learning environment for both novice and experienced users to interact and gain new insights.



**ISTFA 2015 attendees enjoying the Expo**

## EXPO, ATTENDEE CHAIR, AND INTERNATIONAL CHAIR

ISTFA isn’t just about the technical program. There are other critical aspects of the conference that need to be recognized as well. Efrat Moyal of LatticeGear guided the Expo Committee through another successful year. It was wonderful for me to see so many vendors bringing tools to the Expo, as so much more is learned by sitting down in front of a piece of equipment and using it.

Felix Beaudoin embraced a challenging role on the Organizing Committee by becoming the first Attendee Chair. Felix was charged with improving the overall attendee experience at the conference, and he more than exceeded my expectations. Also, it is important to point out that ISTFA is an international conference, with approximately half of our presenters coming from countries outside of the United States. Dr. Lihong Cao of AMD headed the International Committee in 2015, and she did an excellent job.



**General Chair James Demarest and the ISTFA 2015 Organizing Committee**

All of us on the Organizing Committee extend our heartfelt thanks for making the conference such a great experience. We look forward to seeing you next November in Fort Worth, Texas, at ISTFA 2016!

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Wentao Qin, Technology Assessment and Characterization Lab, ON Semiconductor

## ISTFA 2015 BEST POSTER:

*"Selective Etching of Highly-p-Doped Si Substrate Using Low-p-Doped Si epi as an Etch Stop Layer"*

Valentina Korchnoy, Intel Israel

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*"MOFM: Magneto-Optical Frequency Mapping System for Very Low Resistance Short Failure Current Imaging"*

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**Congratulations to the following winners:**

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- 1st Michael Woo, Raytheon Failure Analysis Lab
- 2nd Joseph Ziebarth, IM Flash Technologies, LLC
- 3rd Martin Serrano, Raytheon Failure Analysis Lab

### Category II: Black & White Images

- 1st Noel Forrette, IM Flash Technologies, LLC
- 2nd Luigi Aranda, Raytheon Failure Analysis Lab
- 3rd Rony R. Celetaria, Analog Devices Gen. Trias, Inc.

### Category III: False Color Images

- 1st Mark Kimball, Maxim Integrated Circuits
- 2nd Andrew Ozaeta, Raytheon Failure Analysis Lab
- 3rd Debra L. Yencho, Texas Instruments

All winners received a recognition plaque or certificate and a one-year EDFAS membership. The winning entries will be featured on the cover of this magazine during 2016. They also may be viewed on the EDFAS website.

## EDFAS 2015 VIDEO CONTEST WINNER

**Congratulations to the following winner:**

*"IR Thermography, Running Bug inside Power MOSFET," by Kevin Sanchez, Elsa Locatteli, and Florie Mialhe, Laboratories and Expertise, Quality Assurance, Centre National d'Etudes Spatiales (CNES), Toulouse, France*

The winner received a \$50 gift card, a complimentary registration to a future ISTFA conference, and a first-place winner plaque. The winning entry may be viewed on the ISTFA 2016 website.

## ISTFA 2015 PANEL DISCUSSION AND USER GROUP SUMMARIES

Summaries of the ISTFA 2015 Panel Discussion and the four User Groups can be found beginning on page S-1 of this online issue. ■

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# A SUMMARY OF THE ISTFA 2015 PANEL DISCUSSION: FIRST-SILICON DEBUG

Felix Beaudoin  
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The ISTFA 2015 Panel Discussion was dedicated to the challenge of performing failure analysis (FA) and debug of first-silicon products. Time-to-market of new products is critical, and product systematic failure can result in months of delay. High pressure is on the FA laboratory, which is expected to find root cause in days, if not hours. The panel presentations discussed methodologies for performing first-silicon debug and the importance of setting up the right culture and environment for success.

The panel members were Ryan Ross of NASA Jet Propulsion Laboratory, Pasadena, Calif.; Geir Eide of Mentor Graphics, Wilsonville, Ore.; Izak Kapilevich of DCG, Chandler, Ariz.; and Joe Lebowitz of Maxim. The panel was moderated by Tracy Myers, ON Semiconductor, Gresham, Ore.

The panel opened with a presentation by Ryan Ross on the complex task of planning for new product introduction (NPI) to enable successful first-silicon debug. He argued that ultrafast NPI issue identification is a high-visibility opportunity to shine or fail. Ryan highlighted that an FA plan must be started 6 months prior to a new product and should include deliverables such as layout, test conditions and test program, automatic test pattern generator diagnostic package, memory logical to physical translation, and probe card and load board to enable dynamic FA. Planning should start approximately 18 months in advance if new tooling, process flow, and procedures are required to tackle future FA challenges on upcoming technologies.

Geir Eide then focused on the test perspective of first-silicon debug. He stated that effective and automated diagnosis of a test failure requires an accurate model of the actual fail mechanism. However, design marginalities, which are often involved in new product failures, are hard to model. Geir presented two trends that further increase

the diagnosis challenge: the introduction of more complex design-for-test structures, and the growing number and complexity of on-chip instruments. On the bright side, he presented the IEEE 1687 IJTAG standard that enables access to any component within a system-on-chip without a priori knowledge through instrument-specific instructions.

Izak Kapilevich followed with an introduction on the FA organization and described the FA process flow used to identify failure root cause. He argued that when a new device is introduced with a new problem, the FA lab will typically try all static and dynamic optical-based techniques to localize the failure to a smaller area of interest to improve the physical FA success rate. He also emphasized the importance of wafer-level testing to perform quick die-to-die analysis to improve turnaround times.

Izak presented a comparison between three companies and correlated their respective first-silicon debug time to root cause to their level of FA readiness.

Joe Lebowitz concluded the panel presentations with five

examples that illustrated the critical importance of test and FA for first-silicon debug. In his opinion, the fab ultimately owns the yield issue even if the root cause can be design, test, or FA. The first case study he presented highlighted a yield loss due to a frequency shift on a multicore processor that was ultimately traced back to a test sequence change to improve test time. The die-heating differences shifted the measured  $F_{max}$ . The corrective action was to put in place a change control for all changes, including test. In another example, Joe discussed a 0 km automotive customer return that failed for missing-metal defects. Root-cause analysis identified that, due to incomplete test coverage, the fab defects could not be screened in the specific failing block. Containment action was to implement 100% in-line defect scans of specific care area at all metal layers. Joe concluded

**“THE PANEL PRESENTATIONS  
DISCUSSED METHODOLOGIES  
FOR PERFORMING FIRST-SILICON  
DEBUG AND THE IMPORTANCE OF  
SETTING UP THE RIGHT CULTURE AND  
ENVIRONMENT FOR SUCCESS.”**



that accuracy and speed in diagnosing issues is essential to semiconductor manufacturer success or failure.

The last portion of the panel was dedicated to an open conversation between the attendees and the panelists. It was discussed that, to achieve success, everyone must own the issue across organizations. It was mentioned that the FA engineer should always be involved in any problem-solving session. One attendee also commented that

spending money for tools is the easy part; finding FA engineers with the appropriate skills is harder. This comment led to several exchanges on what defines an FA engineer, and most attendees must have recognized themselves in the different descriptions given. The panel concluded on a topic proposition for the ISTFA 2016 Panel Discussion: “The Next-Generation FA Engineer.” See you next year in Fort Worth, Texas! ■

## ISTFA 2015 CONTACTLESS FAULT ISOLATION USER GROUP

Moderators: Patrick Parady and Dan Bockelman, Intel Corporation  
 patrick.parady@intel.com  
 dan.bockelman@intel.com

Optical probing techniques continue to be critical in the failure analysis (FA), fault isolation (FI), and product development space. As the industry moves into the 10/14/16/22 nm geometries, many wonder if the current techniques will generate the results needed to improve yield, debug, and characterization and to move products to market. Or, instead, are new technologies badly needed to sustain today’s pace of innovation in the process space? To that end, the topics this year were specific toward new techniques and technologies. An inflection point in the wavelengths of current infrared (IR) tools to potential shorter wavelengths solutions was discussed. New studies and some initial toolset work to include visible laser probing was completed, as well as an alternative 1154 nm wavelength for current IR toolsets. A full presentation on debug data techniques, for the foundry- and design-only-based scenario, was also given at this year’s conference. Further discussion followed on a number of design-for-test (DFT) and scan failures, and the physical toolsets/techniques used to help solve silicon issues were demonstrated. Future recommendations on DFT, test looping, and test complexities moving forward were discussed as well. Finally, a new technique used to debug/characterize silicon designs in a motherboard/platform setup was discussed. For a new integration of an infrared emission microscopy (IREM) system and a motherboard, the means to debug and characterize new products and features was completed.

Dr. Christian Boit (Berlin University of Technology, Berlin, Germany) gave the first presentation, “Contactless Visible Light Probing for Nanoscale ICs through 10  $\mu\text{m}$  Bulk Si.” This presentation focused on imaging and optical techniques with visible laser light. Using confocal

microscopy to obtain better degrees of freedom in probing, the near-infrared plus silicon solid immersion lens (SIL) combination is only good for >20-nm-node technologies. However, moving forward, a minimum 2 $\times$  improvement will be needed to keep up with the aggressive shrink for future process nodes. Because the numerical aperture for IR-based optical tools is already at the limit (3.5 for silicon), one of the only other adjustments is lambda (wavelength) for resolution improvements. Using shorter-wavelength lasers has advantages, as described above, but very big challenges as well. One of these challenges is that silicon is very absorptive at the shorter wavelengths, especially those in the visible range. For his work at 650 nm, Dr. Boit described the reasonable absorption depth (AD) for the 650 nm laser to be  $\sim 3.5 \mu\text{m}$  remaining silicon thickness (rst). This rst depth provided the optimal working distance for the focal plane using the confocal system. The advantage here is that only the focal plane is transferred and the back surface reflection is suppressed, which may increase resolution by 1 to 1.5 $\times$ . For 10  $\mu\text{m}$  of rst, the AD is 6 $\times$  that of 3.5  $\mu\text{m}$  rst, but using a confocal system still provides a good image. Dr. Boit used a Zeiss laser scanning microscope air gap (non-SIL) system for his experiments. He measured improvements up to 1.68 $\times$ , using an older process technology. Dr. Boit stated that the bandgap for the SIL must be >1.9 eV and that GaP, transparent to 550 nm, was identified as a good candidate material. He also stated that the technology will not be useable with GaP above 2.25 eV; instead, other materials (i.e., SiC) will need to be explored. However, SiC has a worse index of refraction and the maximum silicon thickness decreases further, so there are challenges with respect to future materials as

well. By the end of the year, Dr. Boit expects to have more experiments completed using a Hamamatsu detector for modulation results. There was further audience discussion centered around the power needed for the laser-assisted device alteration (LADA) effect, the detected waveforms that had spikelike artifacts on the leading edge, and finally why Dr. Boit included e-beam technology in his 2019 development roadmap.

Dr. Baohua Niu (Intel Corp.) gave the second presentation, “1154 nm Laser for Defect Localization, Design Debug and FI Applications.” Current optical techniques in the near infrared use heavily both the 1064 nm and 1300 nm to >1340 nm wavelengths for debug applications. The 1064 nm gives the highest resolution, while lasers in the 1300 nm wavelength range are losing steam in the industry due to the aggressive process shrink and the required resolution needed to effect productive node isolation, and so on. Using the 1064 nm wavelength also has some drawbacks. While it is the industry’s workhorse wavelength for resolution and optical techniques, the SIL materials used to support it have different properties. While the 1064 nm wavelength, used in conjunction with the silicon SIL, has the best possible imaging resolution, for higher-temperature work, the SIL becomes highly absorptive and less stable to work with over the range of the silicon area at different operating temperatures. The 1064 nm wavelength, when used with GaAs material, does not have the same temperature instability as the above but has slightly less resolution versus the aforementioned silicon SIL material, has the propensity to corrode over time, and is expensive. Due to the above issues for both the wavelength and SIL materials, Dr. Niu explored to see if there was an alternative to the aforementioned issues by using a different wavelength. The 1064 nm laser is below the 1107 nm silicon indirect bandgap, and the 1319/1340 nm lasers are above. Because minimum absorption occurs at 1154 nm in doped silicon and is  $\sim 20\times$  lower than that of 1064 nm, the question becomes: Could it also be a good light source for optical techniques that we use today as an alternative, and, if so, what are the tradeoffs? Dr. Niu showed the experimental results using a system with an 1154 nm light source and a silicon SIL tip with a 3 mm radius with  $<30\%$  signal loss. Due to advantages in the bandgap of silicon, the 1154 nm laser has much less effect on silicon versus 1064 nm (charge injection). A number of real data examples were discussed, including waveforms and continuous-wave signal imaging and probing (frequency maps), showing how well the 1154 nm laser was used. The LADA effect for 1154 nm is similar to that of 1064 nm (typical shift of 5 to 10 ps). The modulation signal strength is  $\sim 2\times$  stronger with

1154 nm versus the current 1064 nm optical techniques. For waveform probing, the transistor signal strengths are comparable; PMOS has the same strength as NMOS devices. Although with the higher 1154 nm wavelength (versus 1065 nm) there is a small 5% loss in overall resolution, the strong modulation of light and other considerations that make the 1154 nm an acceptable alternative to the 1064 and 1300 nm technologies can further simplify the overall optical probe tool configuration by use of only one wavelength (1154 nm) versus the dual-wavelength system, comprised of both the 1064 and 1300 nm lasers. The cost of SIL tip material and overall tool ownership can also be reduced.

Dr. Joy Liao (NVIDIA Corp.) gave the third presentation, “Volume Electrical FA for Product-Specific Yield Enhancement.” Dr. Liao started her presentation by stating that foundry-based companies cannot ramp yield alone. She also made strong observations that yields are increasingly product-specific and that DFT methodologies are key to ramping yield, including shift, chain, automatic test pattern generation (ATPG) at speed, memory built-in self-test, and so on. Physical failure analysis, based on diagnosis alone, has poor success rates. Shift failures are a huge portion of early failures. Reliability failures often appear as shift failures as well. Dr. Liao also talked about the application of electrical failure analysis (EFA) techniques to observe internal circuit behavior. She showed a number of test cases, including:

- Good/bad die scan chain image/comparison, using emission toolset/techniques
- Modulation mapping on a broken scan chain
- Modulation mapping and continuous-wave laser voltage probing (LVP) on a broken scan chain
- Combination of both LVP and emission on a broken scan chain
- Soft defect localization (SDL) and ATPG at-speed diagnosis
- SDL with voltage dependence

Dr. Liao further discussed the capability to automate chain navigation with software means to make more intelligent localization decisions. On 20 nm, more aggressive DFT and test compression is challenging. Moving forward, more aggressive DFT architecture continues to be needed. Less data are available from production wafer-level testing, further limiting volume software diagnosis. More complicated test loops and requirements for LVP work are becoming more challenging as well. Up to five broken scan chains per day were solved. The combination of LVP, modulation mapping, SDL, and emission techniques is

required for fast EFA on current and future process technology nodes. Further questions and discussions were held, including what percentage of on-die cases goes to physical versus electrical FA. This is a business decision, and it varies based on the negotiation between the design house and the foundry. Another question was asked about foreseeing foundries being able to support the industries with the right agreements in place. The response for NVidia was yes, and that NVidia is willing to share their in-depth knowledge to enable foundries to be successful.

Mr. Dave Budka (Intel Corp.) gave the fourth and last presentation, “Power Debug on Fully Integrated Voltage Regulator (FIVR) Introduced on Deep Low-Power States.” Mr. Budka outlined the Haswell ULT (mobile chip) and how it contained an FIVR system, including the high-level reasons why Intel did this design. With a new technology, there is always a need to fully validate/characterize the new design and how it is operating, looking for any potential issues. Mr. Budka went on to outline how the new FIVR technology is based on the principle of a buck converter (up to 16 phases, 90% efficient) and has a feedback mechanism to sample workloads for different applications. It also was the power control for seven domains dynamically, as the chip is changing its workload and power states. Mr.

Budka discussed the need for the platform IREM system. This system consists of an IREM optical probe tool with a motherboard/platform system docked to the table, with the means to load and run different software applications, and so on. Mr. Budka showed numerous IREM images for both static and dynamic cases, demonstrating the behavior of the FIVR domains and the data supporting the removal of an on-package air core inductor to lower overall product costs. Additional test cases, showing the results from both electrical overstress and thermal runaway, were discussed. Further audience discussion centered around how motherboard/platform work is difficult to enable but provides a lot of good information, especially with the capability to run the same (or very similar) applications that original equipment manufacturers may run.

This year’s Contactless Fault Isolation User Group had 98 attendees, representing semiconductor manufacturers, industry suppliers, universities, and national labs. The session had four technical presentations, each followed by a presenter’s question-and-answer panel session. The presentations covered a wide range of important industry topics. Excellent presenters, panelists, and audience participation made it another productive year for the ISTFA Contactless Fault Isolation User Group.

## ISTFA 2015 FIB USER GROUP

Moderators: Steven Herschbein, IBM, and Richard Livengood, Intel Corporation

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The 2015 FIB User Group meeting was well attended, with approximately 80 people representing the failure analysis, debug, and materials analysis communities. This year’s User Group covered three basic topic areas: novel patterning applications, novel ion species for transmission electron microscopy (TEM) prep and other applications, and TEM sample preparation.

The session began with two presentations on novel Ga<sup>+</sup> FIB patterning techniques. The first was by Philipp Scholz (Berlin University of Technology, Berlin, Germany) on the use of a Ga<sup>+</sup> FIB to create a solid immersion lens (SIL) in the silicon substrate to enable optical probing of subsurface transistors. This technique increases the numerical aperture for optical microscopes without having an actual SIL lens on the scope, an application that may be necessary if the sample substrate is too small to land a SIL lens on the surface. This work at TU Berlin demonstrated optical resolution down to 387 nm.

The second novel patterning presentation was by Jason Sanabia of Raith America, Inc. Jason presented the use of the Raith nanoFIB Two to perform novel patterning for various larger-area machining applications, such as nano-fluidic devices, plasmonic devices, nanopores, x-ray zone plates, and other novel direct-write applications. One of the biggest challenges is nonuniform machining artifacts that occur during mosaic patterning, where two pattern regions must be connected. When stitching two adjacent FIB-machined areas together, there is an overmill at the transition point due to the abrupt milling step of the first milled area with the second milled area. A possible solution to reduce these artifacts is the application of ion milling in much lower doses, with or without overlapping edges. Jason demonstrated that edge-to-edge artifacts could be greatly reduced if the material removal was amortized over several milling passes. Another solution is to move the stage under the ion beam, thus expanding the effective ion milling

area so that it is greater than the submillimeter field of view.

For novel FIBs, there were two specific references. The first was part of Jason Sanabia's Raith nanoFIB presentation, where he discussed possible uses for liquid metal ion source alloy-source-based beams. Raith now has alloy sources available, and Jason showed various applications that used gold, silicon, and AuGe cluster beams for nanopore and plasmonic device machining, respectively.

The second area of focus was the presentation by Edward Principe (Tescan USA) on the use of xenon plasma cusp ion sources for TEM prep and other applications. Edward discussed the implementation of a rocking stage into the dual-beam plasma FIB to help mitigate ion beam channeling effects that cause curtaining during cross sectioning and uneven milling due to varying grain orientation. The basic idea is to normalize the material-removal rate by varying the ion beam incident angle on the substrate. Edward also reviewed the addition of new detector hardware to enable large-area 3-D tomography and time-of-flight SIMS in the Tescan dual-beam platform. The last area discussed in the Tescan presentation was the use of xenon beams for delayering. According to Edward, the xenon beam is particularly good for this application, due to its low current density in combination with Tescan's endpoint-detection system.

TEM sample preparation was a very strong theme in this year's User Group meeting, with three of the five presentations covering TEM prep and much of the following discussion focusing on the subject. Jamil Clarke of Hitachi High Technologies America discussed techniques and tooling to achieve ultrathin, low-damage lamellae. The two primary advancements are the inclusion of a seven-axis stage and the incorporation of an argon or xenon ion beam, to eliminate curtaining and to remove amorphized materials, respectively. The seven-axis stage allows the user to reorient the sample during lamella preparation

to improve machining uniformity and eliminate curtaining effects. The inclusion of an argon ion gun into the dual-beam platform (making it a tribeam) enables in situ removal of the damaged region of the lamella caused by the higher-energy Ga<sup>+</sup> ion beam.

Matt Bray of FEI Company presented a review of the three-step process for creating TEM lamellae down to 7 nm. The three steps are "chunking," the process of undercutting the sample substrate; lift-out, the process of moving the chunk from the sample to the TEM grid; and thinning, removing all the material down to the region of interest. Although these techniques are not new per se, the presentation emphasized that all three steps are now highly automated, which enables TEM prep access to a less-experienced user base and improves overall efficiency and prep quality.

The final area of TEM prep was part of Edward Principe's presentation on the Tescan xenon plasma dual-beam platform. Edward discussed the benefits of using a high-current xenon beam to improve lamella prep throughput time. He also discussed building multiple windows into the lamella to expand the analysis region of interest to larger areas.

At the conclusion of the five presentations, the attendees' discussion centered on the merits of using different ion beam species and different beam energies for TEM sample prep and other large-area milling techniques. Much discussion ensued on using xenon beams and damage mitigation when using low-energy gallium or argon ions. The audience was also interested in hearing about other alternative ion sources, such as helium and neon gas-field ion sources (GFIS) and cold beams. It was noted that there was a talk on cesium cold beams in the 2014 User Group and one on neon GFIS in the 2013 User Group but nothing in 2015. Looking to next year, we will pick up the theme of alternative beams and applications.

## ISTFA 2015 SAMPLE-PREP/3-D PACKAGE-PREP USER GROUP

Moderators: Jake Klein, Texas Instruments, and Rose M. Ring, Globalfoundries, Inc.

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**Q**uick and reliable sample preparation, from electron-transparent transmission electron microscopy (TEM) lamellae preparation to 3-D package decapsulation, defines the success of any root-cause

failure analysis (FA) project or request. Sample preparation has been a key topic at ISTFA for decades. The Sample-Preparation User Group meeting has been widely attended, and this year was no different. More than 60 attendees

from semiconductor manufacturers, industry suppliers, universities, and national labs represented various sectors in the FA community, demonstrating the key role sample preparation has in any FA laboratory. This year's session was sponsored by Digit Concept.

Four technical presentations were followed by a question-and-answer panel discussion with five panelists. Mr. Patrick Poirier of Digit Concept (Secqueville-en-Bessin, France) joined the presenters to form the panel at this year's session.

For TEM sample preparation, consistent quality and quick turnaround time are critical challenges for delivering a timely root-cause FA. In his presentation "Updated Sample Preparation and STEM Workflows," Dr. Stephan Kleindiek of Kleindiek Nanotechnik spoke about solutions that could help meet these challenges. He presented an updated TEM sample-preparation and scanning TEM (STEM) imaging workflow using a new loadlock-compatible, mouse-based drag-and-drop in situ lift-out hardware/software (HW/SW) tool. The lift-out tool contains a platform equipped with a microgripper to contact the sample, a three-axis substage system for moving the sample on the SEM stage, and a TEM grid holder. A video showing the different functions and capabilities of the lift-out shuttle HW/SW system was also presented. The tool, coupled with an SEM-compatible glue, was used in lifting and transferring the TEM lamellae to the TEM grid without the use of any ion-beam-assisted deposition or milling process. The same stage also allows sample rotation for inverted TEM sample preparation and STEM imaging and characterization.

For complex IC packages, successful root-cause FA depends on various critical factors. One such critical factor is the preservation of the original state of the "failures" during the package decapsulation process. For plastic-packaged ICs, the process must selectively remove the epoxy mold compounds in a very reasonable time, preserving all the bond wires, bond pads, dice, and, especially, the original defect sites. The process is complicated by the introduction of new and advanced IC packaging with different materials and package concepts, such as system-in-package, 3-D stacked dice, GaAs, bond over active circuit, and copper over anything. This creates the need for a decapsulation tool that can handle a wide range of packages, as well as the need to develop processes that can preserve the integrity of the original failure sites. These requirements present critical challenges to the conventional plasma and acid decapsulation techniques.

Dr. Jaiqi Tang of Jiaco Instruments B.V. presented "High-Performance Decapsulation Technologies for Complex IC Packages." He explored the application of the oxygen-only

atmospheric pressure microwave-induced plasma (MIP) decapsulation technique, using a focused plasma etching approach, as a potential solution to the decapsulation challenges on advanced IC packages. In his overview, he spoke about the principle of the MIP decapsulation tool and technique and its comparison with conventional  $O_2$ - $CF_4$  plasma and acid decapsulation techniques. He presented a few applications on complex ICs of different package materials and stress treatments, such as thermally stressed (high-temperature storage, temperature cycling, highly accelerated stress test) silver and copper wire packages, 3-D stacked-dice packages after laser ablation, electrical-overstress-damaged devices and packages, contaminated dice, and so on.

**"FOR TEM SAMPLE PREPARATION, CONSISTENT QUALITY AND QUICK TURNAROUND TIME ARE CRITICAL CHALLENGES FOR DELIVERING A TIMELY ROOT-CAUSE FA."**



Sample preparation on defect-isolated samples is crucial in yield improvement and technology development. Due to limited failing devices, a high success rate is paramount. After successful nondestructive isolation, an effective sample-preparation technique that preserves the integrity of the failing mode is required. With the decrease in technology node size, increased functionality, and 2.5-D/3-D device buildup, conventional sample-preparation methods are fast reaching their limitations.

Dr. Christian Schmidt of Globalfoundries presented "Sample Preparation for Package FA on 14 nm and 20 nm Technology." He provided an overview and comparison of current state-of-the-art sample-preparation methods and techniques for fault-isolated target defects. He listed key developments and challenges on packaged ICs that define the changing toolsets and approaches to packaged FA, from the shrinking redistribution layer and higher connection density affecting the die-to-die and die-to-substrate interaction to the increasing importance of different assembly technologies, such as through-silicon via and copper pillar contacts, the emergence of 2.5- and 3-D concepts into the manufacturing process, and the effective nondestructive fault isolation techniques, such as lock-in thermography, electro-optical terahertz pulsed reflectometry, acoustic microscopy, and so on. He named a few sample-preparation options, from dicing to mechanical polishing to plasma

FIB cross sectioning and ion milling. The presentation was concluded with a case study involving a T0 package failure, where the package FA flow, involving a few state-of-the-art FA toolsets, was followed. The summary highlighted the growing importance of 3-D x-ray for FA turnaround-time reduction on complex packages as well as plasma FIB for successful package preparation.

Power semiconductor sample-preparation trends in relation to advances in semiconductor architecture and advanced power package design and materials were discussed next. Ian Kearney of Texas Instruments presented “General Power MOSFET/3-D Stacked Die Sample Prep.” He gave an overview of the popular industry FA techniques used on discretes and integrated power devices.

Ian presented various package polishing techniques and discussed a few FA case studies involving discrete

and integrated power chip-scale package/land grid array and 3-D stacked-dice packaged devices. The case studies highlighted package FA challenges involving solder voiding and solder profiling, wire sag isolation, solder cracking, and 3-D multichip-module package decapsulation after temperature cycling (MIP), to name a few.

After the presentations, the session continued with a question-and-answer panel discussion. Several involved conversations took place among the User Group attendees and the panelists about sample-prep challenges and limitations and the opportunities for future trends and directions. Several discussions continued after the session was over. Many thanks to all the participants who stayed until the very end, and special thanks to Digit Concept for their support.

## ISTFA 2015 NANOPROBING USER GROUP

Moderators: John Sanders, DCG Systems, and Nicholas Antoniou, ReVera, Inc.

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A large number of presenters covered a broad spectrum on topics surrounding nanoprobng during the Nanoprobng User Group.

Sweta Pendyala of Globalfoundries started the presentations and addressed how to reduce the time it takes for nanoprobng to localize a defect. Localization techniques such as scanning electron microscopy (SEM)-based voltage contrast and atomic force microscopy (AFM)-based current imaging have been employed to localize defects on bulk semiconductor technology. These techniques cannot be used “as is” for localizing defects on silicon-on-insulator (SOI) technology because there is no direct path to ground from the SOI to the sample chuck. Two different atomic force probe (AFP)-based localization techniques have been successfully implemented to localize defects on SOI technology. The first technique is capacitance-based top-down scanning capacitance localization. In this technique, a low-frequency alternating current signal on the substrate causes a change in capacitance. The amplitude of the signal indicates the amount of dopant and the phase type of dopant. Using a reference part, scanning capacitance can pinpoint the defect area, and then nanoprobng can be performed there. The second technique is a current-imaging-based picocurrent localization technique that has been modified to localize defects on SOI. The AFP provides a current map, and, in SOI, the path to ground

can be provided through the part by using the defect as a detector. For example, one can bias the ground rail and ground  $V_{dd}$ . In summary, scanning capacitance can be used on SOI and is highly sensitive but can cause false positives. Picocurrent localization needs a path to ground, but if one can be found, it rarely gives a false positive.

Two questions were asked by the audience:

- What is the tolerance of the topography? Answer: 15 to 20 nm
- What is the typical raster time? Answer: 2 min

Vinod Narang of AMD Singapore presented the failure analysis for advanced microprocessors. Soft fails, in which an SRAM bit cell exhibits voltage sensitivity, are difficult to analyze. In this work, SEM-based nanoprobng followed by transmission electron microscopy (TEM) was shown to successfully identify the root cause of the failure. The work also highlights that collaboration is needed with design teams to simulate the fails. This helps to explain the nanoprobng and physical failure analysis observations to further confirm and validate the findings. A case study was presented for a built-in self-test soft failure, an SRAM double bit that failed at high voltage and high temperature. By probing each transistor in the SRAM cell, a single transistor was found with low  $I_{dsat}$ . A cross-sectional TEM image of the gate did not explain this failure. By tilting the

sample in the TEM, it was found that the suspected contact was partially missing silicide. A lengthwise cross-sectional TEM confirmed this finding. To confirm that missing silicide would cause this failure, it was simulated in the design and was corroborated this way. Even partially missing silicide can cause the cell to become unstable at high voltage.

A question from the audience was raised: Can the

## “CAN THE MISSING SILICIDE ALSO BE IN OTHER AREAS BUT NOT DETECTED? THE ANSWER WAS YES, IT CAN.”



missing silicide also be in other areas but not detected? The answer was yes, it can.

Shih-Hsin Chang of MA-tek, Hsinchu, Taiwan, also spoke of the challenges facing failure analysis, especially in how to localize failures in the nanoscale. Four cases were introduced to demonstrate how to use an AFM-based nanoprobe (AFP) to achieve this goal. With the help of pico-current imaging, scanning capacitance microscopy, and IV measurements, the location of failures can be precisely identified and the properties of failures can be successfully probed. Sample preparation, on the other hand, is also a difficult task. The probing results on samples prepared by mechanical polish as well as by plasma FIB were demonstrated. The AFP offers high resolution and can have up to eight probe heads and a contact resistance of less than 30  $\Omega$ . In some cases, a failing part must be compared to a standard reference part. Contact resistance is another issue that can be reduced by using a Kelvin probe setup. If localization is lacking, a picocurrent image can narrow down the area, and this can be subsequently marked with a probe and then sectioned for TEM imaging analysis. The probe is used to mark the area of interest.

LiLung Lai of SMIC, Shanghai, China, shared his strategy of device analysis via nanoprobe methodology. In an organization, who decides how to proceed in device analysis? It helps to have a predefined methodology. Can it be done automatically or manually? Is the analysis direct current only or also alternating current? Some fundamentals were presented:

- Compare I-V relationships by nanoprobe
- Look at transfer versus output characteristics ( $I_{on}$ ,  $V_t$ ,  $I_{off}$ )
  - Transfer:  $I_d$ ,  $V_g$ , reflect continuous behavior for MOS

- Output:  $I_d$ ,  $V_d$  reflect current transformer-loop resistance. In the case of an extra diode at the source/drain,  $I_d$ - $V_g$  analysis would miss the electrical signature.
- For a gate stack failure, sweep direct current versus alternating current. Pulsed IV gives a signature of static/read noise margin.

For a 6T cell, I-V data at the contact can reveal a pull-down NMOS mismatch. Having no window for read noise margin proves that it is a single-bit failure. The data analysis for single MOS transistors and single-bit SRAM was included. In using nanoprobe to characterize MOSFETs, one must look at not only the output curves ( $I_d$ - $V_d$ ) but also the transfer characteristics ( $I_d$ - $V_g$ ). For a single-bit SRAM, the complete analysis should include the following I-V data: transfer gate loop, output source drain, and pulsed I-V (and/or noise margin) at metal 1. Also, capacitance-voltage data enhance gate/channel analysis. Pulsed I-V helps with speed-related issues, and pulsed noise margin is necessary to detect resistive gates.

Stephan Kleindiek of Kleindiek Nanotechnik, Reutlingen, Germany, presented new techniques for successful probing experiments (e.g., characterizing a transistor). Success depends on three factors:

- Clean samples, probe tips, and environment
- High-precision positioning capability
- High stability (low drift)

A probing platform with compact dimensions provides these features. Results on 14 nm technology were presented. Prior to transistor characterization lies the task of locating the area of interest.

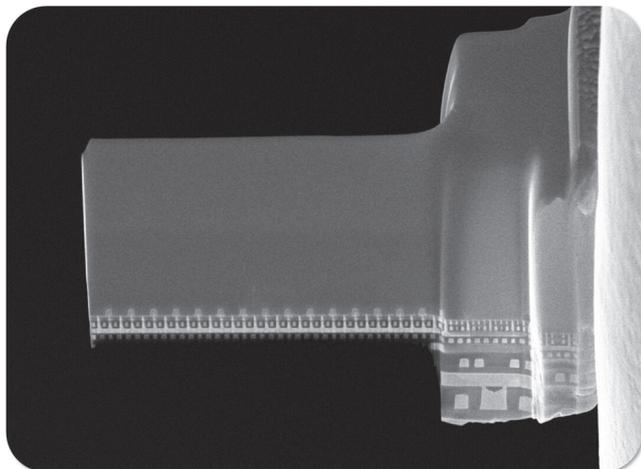
Current imaging (CI) is a method for visualizing/mapping current levels on the sample surface. This method involves the use of a nanomanipulator to land a probe tip on the sample surface and gently sweep the biased tip across the surface while recording the resulting current flow. The surface is scanned similar to a conductive AFM but without the force feedback. While scanning, the probe is lowered and stopped when the signal is detected. Correlative microscopy (typically SEM) can confirm the area. The current path can be configured in various ways by using additional (stationary) probe tips or the sample bulk's contact. The resulting current maps yield insight into the sample's behavior. Recent advances using the CI technique were presented. An example of a leaky gate was shown, as was a beneficial side effect of this technique, which is cleaning out the surface of the sample like a windshield wiper!

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## FEI ANNOUNCES HELIOS G4 DUALBEAM

FEI (Hillsboro, Ore.) announced the new Helios G4 DualBeam series, which offers the highest-throughput ultrathin transmission electron microscopy (TEM) lamella preparation for leading-edge semiconductor manufacturing and failure analysis applications. The new DualBeam series, which includes FX and HX models, takes a significant leap forward in both technological capability and ease of use.

The new Phoenix focused ion beam makes finer



Inverted lamella

cuts with higher precision and simplifies the creation of ultrathin (sub-10 nm) lamella for TEM imaging. The FX is a flexible system that delivers dramatically improved scanning transmission electron microscopy (STEM) resolution—down to sub-3 Å—and significantly shortens the time to data for failure analysis. Images can now be obtained within minutes of completing the lamella, rather than the hours or days previously required to finalize the images on a stand-alone S/TEM system. The HX model is geared specifically for high-throughput TEM lamella production. It features an automated QuickFlip holder that reduces sample preparation times.

“FEI is the first to market with a TEM sample-preparation solution capable of making 7-nm-thick lamella, addressing the needs of our customers who are developing next-generation devices,” states Rob Krueger, Vice President and General Manager of FEI’s semiconductor business. “In

addition, by offering the ability to achieve sub-3 Å image resolution in a DualBeam, failure analysis labs can now dramatically cut time to data without compromising image quality. And, by combining high-resolution imaging and sample preparation on one system, we have reduced the amount of valuable lab real estate required.”

For more information: web: fei.com; tel: 408.224.4024.

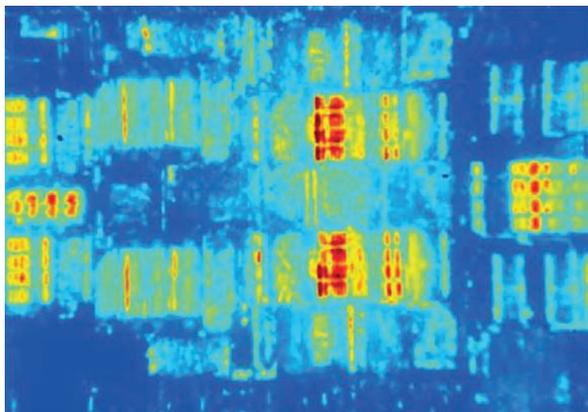
## DCG INTRODUCES MERIDIAN M

DCG Systems (Fremont, Calif.) announced the release of the Meridian M system for isolation of routine and challenging electrical faults at the wafer level. Offering photon emission for transistor-level defects and leakage and a complete portfolio of static laser simulation techniques for metallization defects, the Meridian M system is a critical tool to support production-use cases in memory and foundry failure analysis labs. Its high-sensitivity, extended-wavelength DBX optics capture even the most challenging faults, including:

- Large-area process variation in advanced memory devices that can lead to anomalous leakage
- High-resistivity wordline-to-wordline or bitline-to-bitline shorts within memory cells
- Resistive faults in low-voltage graphics processing units and other low-voltage logic circuits
- Any weakly emitting faults requiring long integration time

The Meridian M system also captures electrical faults that emit photons primarily in the thermal range (>1850 nm), such as partial opens, high-ohmic shorts, and electromigration.

“Static optical fault isolation (OFI) is in a renaissance,” said Praveen Vedagarbha, business unit manager of the Meridian Product Group at DCG Systems. “While dynamic OFI is important for localizing parametric faults, static OFI is faster and easier to use than its dynamic counterpart because it does not require docking to a tester or having the device and tester knowledge necessary to edit the test program. The speed and ease of use of the Meridian M system is particularly valuable in early yield ramp, when rapid feedback to the process engineering team is critical.”



Source: Shehata et al., ISTFA 2014

### Meridian M emission image from 22 nm silicon-on-insulator test chip

Among static-only OFI systems, Meridian M has demonstrated superior performance in localizing faults with the weakest photon emission. Custom-designed optics, a set of user-selectable wavelength ranges, and the lowest background noise in the industry allow Meridian M to be optimized for a variety of fault types, from conventional “optical” emitters such as excessive leakage, saturation, and latch-up faults to longer-wavelength “thermal” emitters, such as high-resistance shorts and dopant displacement errors. Because it accommodates full wafers in addition to packaged die, the Meridian M system allows comparison of good die to bad die, aiding interpretation of complex thermal and photon emission images.

The Meridian product line at DCG Systems leads the industry in active installed base, with wafer-based or packaged-part systems at all leading fabless, foundry, and integrated device manufacturers.

For more information: web: [dcgsystems.com/products/electrical-fault-analysis/meridian-line/meridian-m/](http://dcgsystems.com/products/electrical-fault-analysis/meridian-line/meridian-m/); e-mail: [jet\\_perland@dcgsystems.com](mailto:jet_perland@dcgsystems.com).

## RENISHAW OFFERS inVIA CONFOCAL RAMAN MICROSCOPE

Renishaw (Gloucestershire, U.K.) is an experienced supplier of integrated Raman-atomic force microscopy (AFM) solutions, having offered them for more than 16 years. The latest addition to the range of instruments it supports is Bruker’s Dimension Icon AFM. This additional pairing demonstrates the extreme flexibility of the Renishaw inVia confocal microscope and its capability to interface with a wide range of instruments employing many analytical techniques.

The inVia-Icon is a fully integrated Raman-AFM system. It has a comprehensive range of features, making it the highest-performing yet easy-to-use system for co-localized Raman-AFM measurements. It supports a full range of AFM techniques and  $\mu$ -Raman capabilities and can characterize the properties of materials at submicrometer and nanometer scales.

The Dimension Icon provides users with uncompromised performance, robustness, and the flexibility to perform nearly every AFM measurement type at resolutions previously only obtained by extensively customized systems. The inVia microscope complements this by producing both rich, detailed, chemical images and highly specific Raman data from discrete points. Users can make both Raman and AFM measurements without moving their samples between instruments and without compromising performance. In addition, both instruments can be used independently, if necessary.

The inVia-Icon combination has a flexible arm linking the two instruments; this couples light between the two with mirrors, providing a higher efficiency than fiber optic coupling. This ensures that users can acquire high-quality data in the minimum time with market-leading signal-to-noise levels.

The flexible coupling arm employs Renishaw’s StreamLineHR high-resolution mapping technology. It can Raman map areas up to  $500 \mu\text{m} \times 500 \mu\text{m}$ , with position encoders ensuring 100 nm repeatability. Bruker’s proprietary PeakForce QNM complements StreamLineHR by providing even higher-resolution nanomechanical information.

“Renishaw’s patented sampling arm allows the sample to be measured while it is still mounted on the AFM. Making correlated measurements with both systems is easy,” said Tim Batten, Renishaw applications scientist. He added, “The arm does not contact the AFM and, as such, does not affect its performance.”

Adding inVia’s powerful chemical imaging capabilities to the Bruker Dimension Icon sets a new standard, delivering high-performance surface characterization with both efficiency and ease.

For more information: web: [renishaw.com/en/raman-spm-afm-combined-systems--6638](http://renishaw.com/en/raman-spm-afm-combined-systems--6638); e-mail: [raman@renishaw.com](mailto:raman@renishaw.com).



# TRAINING CALENDAR

Rose M. Ring, Globalfoundries  
rosalinda.ring@globalfoundries.com

## SEMICONDUCTOR ONLINE TRAINING

EDFAS is proud to offer online training specialized for semiconductor, microsystems, and nanotechnology suppliers and users. The online courses are designed to help engineers, technicians, scientists, and managers understand each of these dynamic fields. This one-year subscription provides access to several courses covering semiconductor failure analysis, design, packaging, processing, technology, and testing. Courses in this series, which may be taken anytime or anywhere, bring online training straight to your desk. Take as many as you like—there's no limit—all for one low cost. Find out more by visiting [edfas.org](http://edfas.org) and clicking on Education.

### February 2016

EVENT	DATE	LOCATION
Introduction to Metallurgical Lab Practices	2/9-11	Novelty, OH
How to Organize and Run a Failure Investigation	2/22-23	Foothill Ranch, CA
Introduction to Material Science	2/22-24	Novelty, OH
Principles of Failure Analysis (3 day)	2/24-26	Foothill Ranch, CA

**Contact: ASM International**

2016 FLEX Conference & Exhibition	2/29-3/3	Monterey, CA
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**Contact: 2016 FLEX**

### March 2016

EVENT	DATE	LOCATION
2016 SEMI Industry Strategy Symposium	3/6-8	Nice, France
Practical Interpretation of Microstructures	3/7-10	Rancho Dominguez, CA
Metallographic Techniques	3/14-17	Novelty, OH

**Contact: ASM International**

### March 2016 (cont'd)

EVENT	DATE	LOCATION
Modern Polarized Light Microscopy	3/7-11	Westmont, IL
Raman Microspectroscopy	3/8-10	Westmont, IL
Scanning Electron Microscopy	3/14-18	Westmont, IL

**Contact: McCrone Group**

17th International Symposium on Quality Electronic Design	3/15-16	Santa Clara, CA
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**Contact: 2016 ISQED**

CMOS, BiCMOS, and Bipolar Process Integration	3/21-22	Albuquerque, NM
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Wafer Fab Processing	3/29-4/1	San Jose, CA
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**Contact: Semitracks, Inc.**

### April 2016

EVENT	DATE	LOCATION
Component Failure Analysis	4/4-7	Novelty, OH
Principles of Failure Analysis (4 day)	4/11-14	Novelty, OH
Metallographic Interpretation	4/18-21	Westlake, OH

**Contact: ASM International**

### Contact Information

#### ASM International

Tel: 800.336.5152, ext. 0  
e-mail: [MemberServiceCenter@asminternational.org](mailto:MemberServiceCenter@asminternational.org)  
Web: [asminternational.org](http://asminternational.org)

#### McCrone Group

Tel: 630.887.7100  
Web: [mccrone.com](http://mccrone.com)

#### Semitracks, Inc.

Tel: 505.858.0454  
e-mail: [info@semitracks.com](mailto:info@semitracks.com)  
Web: [semitracks.com](http://semitracks.com)

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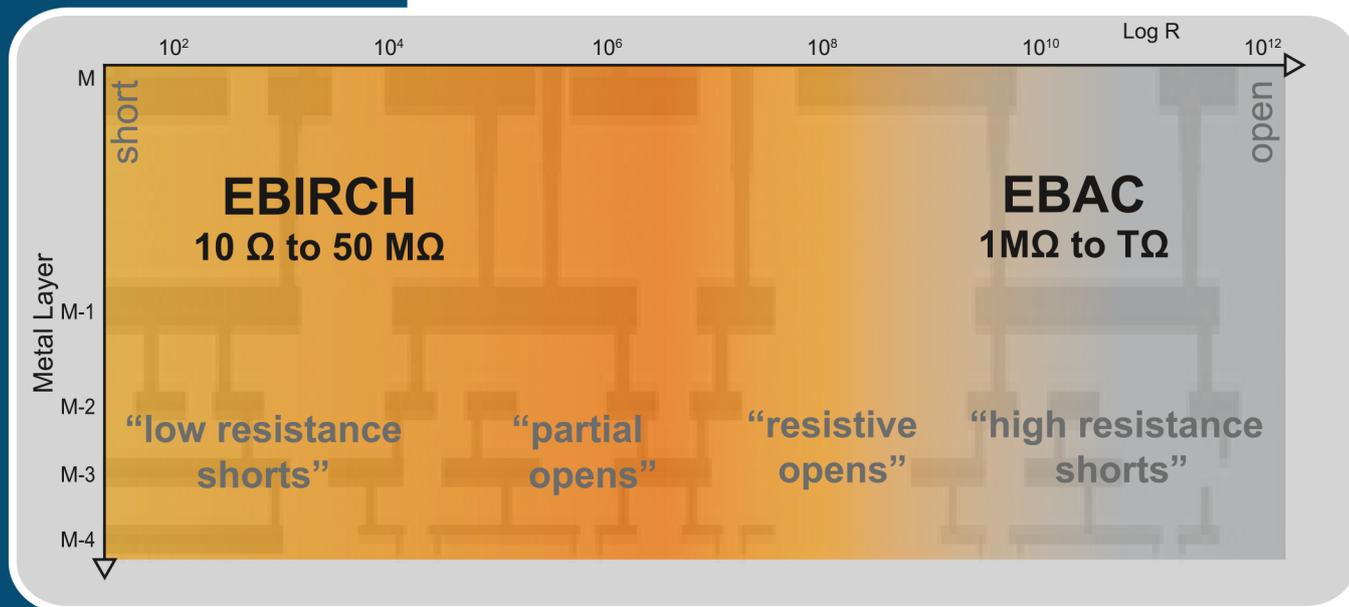
#### 2016 SEMI ISS-Europe

Christina Fritsch  
Tel: +49 3030 3080 77 0  
e-mail: [cfritsch@semi.org](mailto:cfritsch@semi.org)  
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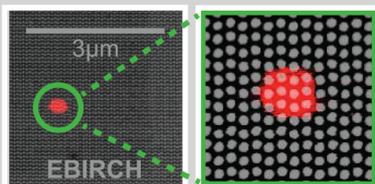
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# BOARD OF DIRECTORS NEWS

## EDFAS BOARD OF DIRECTORS REPORT

Bill Vanderlinde, EDFAS Secretary, IARPA  
[william.vanderlinde@iarpa.gov](mailto:william.vanderlinde@iarpa.gov)

The EDFAS Board of Directors held its annual face-to-face meeting on Saturday, October 31, 2015, in Portland, Ore., preceding the ISTFA event. Board President Cheryl Hartfield kicked off the meeting with the President's report, a high-level review of 2015 accomplishments and challenges. In her report, she discussed future success based on volunteerism, new unique products for the membership, becoming masters of digital content, and maintaining/improving existing products. The Board approved a new mission statement, which will be brought to the membership for a vote in the near future.

Executive Director Terry Mosier of ASM International shared EDFAS year-end financial projections forecasting overall positive performance. He provided an organizational update and reported on the very first ASM affiliate society summit, which was held this past July in Materials Park, Ohio, with Board Vice President Zhiyong Wang representing EDFAS. The goal was to increase strategic engagement between the affiliate societies and the ASM Board and to address the challenges that are common across the affiliate societies. He also discussed the Materials Advantage, a partnership with other professional groups, including TMS, AIST, and ACerS. He sees opportunities in the field of additive manufacturing (3-D printing).

Committee chairs shared year-to-date progress and 2016 plans for their respective areas, covering membership, *EDFA* magazine, education, ISTFA, the journal, and international growth. A common theme throughout the Board meeting was that of identifying ways to strengthen the value EDFAS brings to its members.

Felix Beaudoin, Editor of *EDFA*, reported that the magazine continues to have excellent technical content and strong advertising. An expanded Editorial Board is adding new departments. A digital edition has gone live. Please contact Felix if you are interested in writing an article!

Looking forward to next year, General Chair Martin Keim provided a preview of ISTFA 2016 in Fort Worth, Texas, which will be themed "The Next Generation." Efrat Moyal was announced as Technical Program Chair. ISTFA 2016 will be at the same location and on consecutive weeks with the International Test Conference, providing opportunities for collaboration and shared attendees.

David Su, Chair of the International Growth Committee, reviewed the significant progress in working with our partners in Asia (IPFA) and Europe (EUFANET, ANADEF, and ESREF).

The Board continues to pursue international collaborations, virtual content, and social media using web-based technologies. They are also seeking to better leverage EDFAS volunteers and are looking to implement failure analysis tool roadmapping.

The Board of Directors strives to strengthen the visibility and credibility of our Society by providing value to EDFAS members and, through its volunteers, beneficial contributions to our industry. Your engagement in EDFAS is highly encouraged. Please feel free to connect with any Board member to discuss your ideas or interest in volunteering in the Society.



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# LITERATURE REVIEW

## Peer-Reviewed Literature of Interest to Failure Analysis: Reliability, Counterfeit Electronics, and Reverse Engineering

Michael R. Bruce, Consultant  
mike.bruce@earthlink.net

The current column covers peer-reviewed articles published since 2013 on reliability, counterfeit electronics, and reverse engineering. All of these fields are dependent on failure analysis for their success. Furthermore, failure mechanisms are fundamental to reliability understanding. Feel free to share the following with your reliability colleagues. Note that inclusion in the list does not vouch for the article's quality, and category sorting is by no means strict.

If you wish to share an interesting recently published peer-reviewed article with the community, please forward the citation to the e-mail address listed above and I will try to include it in future installments.

Entries are listed in alphabetical order by first author, then title (in bold), journal, year, volume, and first page. Note that in some cases bracketed text is inserted into the title to provide clarity about the article subject.

- U. Chand, K.C. Huang, C.Y. Huang, et al.: "**Investigation of Thermal Stability and Reliability of HfO<sub>2</sub> Based Resistive Random Access Memory Devices with Cross-Bar Structure**," *J. Appl. Phys.*, 2015, 117, p. 184105.
- M.K. Chen, Y.J. Huang, C.C. Cheng, et al.: "**Failure Analysis of EOS-Induced Damage at Final Electrical Testing**," *J. Mater. Sci.: Mater. Electron.*, 2014, 25, p. 596.
- Y. Chen, L. Yang, C. Ye, et al.: "**Failure Mechanism Dependence and Reliability Evaluation of Non-Repairable System**," *Reliab. Eng. Syst. Saf.*, 2015, 138, p. 273.
- S. Chih-Hsiang, K.Y. Soo, and R. Kaushik: "**Ultra-Thin Dielectric Breakdown in Devices and Circuits: A Brief Review**," *Microelectron. Reliab.*, 2015, 55, p. 308.
- D.P. Ettisserry, N. Goldsman, A. Akturk, et al.: "**Negative Bias-and-Temperature Stress-Assisted Activation of Oxygen-Vacancy Hole Traps in 4H-Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors**," *J. Appl. Phys.*, 2015, 118, p. 044507.
- U. Guin, D. DiMase, and M. Tehranipoor: "**Counterfeit Integrated Circuits: Detection, Avoidance, and the Challenges Ahead**," *J. Electron. Test.: Theory Applic. (JETTA)*, 2014, 30, p. 9.
- U. Guin, D. DiMase, and M. Tehranipoor: "**A Comprehensive Framework for Counterfeit Defect Coverage Analysis and Detection Assessment**," *J. Electron. Test.: Theory Applic. (JETTA)*, 2014, 30, p. 25.
- U. Guin, K. Huang, D. DiMase, et al.: "**Counterfeit Integrated Circuits: A Rising Threat in the Global Semiconductor Supply Chain**," *Proc. IEEE*, 2014, 102, p. 1207.
- K. Huang, Y. Liu, N. Korolija, et al.: "**Recycled IC Detection Based on Statistical Methods**," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, 2015, 34, p. 947.
- K.E. Kambour, C. Kouhestani, P. McMarr, et al.: "**Negative Bias Temperature Instability Threshold Voltage Shift Turnaround in SiGe Channel MOSFETs**," *J. Vac. Sci. Technol. B*, 2015, 33, p. 022201.
- V.G. Karpov: "**Understanding the Movements of Metal Whiskers**," *J. Appl. Phys.*, 2015, 117, p. 235303.
- K.T. Kaschani: "**What Is Electrical Overstress? Analysis and Conclusions**," *Microelectron. Reliab.*, 2015, 55, p. 853.
- C.M. Lin: "**Estimation of ACF Packaging Failure Probability for IC/Substrate Assemblies with Different Pad Array Dimensions**," *J. Mater. Sci.: Mater. Electron.*, 2014, 25, p. 618.
- D. Lock, K.R. Rusimova, T.L. Pan, et al.: "**Atomically Resolved Real-Space Imaging of Hot Electron Dynamics [in Si]**," *Nature Commun.*, 2015, 6, p. 8365.
- K. Mahmood, P. Carmona, S. Shahbazmohamadi, et al.: "**Real-Time Automated Counterfeit Integrated Circuit Detection Using X-Ray Microscopy**," *Appl. Opt.*, 2015, 54, p. D25.
- M. Miao, Y. Zhou, and J.A. Salcedo: "**Compact Failure Modeling for Devices Subject to Electrostatic Discharge Stresses—A Review Pertinent to CMOS**

- Reliability Simulation,”** *Microelectron. Reliab.*, 2015, 55, p. 15.
- I. Moukhtari, V. Pouget, F. Darracq, et al.: **“Negative Bias Temperature Instability Effect on the Single Event Transient Sensitivity of a 65 nm CMOS Technology,”** *IEEE Trans. Nucl. Sci.*, 2013, 60, p. 2635.
  - S.P. Ogden, J. Borja, J.L. Plawsky, et al.: **“Charge Transport Model to Predict Intrinsic Reliability for Dielectric Materials,”** *J. Appl. Phys.*, 2015, 118, p. 124102.
  - M. Pecht: **“The Counterfeit Electronics Problem,”** *Open J. Soc. Sci.*, 2013, 1, p. 12.
  - A. Shrivastava and M. Pecht: **“Counterfeit Capacitors in the Supply Chain,”** *J. Mater. Sci.: Mater. Electron.*, 2014, 25, p. 645.
  - S. Tyaginov, M. Bina, J. Franco, et al.: **“On the Importance of Electron-Electron Scattering for Hot-Carrier Degradation,”** *Jpn. J. Appl. Phys.*, 2015, 54, p. 04dc18.
  - J.B. Velamala: **“Failure Analysis of Asymmetric Aging under NBTI,”** *IEEE Trans. Dev. Mater. Reliab.*, 2013, 13, p. 167.
  - Y. Wang and P.S. Ho: **“Mode II Electromigration Failure Mechanism in Sn-Based Pb-Free Solder Joints with Ni Under-Bump Metallization,”** *Appl. Phys. Lett.*, 2013, 103, p. 121909.
  - Q. Wu, M. Porti, A. Bayerl, et al.: **“Channel-Hot-Carrier Degradation of Strained MOSFETs: A Device Level and Nanoscale Combined Approach,”** *J. Vac. Sci. Technol. B*, 2015, 33, p. 022202. ■



## GUEST EDITORIAL

(CONTINUED FROM PAGE 2)

with secret codes becomes much more reliable and successful. Backside CE also offers access to all active devices for writing and duplication of access codes. As one publication put it, it is like “breaking and entering” IC security. Also, it is much harder to protect the backside, because alignment of frontside to backside for contacting is almost impossible, or very expensive with through-silicon vias.

However, optical backside attacks need to transfer the logic circuit information through bulk silicon, and the photons need to have smaller energies than the silicon bandgap to avoid much electron-hole pair generation, which would shorten the penetration depth too much for easy device preparation. This is practically limiting the microscope’s wavelength to approximately 1  $\mu\text{m}$ . Conventional optical microscopes would then have a feature-size resolution limit in the same range. If we think of optically separating the smallest units carrying local data, MOS transistors, which consist of the gate as the smallest feature and require source, drain, and isolation that are each a little relaxed in size, we typically end up with a node size of approximately 8 times minimum feature size. This means the attack risk with conventional microscopes is given as long as the technology is 120 nm or larger. Therefore, the rapid move to smaller feature sizes of 90 or 60 nm, even down to 22 nm, seems to offer a certain protection against optical SCAs in the future.

The progress of electronic device FA tools and techniques continues to feed the hacker’s dreams and maintains

the threat to security systems in ICs. This is especially important for newer FA tool developments, such as solid immersion lenses (SILs) or visible light access for nanoscale feature sizes. It all depends on how quickly hackers take on the opportunities offered by recent FA developments. Also, on the protection side, advanced FA tools are expensive and not easy to apply.

In the end, it becomes a question of how available advanced FA is to a hacker, who won’t invest millions of dollars in latest-generation tools. However, commercial labs that offer their equipment on an hourly basis are possible sources that could serve in attacks. Also, universities with more public access might be an open door. We at TU Berlin look very closely at who is operating our tools. Another path to facilitate an attack is to find very inexpensive ways to obtain advanced FA performance through simple microscopes, handcrafted parts such as SILs, and so on. It is very hard to make assumptions about where in the world a few people may exist who are capable of doing all of this successfully.

Failure analysis tools will always challenge secret information in ICs, so only backside protection is the solution. This is the key activity in the security community today. Because we know how inventive FA engineers are, we can assure the developers of IC hardware protection: It does and always will require a lot of creativity to improve protection against the power of silicon debug and diagnosis development. ■

# DIRECTORY OF INDEPENDENT FA PROVIDERS

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Electronic companies of all types and sizes require failure analysis (FA) services. The availability of independent laboratories, contractors, and consultants to provide these services is critical as more and more electronic companies adopt the “fabless-to-labless” product engineering business model. The service providers are needed as an outsourced capability for the “labless” companies, while other companies need services to add short-term capacity to their lab, to complement in-house capabilities, or to overcome issues with equipment failures. The independent FA service providers offer consulting, electrical testing, quality and reliability stress and testing, material, electrical, and physical FA services. Our goal is to provide a resource of FA service providers for your reference files. The directory lists independent providers serving various types of electronic companies and includes the address, contact information, expertise, and types of technical services offered by each provider.

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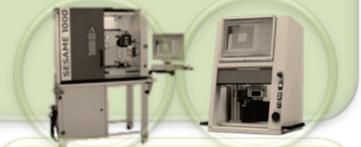
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# NOTEWORTHY NEWS

## IRPS CONFERENCE

The IEEE International Reliability Physics Symposium's (IRPS) annual conference will be held **April 17 to 21, 2016**, at the Pasadena Convention Center in Pasadena, Calif.

The IRPS technical program includes technical sessions, keynote and invited talks on emerging issues, tutorials, workshops, an evening poster session, a year-in-review seminar, panel discussions, and equipment demonstrations. Special attention is given to the reliability of advanced CMOS scaling, new materials introduction, new processes or integration strategies, and/or fundamentally new device architectures. Attendees returning from the IRPS will be better equipped to solve critical reliability problems and develop effective qualification procedures that affect their companies' bottom line.

The IRPS Conference is sponsored by the IEEE Reliability Society and IEEE Electron Device Society. For more information, visit the IRPS website at [irps.org](http://irps.org).



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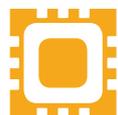
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# 50 Years of Polishing...

## and We Haven't Scratched the Surface

This year **ULTRA TEC Manufacturing, Inc. celebrates 50 years of business.** Over this time we've seen the birth and growth of a number of high-tech industry sectors. We've supplied sample prep equipment to most of them. Over the years we have provided equipment that in some small way aided the growth of the fiber-optic backbone, mapping the human genome and the development of myriad optical, medical, analytical, and semiconductor products. We've helped engineers, reverse engineers, space scientists, smart card companies, game designers, police forces, service labs, and product developers not only to "Do their thing" but to "Do their thing **BETTER!**"

**Our saws and polishers have been used throughout the semiconductor industry since the mid-1980s** - seeing growth as our customers moved from manual polishing to semi-automatic polishing. The launch of the first ASAP-1 product in 1999 expanded our focus to enabling the FA sector's move to backside analysis of the die.

Recent years have provided new challenges and opportunities, with the growth of mobile devices and the attendant need for faster, thinner, larger, smaller, 2D, 2.5D, and 3D IC devices.

As Moore's Law continues to be followed, bent, modified and exceeded, we would like to think there will always be an ULTRA TEC product at hand to help the FA Engineer figure out just what went wrong with their company's IC.

For every EMMI, every SQUID, every FIB, every SIMS, every SIFT, every SIL ... There's an ULTRAPOL, ULTRASLICE or ASAP-1 ready to prepare your sample!

**So, to our customers and friends - we thank you for your business and we look forward to joining you in meeting the technical challenges of the next 50 years together!**

The ULTRA TEC Team

### ASAP-1

1999



2007



2015



### ULTRASLICE

1983



1995



2015



### ULTRAPOL

1984



1996



2015



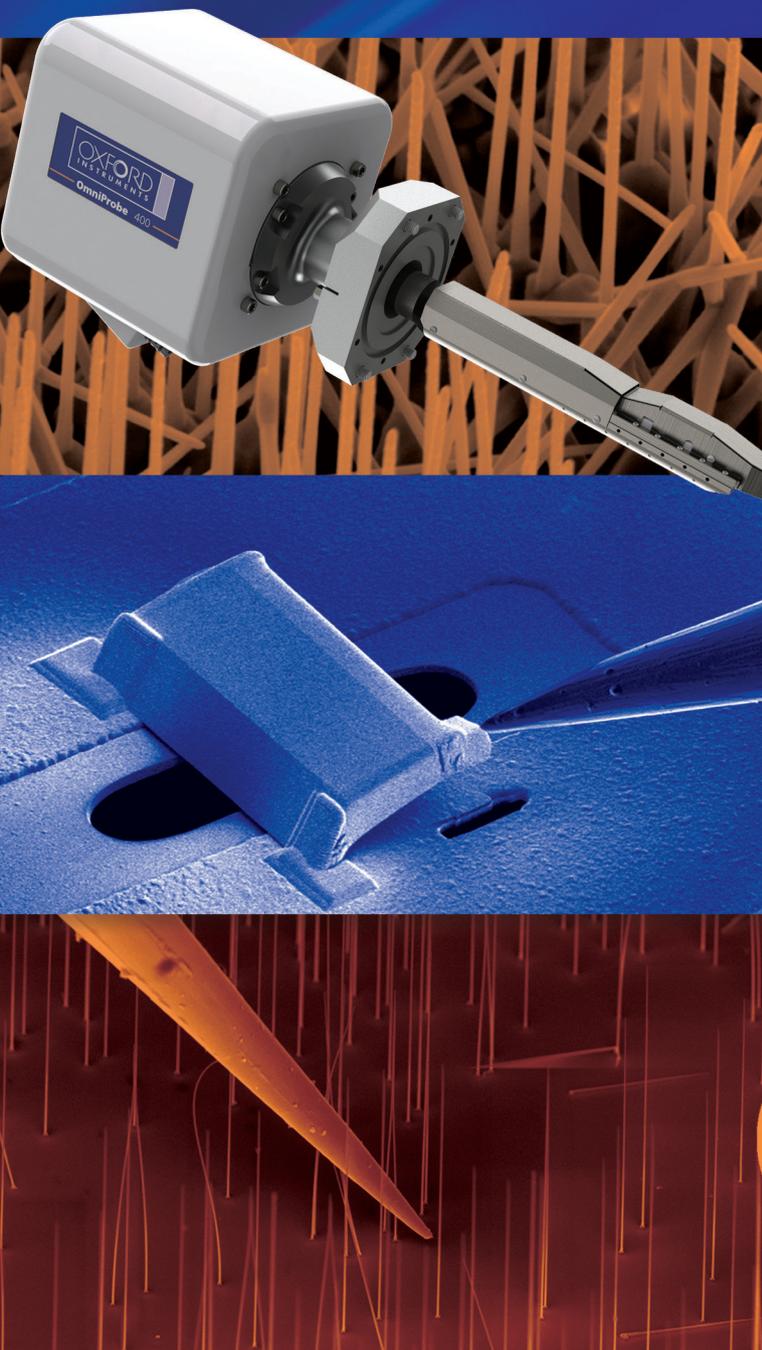
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# ANALYSIS

## OmniProbe® 400 nanomanipulator

Fast, precise, reliable - and no slip-stick effect

# PREP



**OmniProbe** 400 delivers efficient nanomanipulation and analysis - even for advanced applications at the nanoscale.

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- Precision for sub 100nm structures using closed-loop control
- Efficient omnidirectional motion from millimeters to nanometers
- Compucentric rotation for fast plan-view samples and inverted sample placement

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